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Section : 11

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HOMEWORK 10

P1. a

PRESENT STATE	NEXT $W=0$	NEXT $W=1$	OUTPUT
A	A	B	0
B	B	C	1
C	C	D	2
D	D	A	3

b.

Y_1	Y_0	$W=0$: Y_1Y_0	$W=1$: Y_1Y_0	Z_1Z_0
0	0	00	00	00
0	1	01	01	01
1	0	10	10	10
1	1	11	11	11

c.

W	Y_1	Y_0	Y_1	Y_0	Z_1	Z_0
0	0	0	0	0	0	0
0	0	1	0	1	0	1
0	1	0	1	0	1	0
0	1	1	1	1	1	1
1	0	0	0	1	0	0
1	0	1	1	0	0	1
1	1	0	1	1	1	0
1	1	1	0	0	1	1

Y_1

$W \backslash Y_1Y_0$	00	01	11	10
0	0	0	1	1
1	0	1	0	1

$Y_1 = Y_1\overline{W} + Y_1\overline{Y_0} + \overline{Y_1}Y_0W$

Y_0

$W \backslash Y_1Y_0$				
	0	1	1	0
	1	0	0	1

$Y_0 = Y_0 \oplus W$

Z_1

w \ y_1y_0	00	01	11	10
0	0	0	1	1
1	0	0	1	1

$\Rightarrow$

Z_1

y_0 \ y_1	0	1
0	0	1
1	0	1

$Z_1 = Y_1$

Z_i only depended on y_i $(i = 0, 1)$

Z_0

w \ y_1y_0	00	01	11	10
0	0	1	1	0
1	0	1	1	0

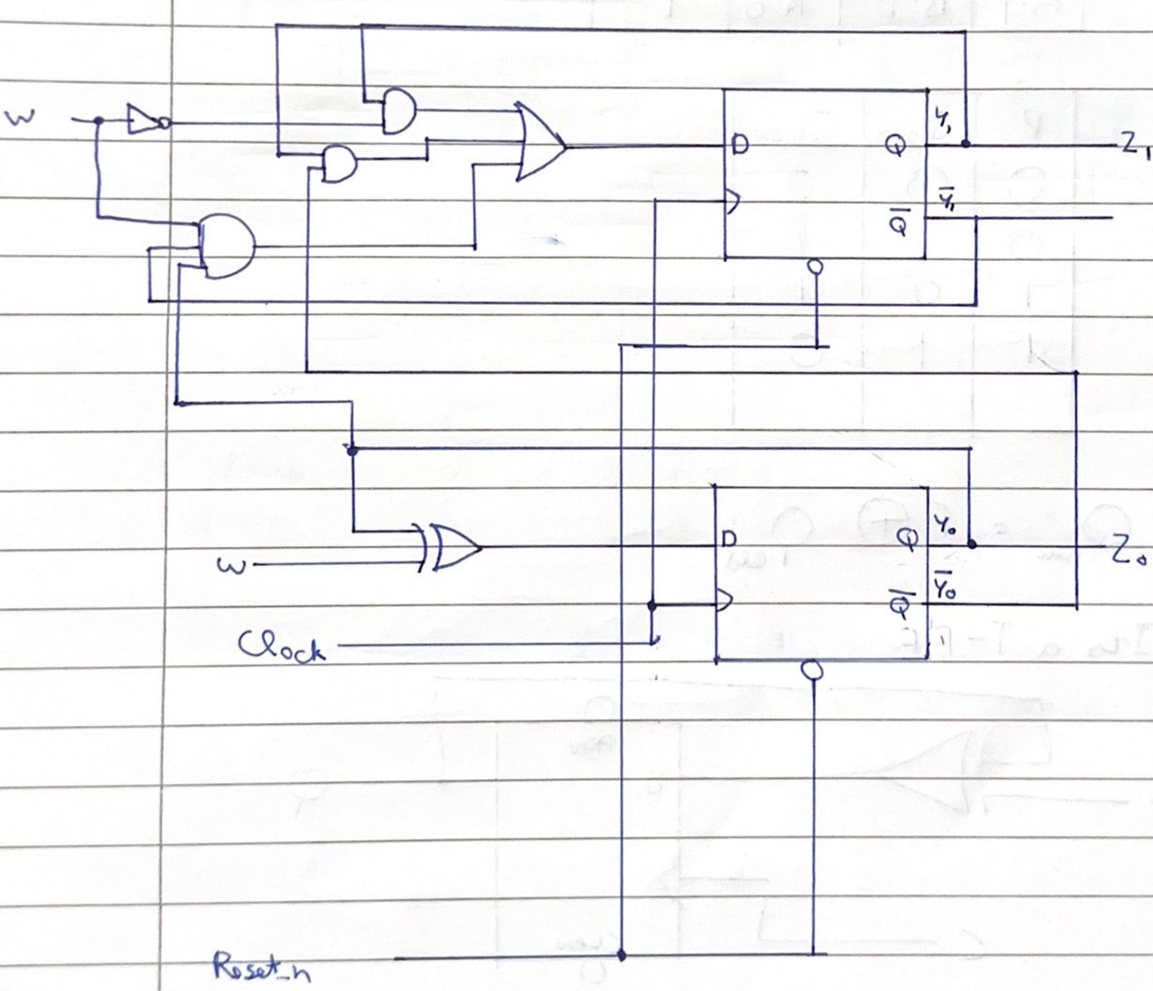
$\Rightarrow$

Z_0

	0	1
0	0	0
1	1	1

$Z_0 = Y_0$

d.

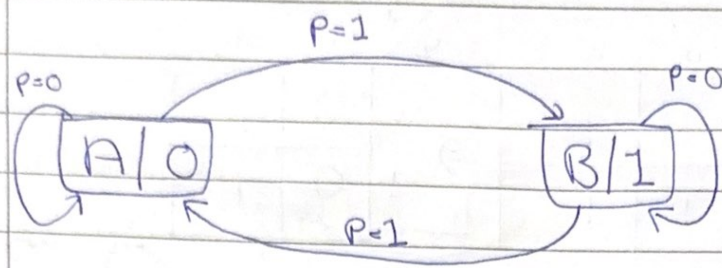


e. FSM, when $w=0$; Points back to same state.

FSM when $w=1$; Points to the next state.
(upcount in binary). ($A \to B$ or $B \to C$ or $C \to D$ or $D \to A$)

P2.

a.



b.

	P=0	P=1	Q
A	A	B	0
B	B	A	1

c.

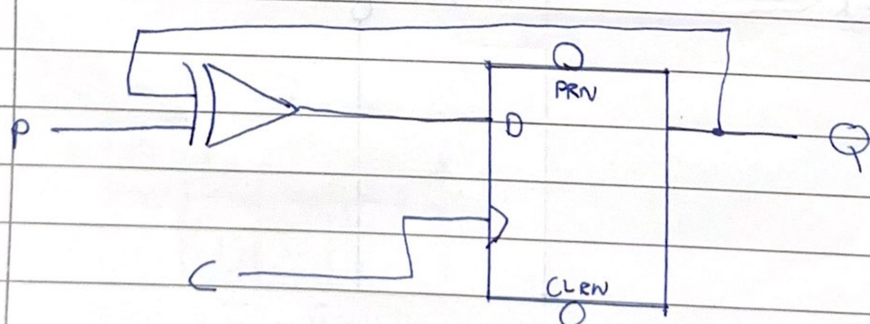
	P=0	P=1	Q
A:0	A:0	B:1	0
B:1	B:1	A:0	1

d.

P	Q_{OLD}	Q_{NEW}
0	0	0
0	1	1
1	0	1
1	1	0

e. $Q_{new} = P \oplus Q_{old}$

f. Its a T-FF



P3. Counting Sequence: 000, 001, 010, 111

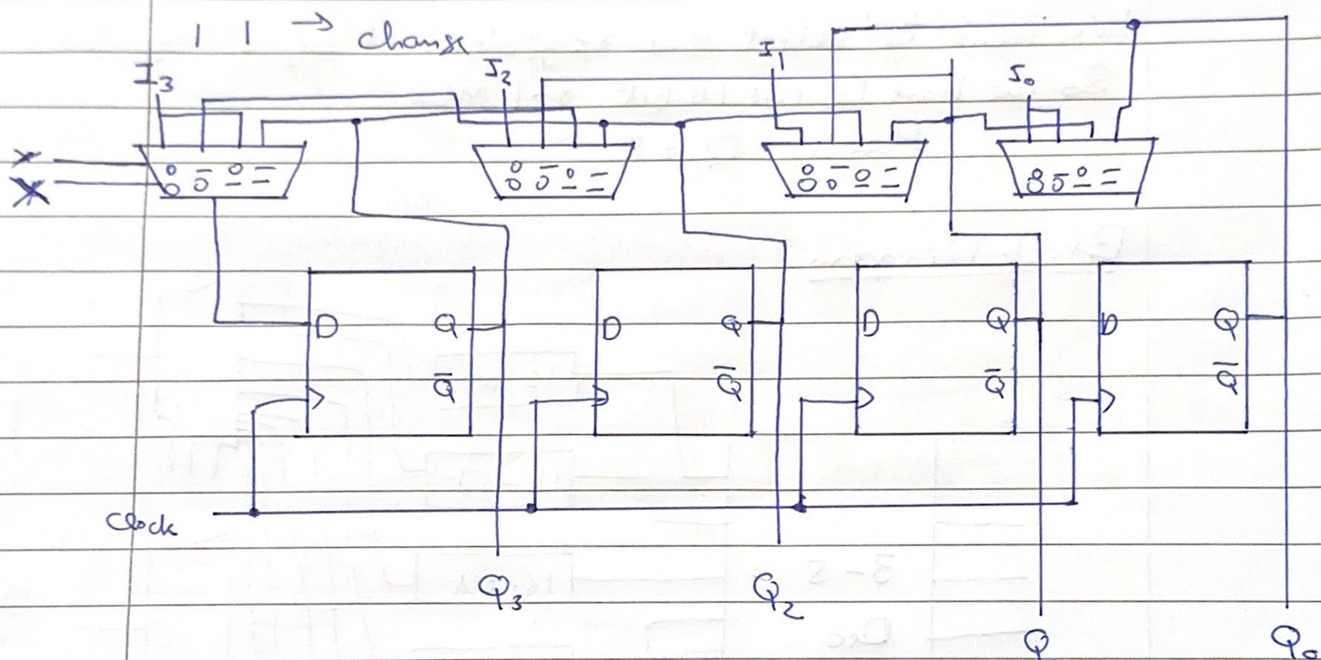
P4. X Y

0 0 → new data

0 1 → shift left

1 0 → " right

1 1 → change



P5. There are eight 16-bit registers. We can access those 8 registers using 1 3-8 decoder.

$W = 1,\ X = 3,\ Y = 8$

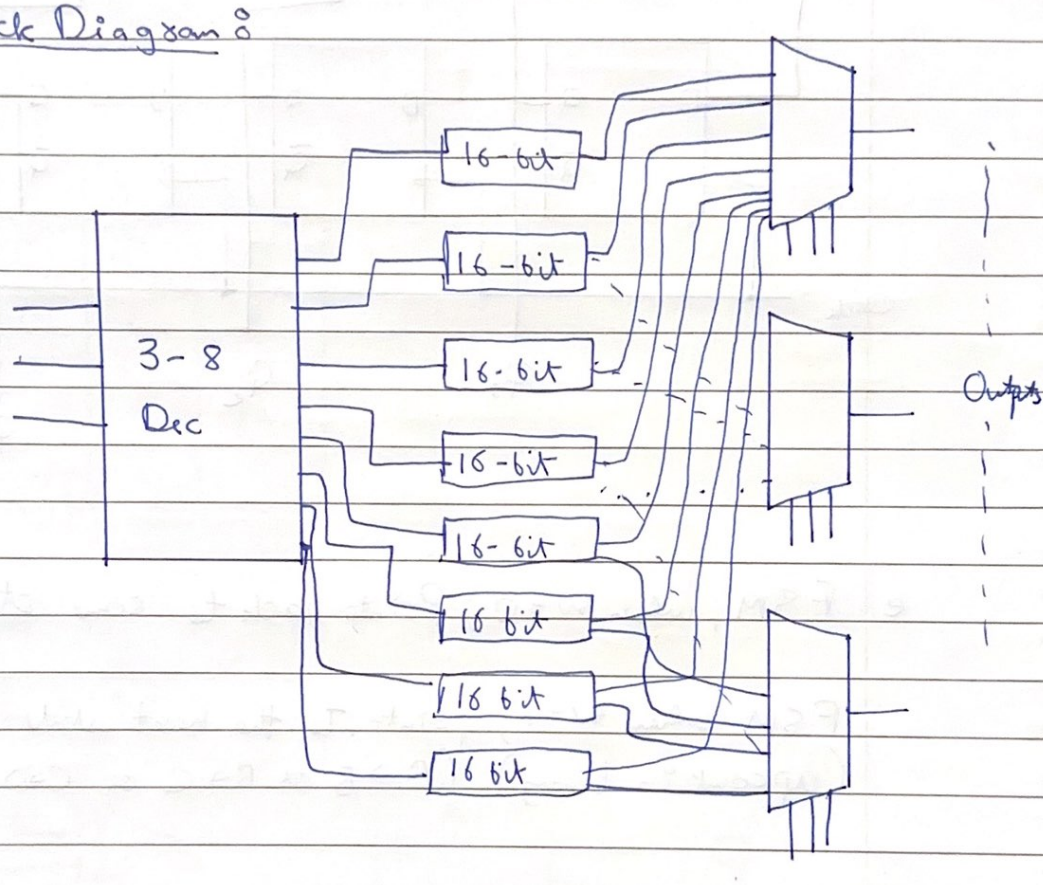
3 output ports means we need 3 MUX's.

Hence, $Z = 3$.

We need to select one register out of 8 registers. So we have to use 16 bit 8-1 MUX.

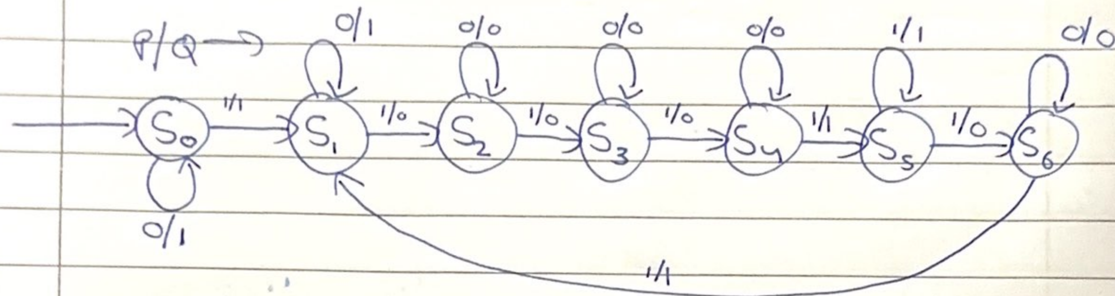
Hence, $Q = 8$

Block Diagram :

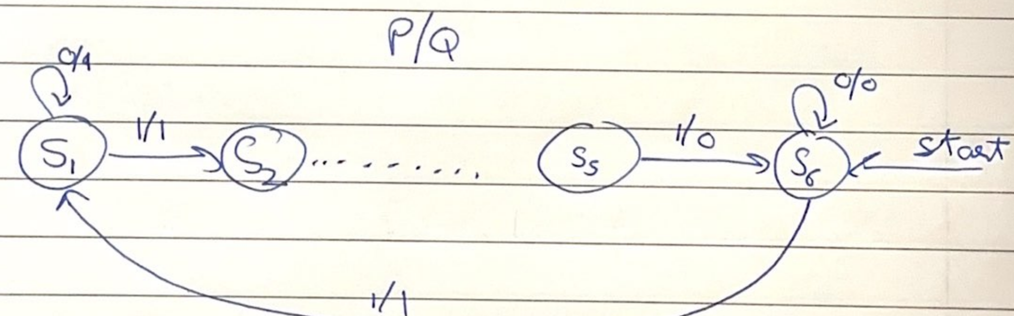


$W=1,\ X=3,\ Y=3,\ Z=3,\ Q=8$

P6. Since, we are only concerned with number of 1's, we can ignore the 0's by changing state only when P = 1.
We start in a special state S_0 where Q = 1 because we have no 1's yet.
Each time we have P=1, we advance to the next state, so it's basically counting 1's.
When it gets to 6, that is div. by 2 & 3, we can restart.



Alternative with O defined as divisible by 2 or 3.
Six states instead of Seven.



It is a Mealy machine. This has an output value rather than a final state.
Moreover, its output values are determined both by its current state and current inputs