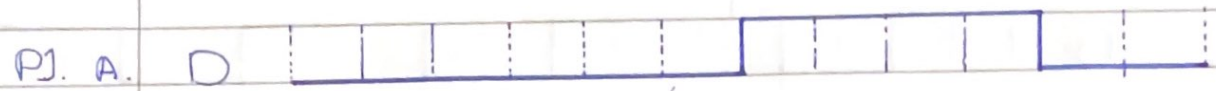
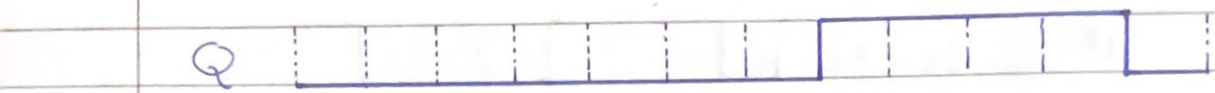
ARYAN RAO
ID: 26495748 /__/____
SEC : 11

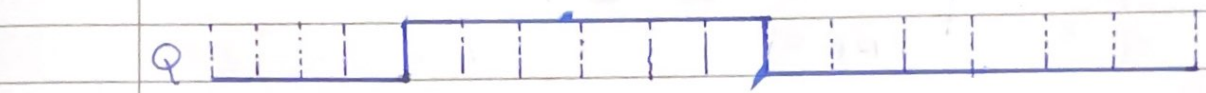
HOMEWORK 8

PJ. A.





B.



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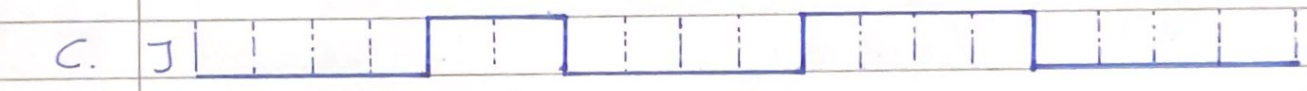
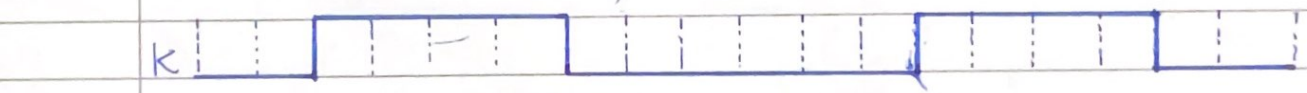
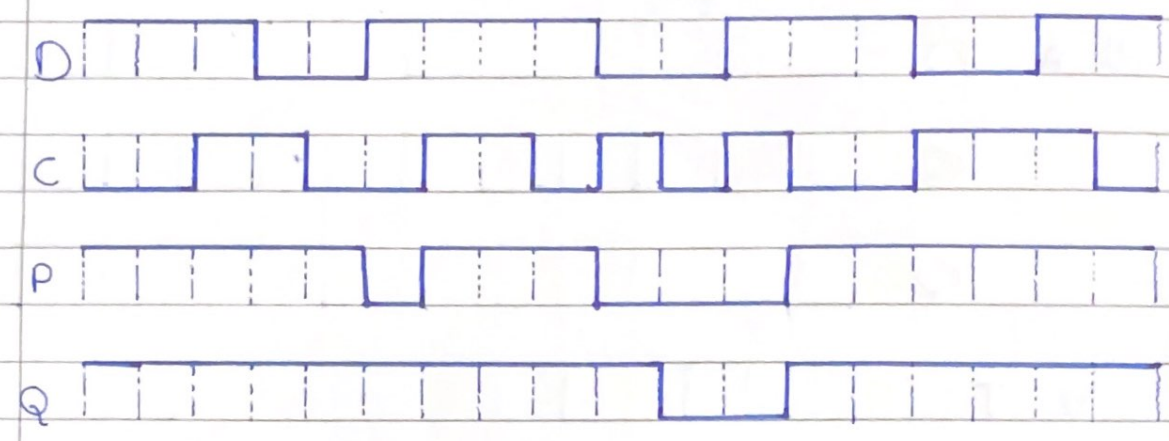




D.



P2. A. Gated SR Latch with NAND Gates

B.

C	S	R	Q	P
0	0	1	Memory	Memory
0	1	0	Memory	Memory
0	1	1	Memory	Memory
1	0	0	Memory	Memory
1	0	1	0	1
1	1	0	1	0
1	1	1	0	0

C.

Memory State:

Goes to memory state in conditions like (0, x, x) & (1, 0, 0) i.e.

$C = 0, \; S = X, \; R = X$

&

$C = 1, \; S = 0, \; R = 0$

Undesirable State:

When

$C = S = R = 1$

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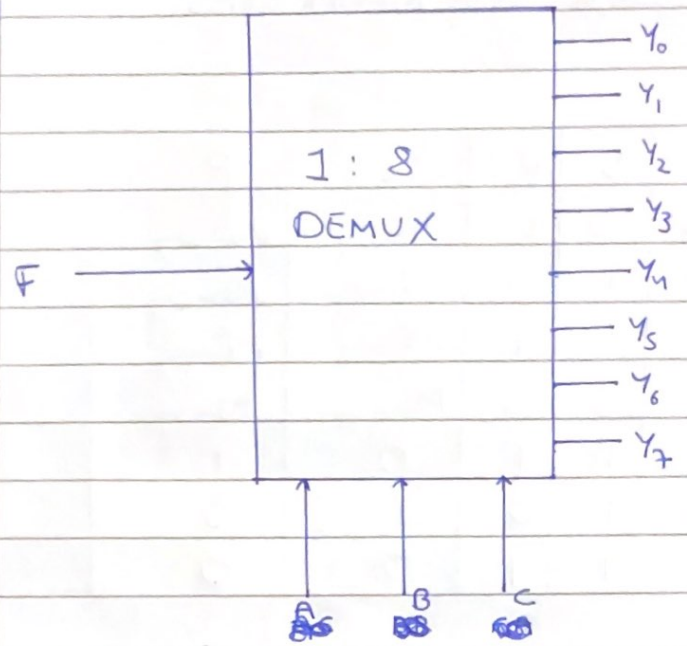
P3. a)



$Y_0 = \bar{C}\bar{B}\bar{A}F$
$Y_1 = \bar{C}\bar{B}AF$
$Y_2 = \bar{C}B\bar{A}F$
$Y_3 = \bar{C}BAF$
$Y_4 = C\bar{B}\bar{A}F$
$Y_5 = C\bar{B}AF$
$Y_6 = CB\bar{A}F$
$Y_7 = CBAF$

$Y_0 = \bar{A}\bar{B}\bar{C}F$
$Y_1 = \bar{A}\bar{B}CF$
$Y_2 = \bar{A}B\bar{C}F$
$Y_3 = \bar{A}BCF$
$Y_4 = A\bar{B}\bar{C}F$
$Y_5 = A\bar{B}CF$
$Y_6 = AB\bar{C}F$
$Y_7 = ABCF$

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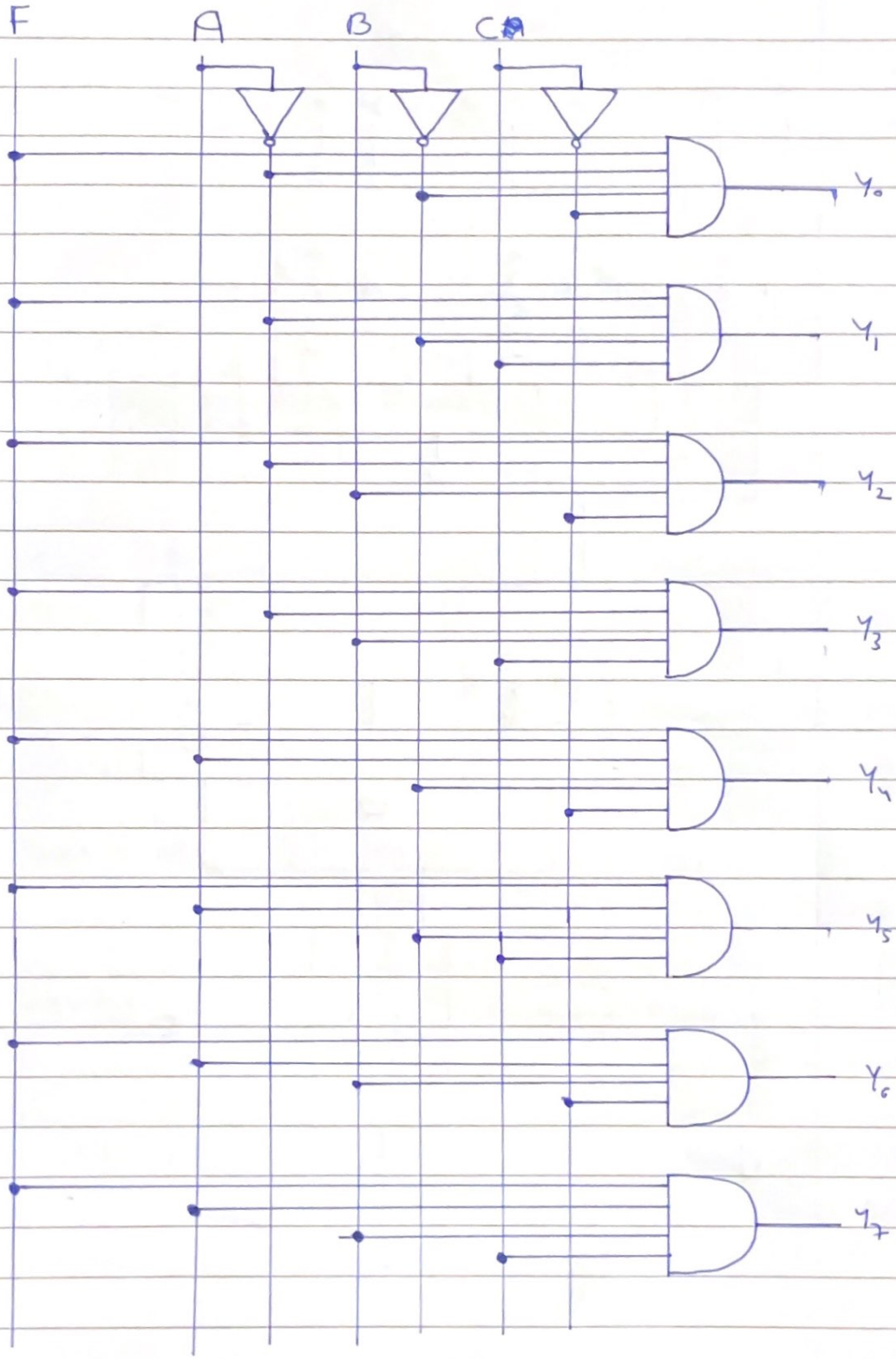
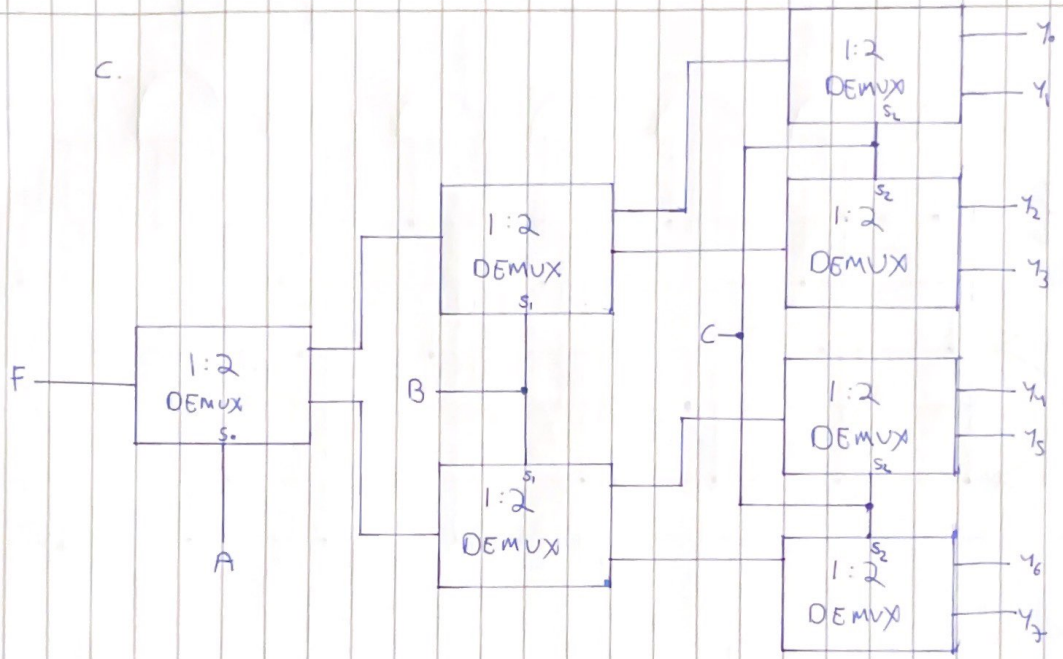
b.

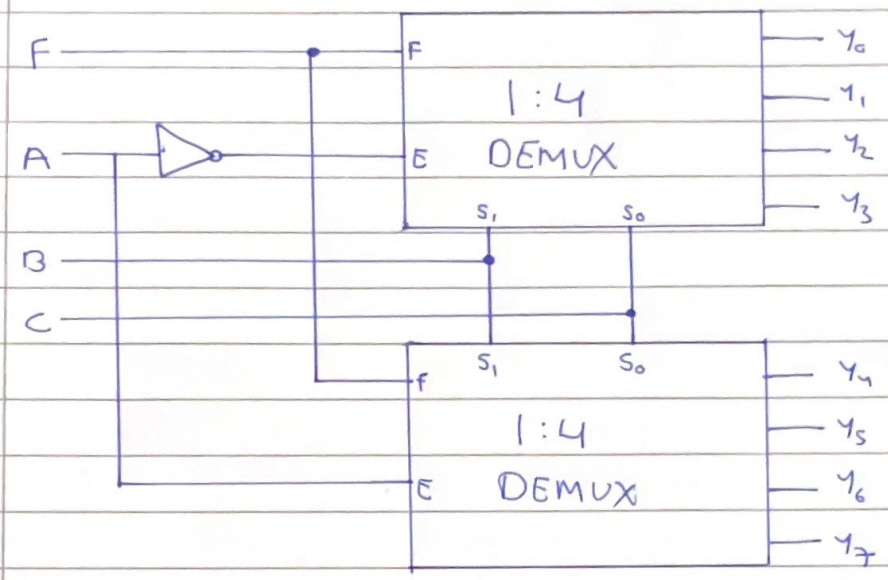


C.


1:2 DEMUX
1:2 DEMUX
1:2 DEMUX
1:2 DEMUX
1:2 DEMUX
1:2 DEMUX
1:2 DEMUX
F
A
B
C
S_0
S_1
S_2
S_2
S_2
S_2
S_1
S_2
Y_0
Y_1
Y_2
Y_3
Y_4
Y_5
Y_6
Y_7

__/__/____

d.



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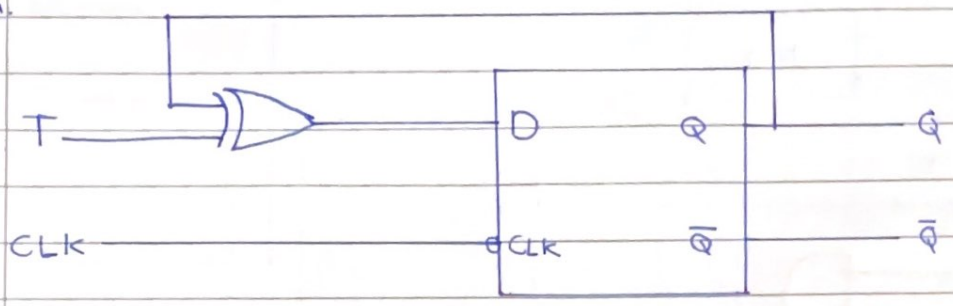
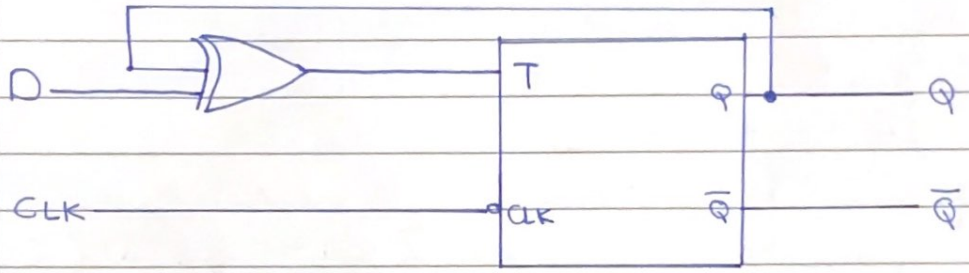
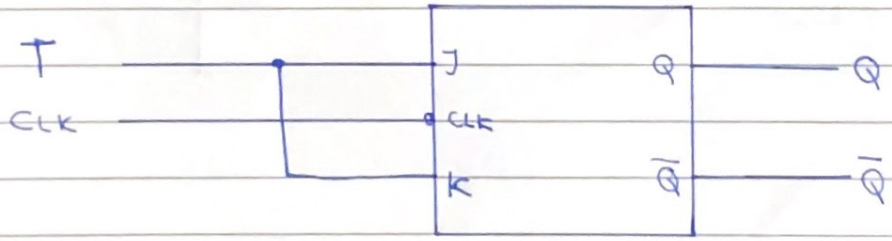
P4. a.


T
D
Q
Q
CLK
CLK
$\bar{Q}$
$\bar{Q}$

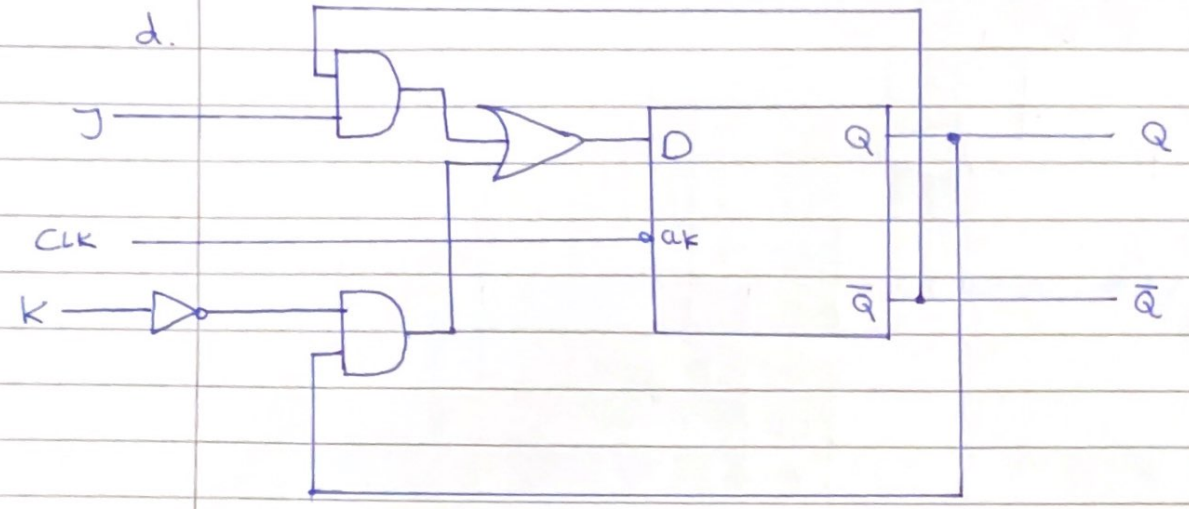
b.


D
T
Q
Q
CLK
CLK
$\bar{Q}$
$\bar{Q}$

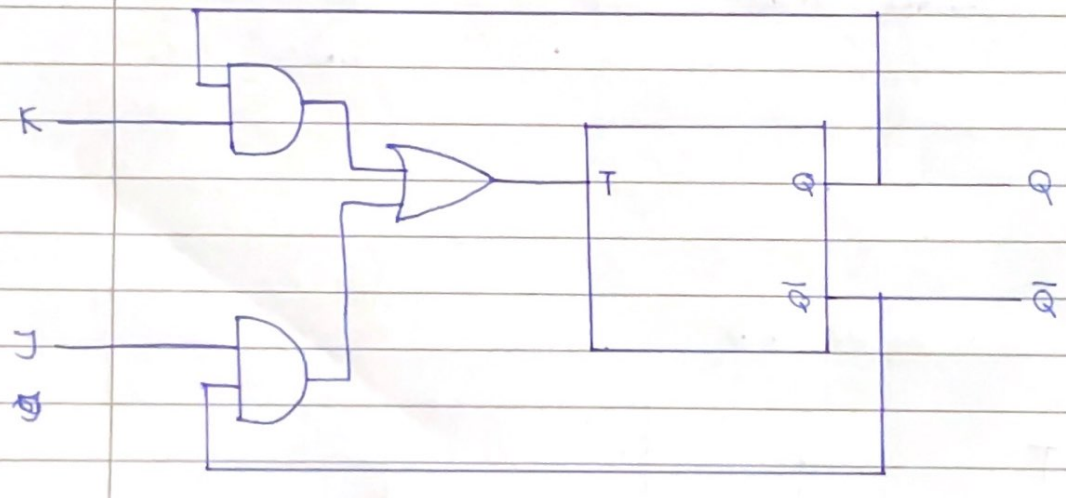
c.


T
CLK
J
CLK
K
Q
Q
$\bar{Q}$
$\bar{Q}$

d.



e.



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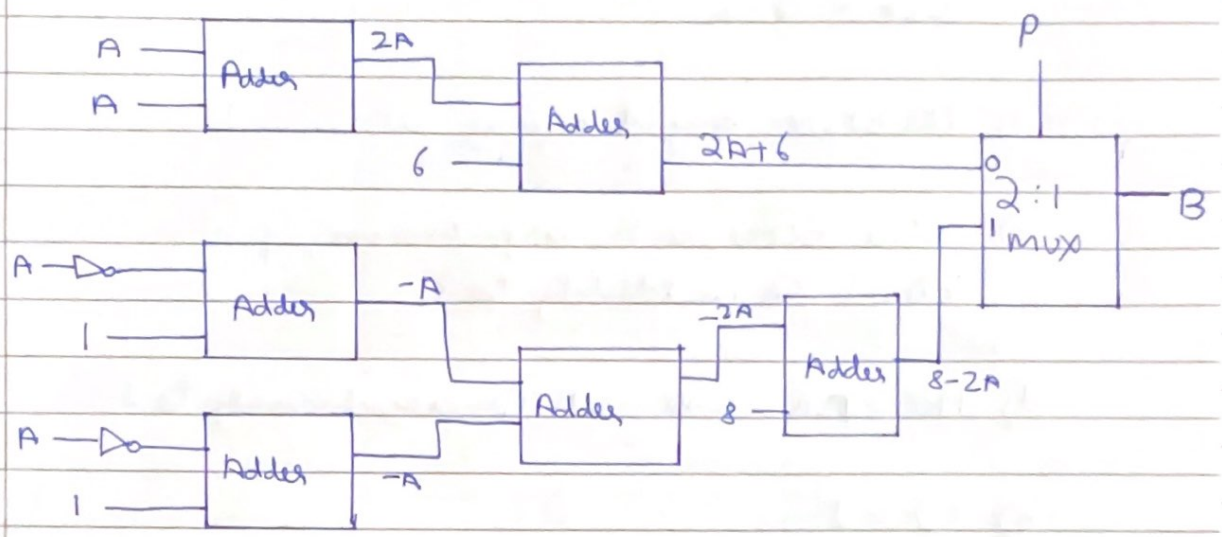
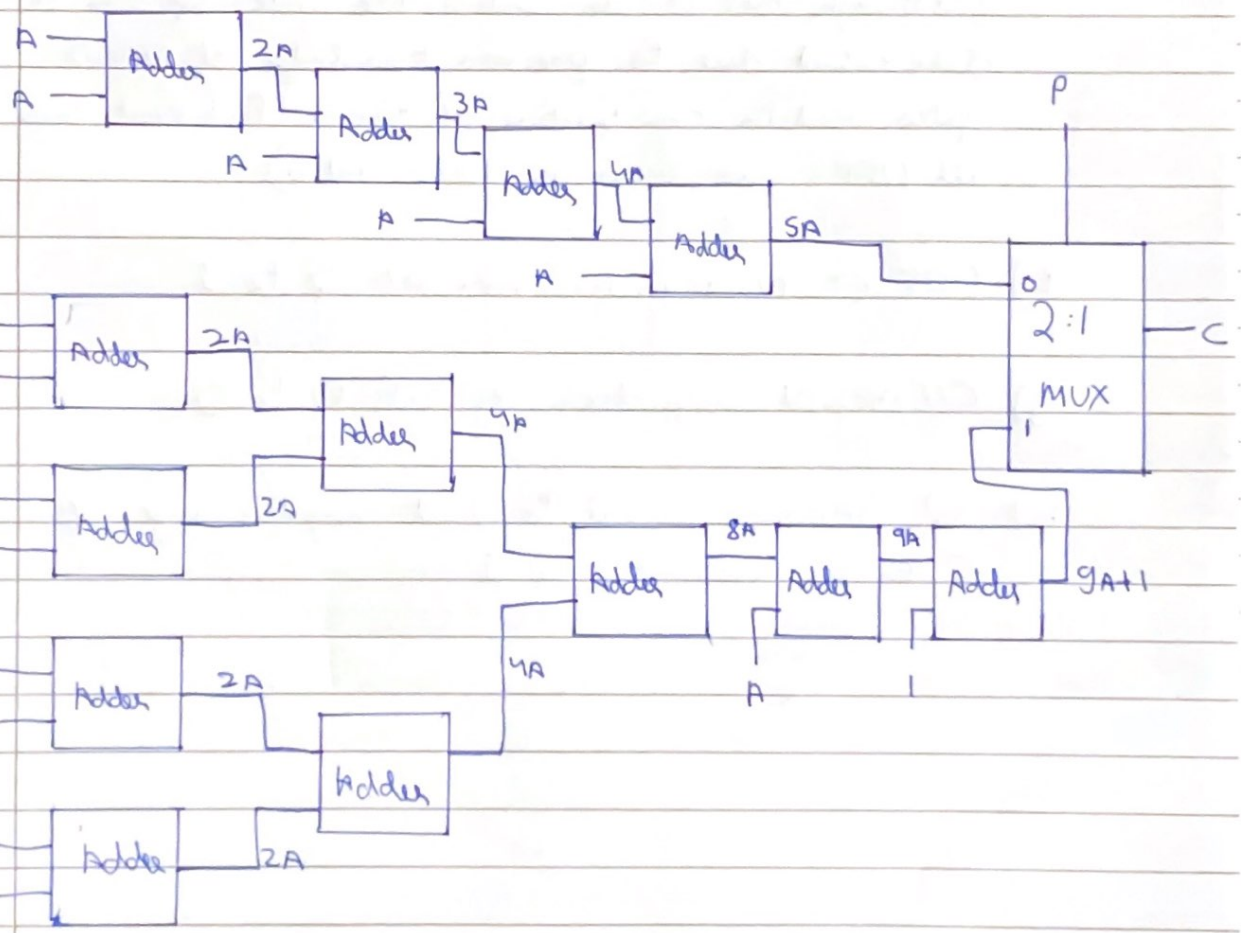
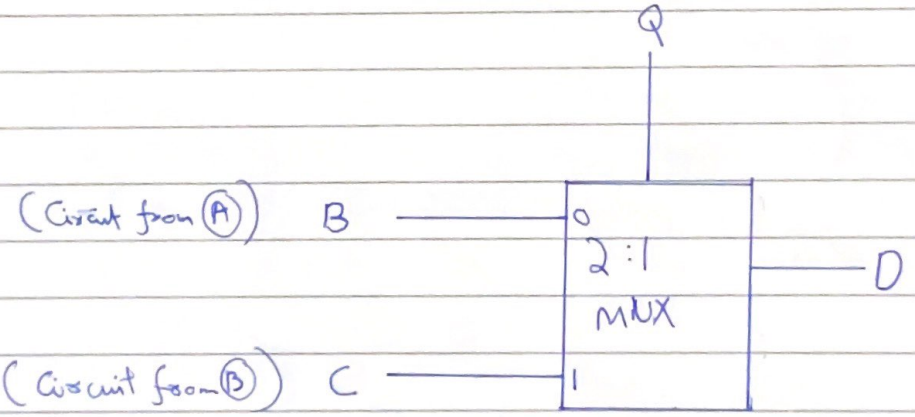
P5. A. We can use 2:1 MUX where selection line is P



B.



C.



P6. a) Q becomes equal to D on the negative edge of CLK → Q = 1

b) PRESET_N asynchronously sets Q to 1.

c) Since CLEAR_N is asynchronous, pulsing CLEAR_N clears Q immediately to 0.

d) PRESET_N will set Q asynchronously to 1.

e) Q = 1.
Although this is an undesirable state, Q can be determined due to previous knowledge of NAND gates used in construction of this DFF. (Not true for all DFF's as some use NOR Gates)

f) PRESET_N asynchronously sets Q to 1.

g) CLEAR_N asynchronously sets Q to 0.

h) Q becomes equal to D at negative edge of CLK as normal : Q = 1