ARYAN RAO

	ID: 264954748 /
	ID: 264954748 / LAB SECTION 11
	CPRE 281- HOMEWORK 1
P1.	A. ASIC: Application specific integrated discuit (ASIC) is an
	integrated chip customised for pasticular use sather than general purpose.
X	Reader A VIII
	B. ASCII; Alphanmeric information like letters & numbers typed
	code for this information is ASCII.
	code for this information in ASCII.
	C. FPGA: Most common type of Progres amnable Logic Device (PLD) is
	FPGA with billions of teransisters & supports implementation
	of complex digital systems
	The state of the s
	D. VHDL: Verilog Hardware Description Language is a hardway of
	description after und by designers of digital ASIC's.
02 r	
P2.	Pactotype implementation is mary expensive as a large number
	of evaces discovered in the texting stage late in
	developmental process are introduced at beginning of process as requirement essess Massoner, fixing these essess in
	as requirement essays Massones, fixing these essays in
	lesting is 10 times more expensive it they had been
	tand earlier.
R	The state of the s
	They can be avoided but with certain penalties:
	Exhaustive testing may not be performed.
	- Exhaustive testing may not be performed. - Proper Integration Test can't be performed if all pasts are wasting - - Bugs produced later may go untexted.
	- Bugs produced later may go untested

13. A. 10101102 = 1x2 + 0 + 1x2 + 0 + 1x2 + 1x2 + 0

D. 149,6=14162+4x16+9x16° = 256 + 64 + 9 = 329,6 2

E. ACDC16 = 10x16+12x16+13x16+12x16° = 40960 + 3072 + 208 + 12 = 44252,0

= 64 + 16 + 4 + 2

B. 1011, = 1/2 + 0 + 1/2 + 1/2°

= 8 + 2 + 1

C. 1750= 1882 + 7884 588°

= 64 + 56 + 5

= 86,01 = 0/85

= 1011112

B.
$$241_{10} =$$

$$241/2 = 120 \rightarrow 1$$

$$120/2 = 60 \rightarrow 0$$

$$60/2 = 130 + 3 + 0$$

$$30/2 = 15 \rightarrow 0$$

$$15/2 = 7 \rightarrow 1$$

1/2= 0 > 1200

= 111100012



