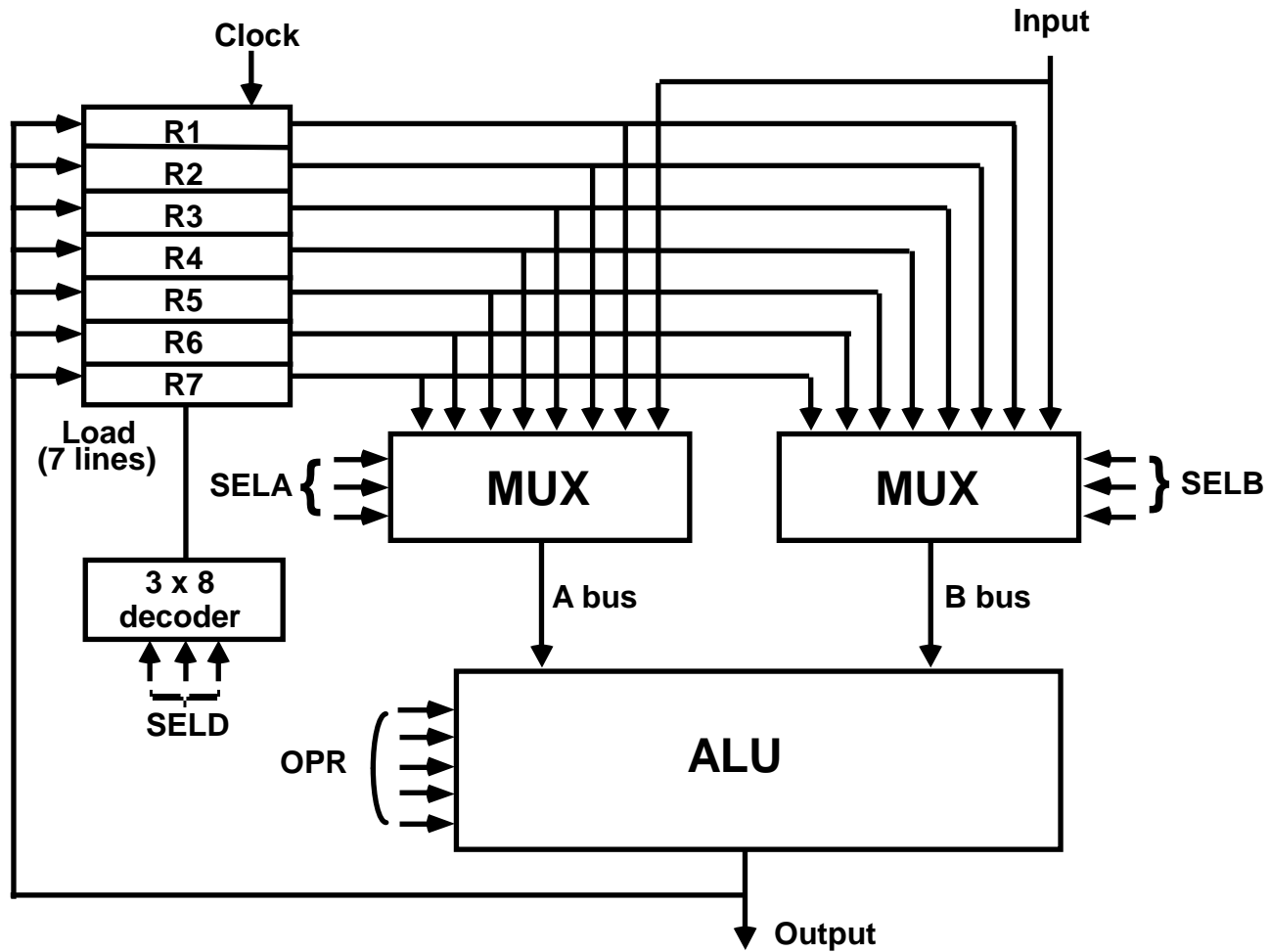


GENERAL REGISTER ORGANIZATION



OPERATION OF CONTROL UNIT

The control unit directs the information flow through ALU by:

- Selecting various *Components* in the system
- Selecting the *Function* of ALU

Example: $R1 \leftarrow R2 + R3$

[1] MUX A selector (SELA): $BUS\ A \leftarrow R2$

[2] MUX B selector (SELB): $BUS\ B \leftarrow R3$

[3] ALU operation selector (OPR): ALU to ADD

[4] Decoder destination selector (SELD): $R1 \leftarrow Out\ Bus$

| | | | | |
|--------------|------|------|------|-----|
| Control Word | 3 | 3 | 3 | 5 |
| | SELA | SELB | SELD | OPR |

Encoding of register selection fields

| Binary Code | SELA | SELB | SELD |
|-------------|-------|-------|------|
| 000 | Input | Input | None |
| 001 | R1 | R1 | R1 |
| 010 | R2 | R2 | R2 |
| 011 | R3 | R3 | R3 |
| 100 | R4 | R4 | R4 |
| 101 | R5 | R5 | R5 |
| 110 | R6 | R6 | R6 |
| 111 | R7 | R7 | R7 |

2

ALU CONTROL

Encoding of ALU operations

| OPR Select | Operation | Symbol |
|------------|----------------|--------|
| 00000 | Transfer A | TSFA |
| 00001 | Increment A | INCA |
| 00010 | ADD A + B | ADD |
| 00101 | Subtract A - B | SUB |
| 00110 | Decrement A | DECA |
| 01000 | AND A and B | AND |
| 01010 | OR A and B | OR |
| 01100 | XOR A and B | XOR |
| 01110 | Complement A | COMA |
| 10000 | Shift right A | SHRA |
| 11000 | Shift left A | SHLA |

Examples of ALU Microoperations

| Microoperation | Symbolic Designation | | | | Control Word |
|---|----------------------|------|------|------|-------------------|
| | SELA | SELB | SELD | OPR | |
| $R1 \leftarrow R2 - R3$ | R2 | R3 | R1 | SUB | 010 011 001 00101 |
| $R4 \leftarrow R4 \vee R5$ | R4 | R5 | R4 | OR | 100 101 100 01010 |
| $R6 \leftarrow R6 + 1$ | R6 | - | R6 | INCA | 110 000 110 00001 |
| $R7 \leftarrow R1$ | R1 | - | R7 | TSFA | 001 000 111 00000 |
| $\text{Output} \leftarrow R2$ | R2 | - | None | TSFA | 010 000 000 00000 |
| $\text{Output} \leftarrow \text{Input}$ | Input | - | None | TSFA | 000 000 000 00000 |
| $R4 \leftarrow \text{shl } R4$ | R4 | - | R4 | SHLA | 100 000 100 11000 |
| $R5 \leftarrow 0$ | R5 | R5 | R5 | XOR | 101 101 101 01100 |

ALU CONTROL

Encoding of ALU operations

| OPR Select | Operation | Symbol |
|---------------|----------------|--------|
| 00000 | Transfer A | TSFA |
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| 10000 | Shift right A | SHRA |
| 11000 | Shift left A | SHLA |

Examples of ALU Microoperations

| Microoperation | Symbolic Designation | | | | Control Word |
|--------------------------------|----------------------|------|------|-----|--------------|
| | SELA | SELB | SELD | OPR | |
| $R1 \leftarrow R2 + R3$ | | | | | |
| $R4 \leftarrow R4$ | | | | | |
| $R5 \leftarrow R5 - 1$ | | | | | |
| $R6 \leftarrow \text{Shl } R1$ | | | | | |
| $R7 \leftarrow \text{Input}$ | | | | | |

ALU CONTROL

Encoding of ALU operations

| OPR Select | Operation | Symbol |
|---------------|----------------|--------|
| 00000 | Transfer A | TSFA |
| 00001 | Increment A | INCA |
| 00010 | ADD A + B | ADD |
| 00101 | Subtract A - B | SUB |
| 00110 | Decrement A | DECA |
| 01000 | AND A and B | AND |
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| 11000 | Shift left A | SHLA |

Examples of ALU Microoperations

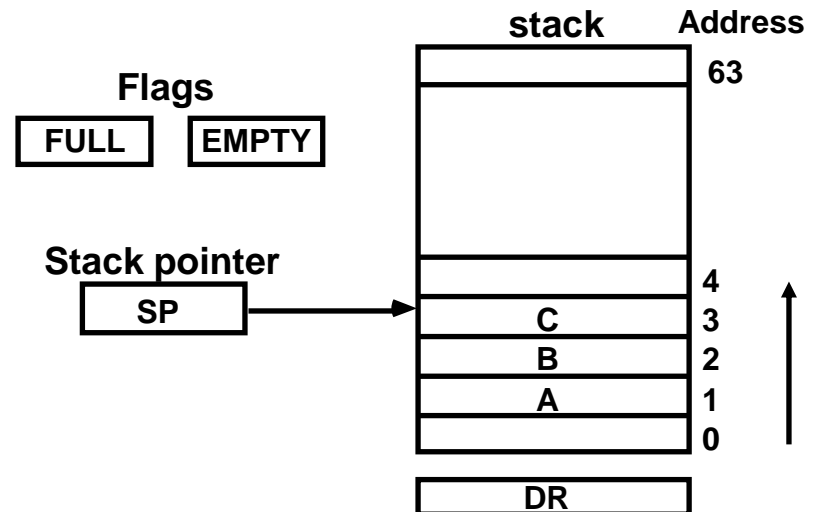
| Microoperation | Symbolic Designation | | | | Control Word |
|-------------------------------|----------------------|------|------|------|--------------|
| | SELA | SELB | SELD | OPR | |
| $R1 \leftarrow R2 + R3$ | R2 | R3 | R1 | ADD | |
| $R4 \leftarrow R4$ | R4 | - | R4 | TSFA | |
| $R5 \leftarrow R5 - 1$ | R5 | - | R5 | DECA | |
| $R7 \leftarrow R1$ | R1 | - | R7 | TSFA | |
| $\text{Output} \leftarrow R2$ | R2 | - | None | TSFA | |

STACK ORGANIZATION

Stack

- Efficient for arithmetic expression evaluation
- Storage which can be accessed in LIFO
- Pointer: SP
- Only PUSH and POP operations are applicable

Register Stack



Push, Pop operations

/ Initially, SP = 0, EMPTY = 1, FULL = 0 */*

PUSH

$SP \leftarrow SP + 1$

$M[SP] \leftarrow DR$

If $(SP = 0)$ then $(FULL \leftarrow 1)$

$EMPTY \leftarrow 0$

POP

$DR \leftarrow M[SP]$

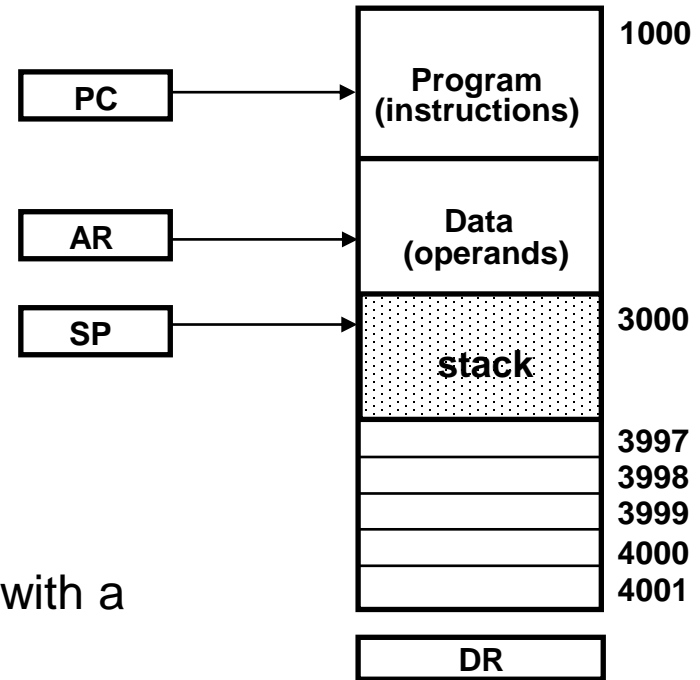
$SP \leftarrow SP - 1$

If $(SP = 0)$ then $(EMPTY \leftarrow 1)$

$FULL \leftarrow 0$

MEMORY STACK ORGANIZATION

Memory with Program, Data,
and Stack Segments



- A portion of memory is used as a stack with a processor register as a stack pointer

- PUSH: $SP \leftarrow SP - 1$
 $M[SP] \leftarrow DR$
- POP: $DR \leftarrow M[SP]$
 $SP \leftarrow SP + 1$

REVERSE POLISH NOTATION

Arithmetic Expressions: $A + B$

$A + B$ Infix notation

$+ A B$ Prefix or Polish notation

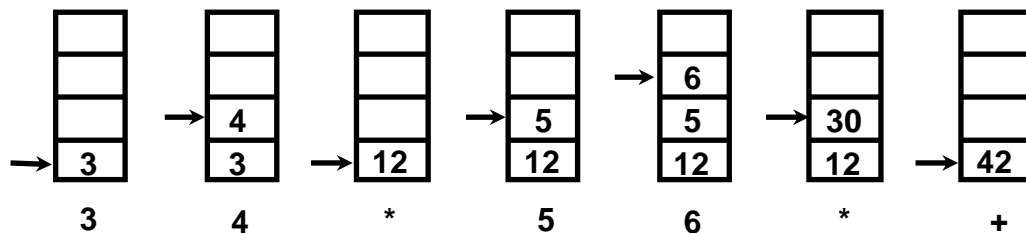
$A B +$ Postfix or reverse Polish notation

- The reverse Polish notation is very suitable for stack manipulation

Evaluation of Arithmetic Expressions

Any arithmetic expression can be expressed in parenthesis-free Polish notation, including reverse Polish notation

$$(3 * 4) + (5 * 6) \Rightarrow 3 4 * 5 6 * +$$



- Let $SP=000000$ in Fig1, then how many items are there in the stack if $FULL=1$ & $EMPTY=0$ & $FULL=0$ & $EMPTY=1$.
- A stack is organized such that SP can be initialized to 4000 in Fig. 2 and the first item in the stack is stored at location 4000. List the micro-operation for PUSH and POP operation.
- Convert the following arithmetic expressions in to reverse polish notation and show the stack operations for evaluating the numerical result:

$$(3+4) [10*(2+6)+8]$$