

DEPARTMENT OF ELECTRICAL ENGINEERING
Indian Institute of Technology, Indore



**EE 622 : Digital Circuit Design
Project -1**

**Implementation of 4x4 6T-SRAM Memory Array From
C-MOS TO GDSII
And RISC V Processor From RTL to GDSII**

PRESENTED BY:

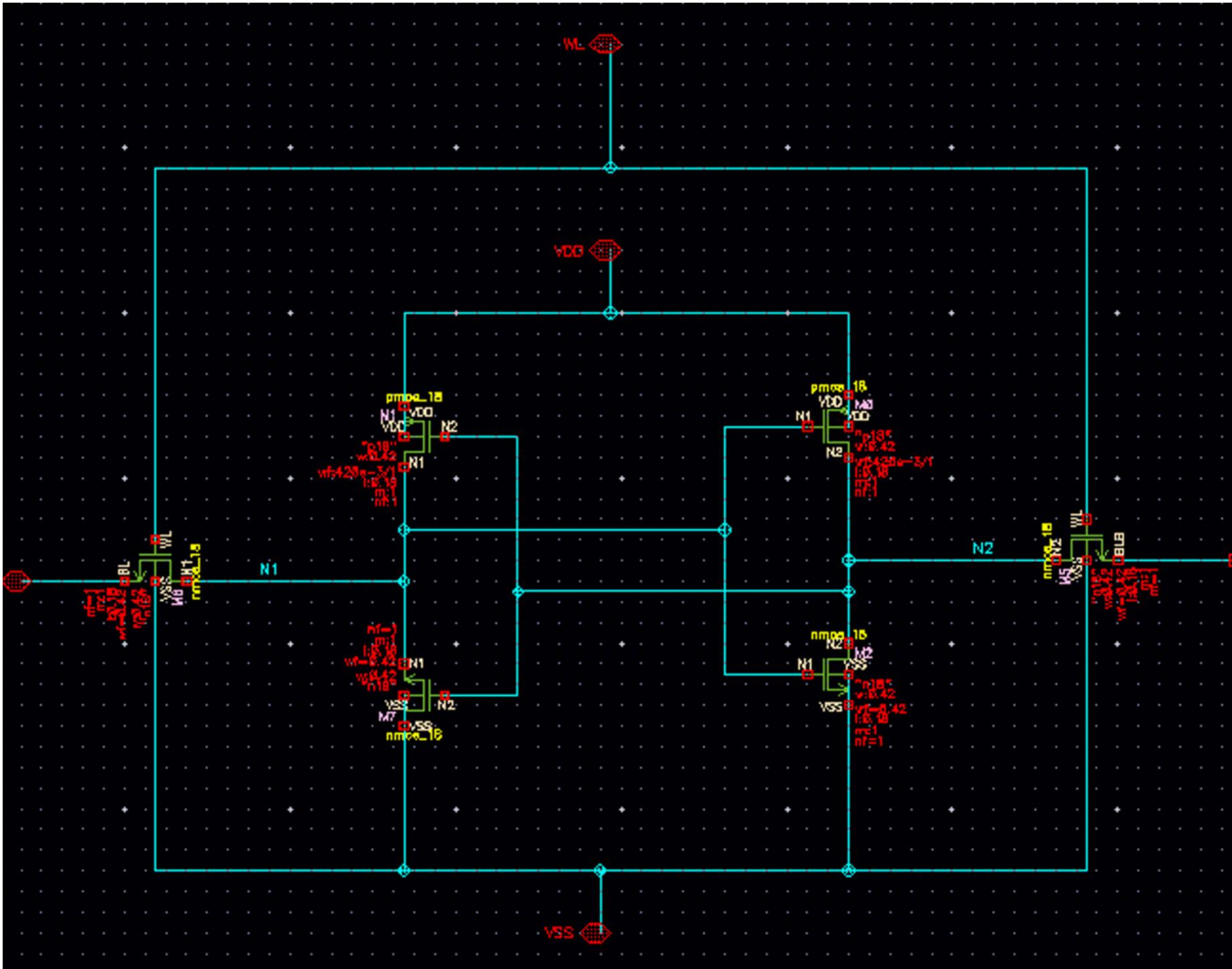
ARYAN TYAGI (mt2502102011)

COURSE COORDINATOR:

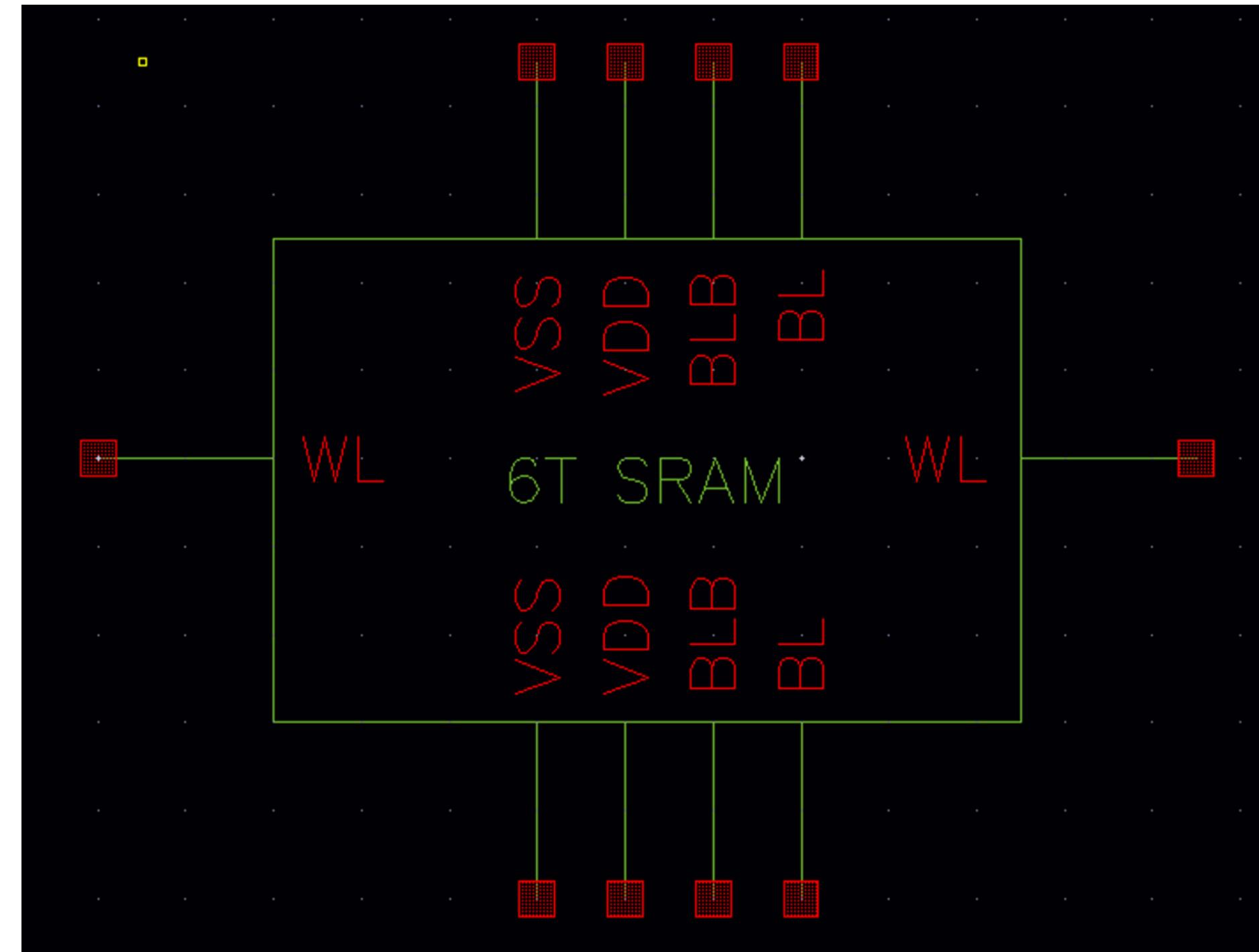
Prof. Santosh Kumar Vishwakarma

6T-SRAM

SCHEMATIC

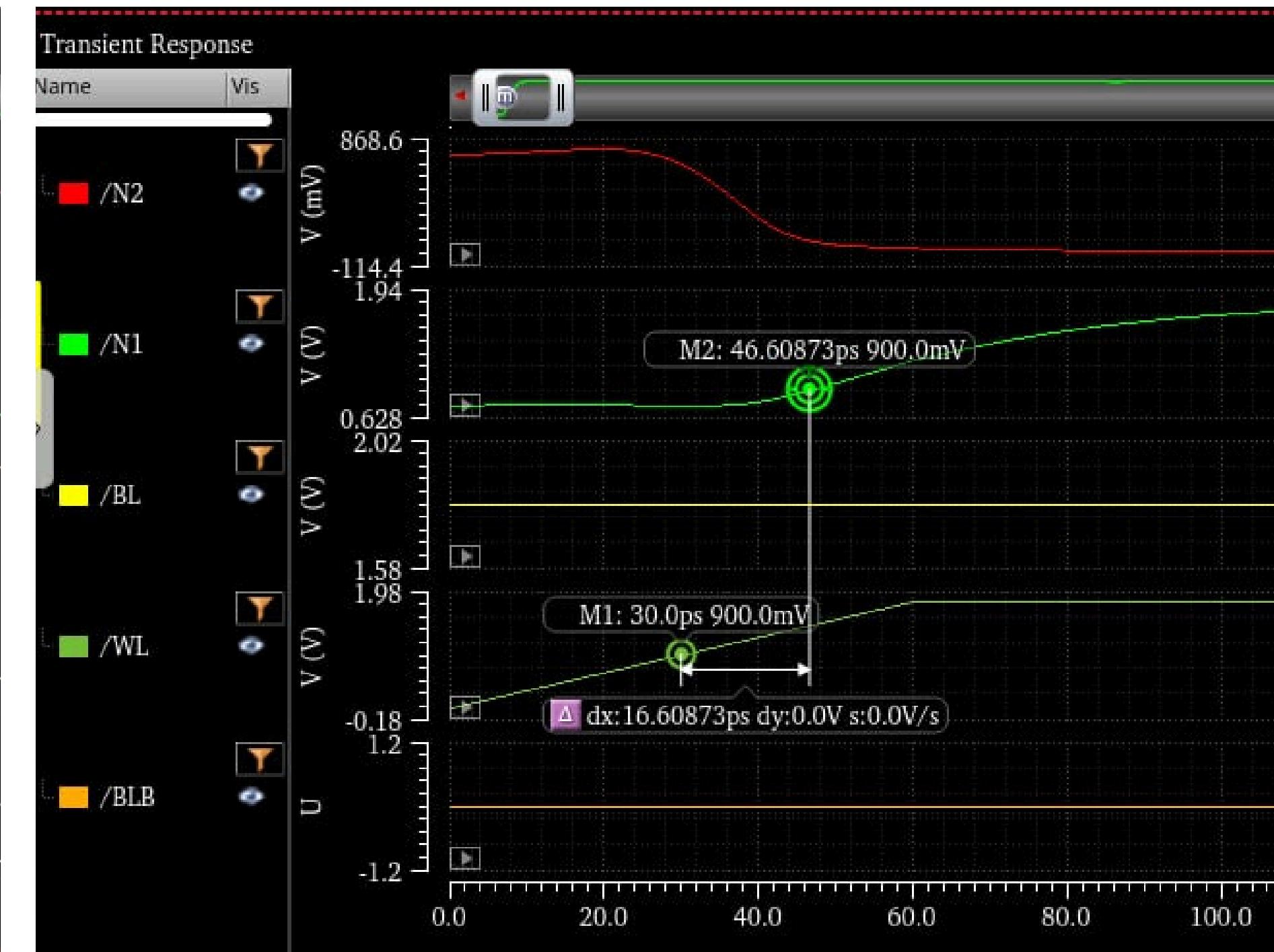
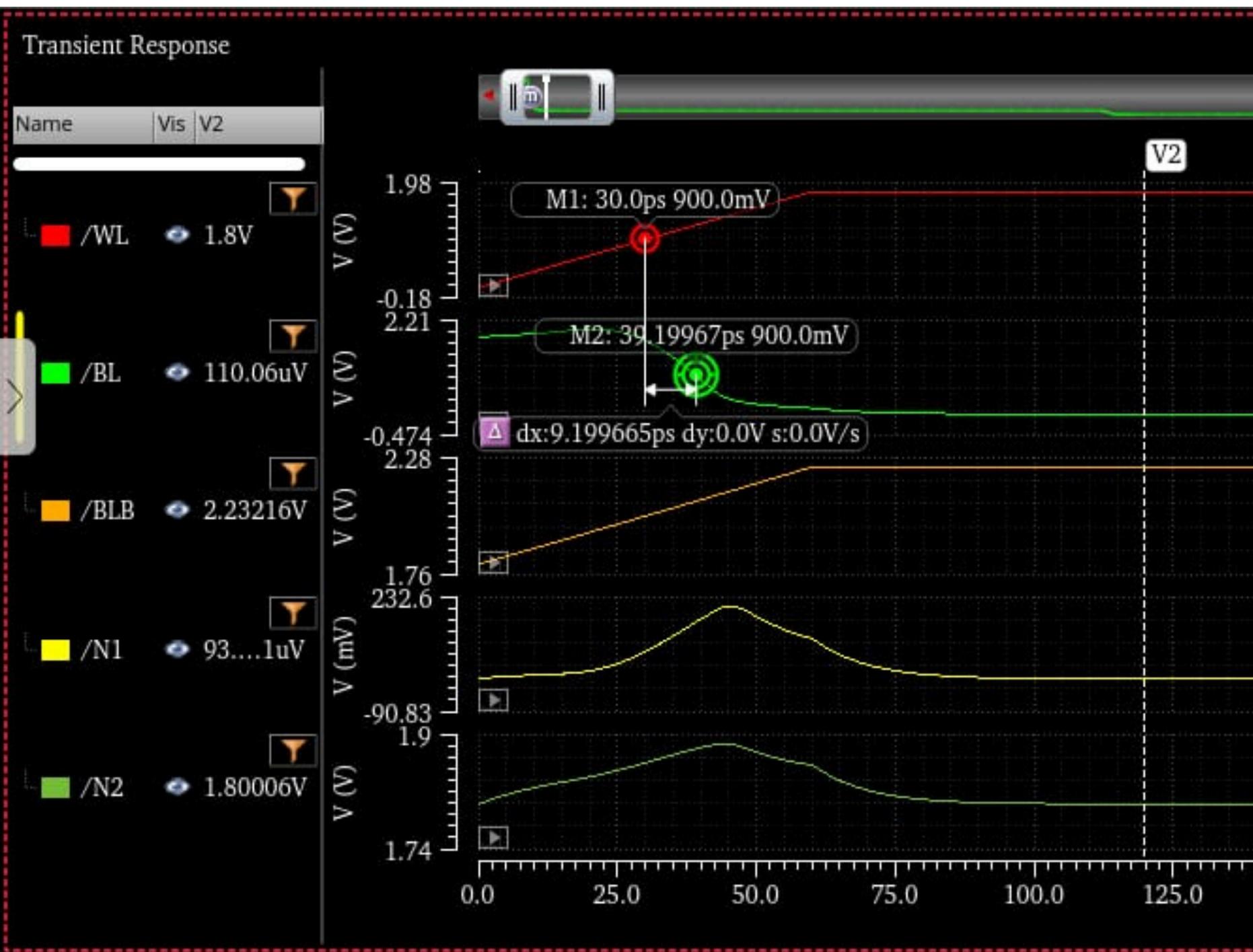


SYMBOL



6T-SRAM GRAPH

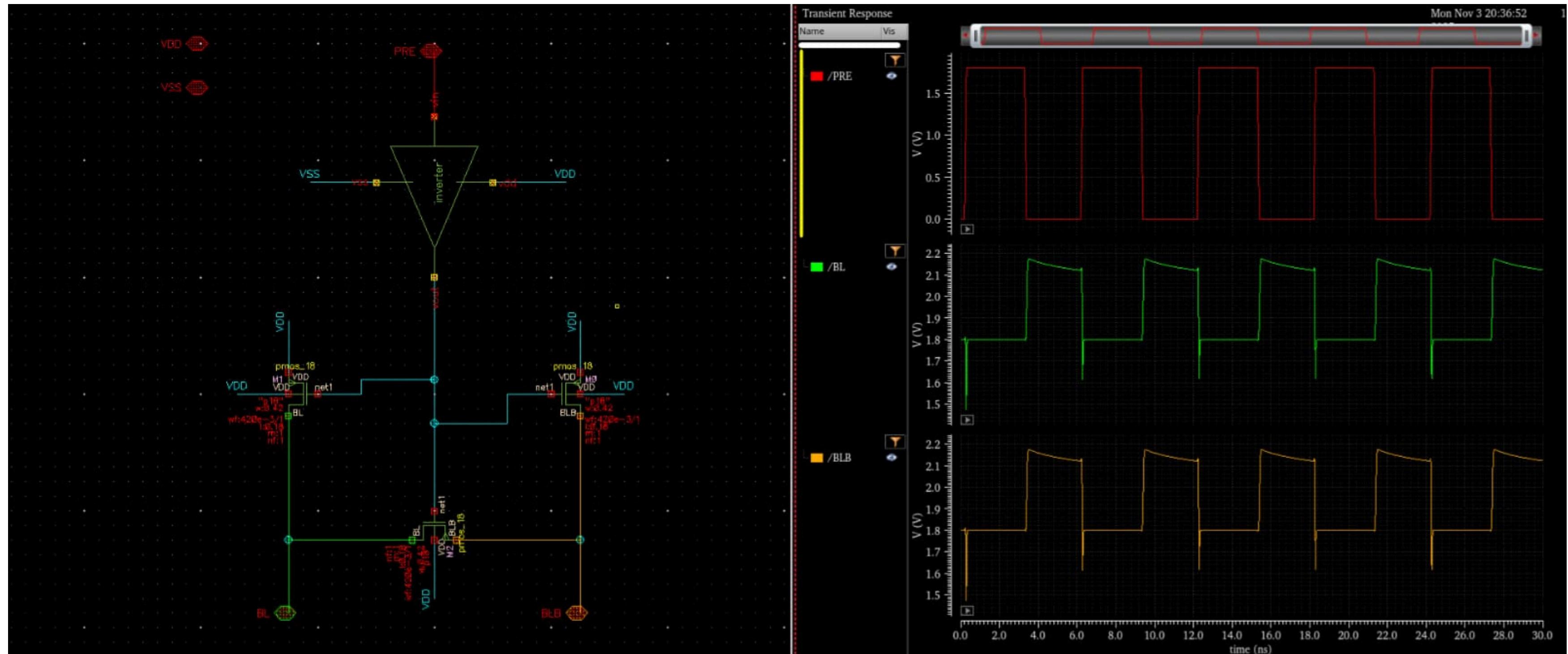
READ



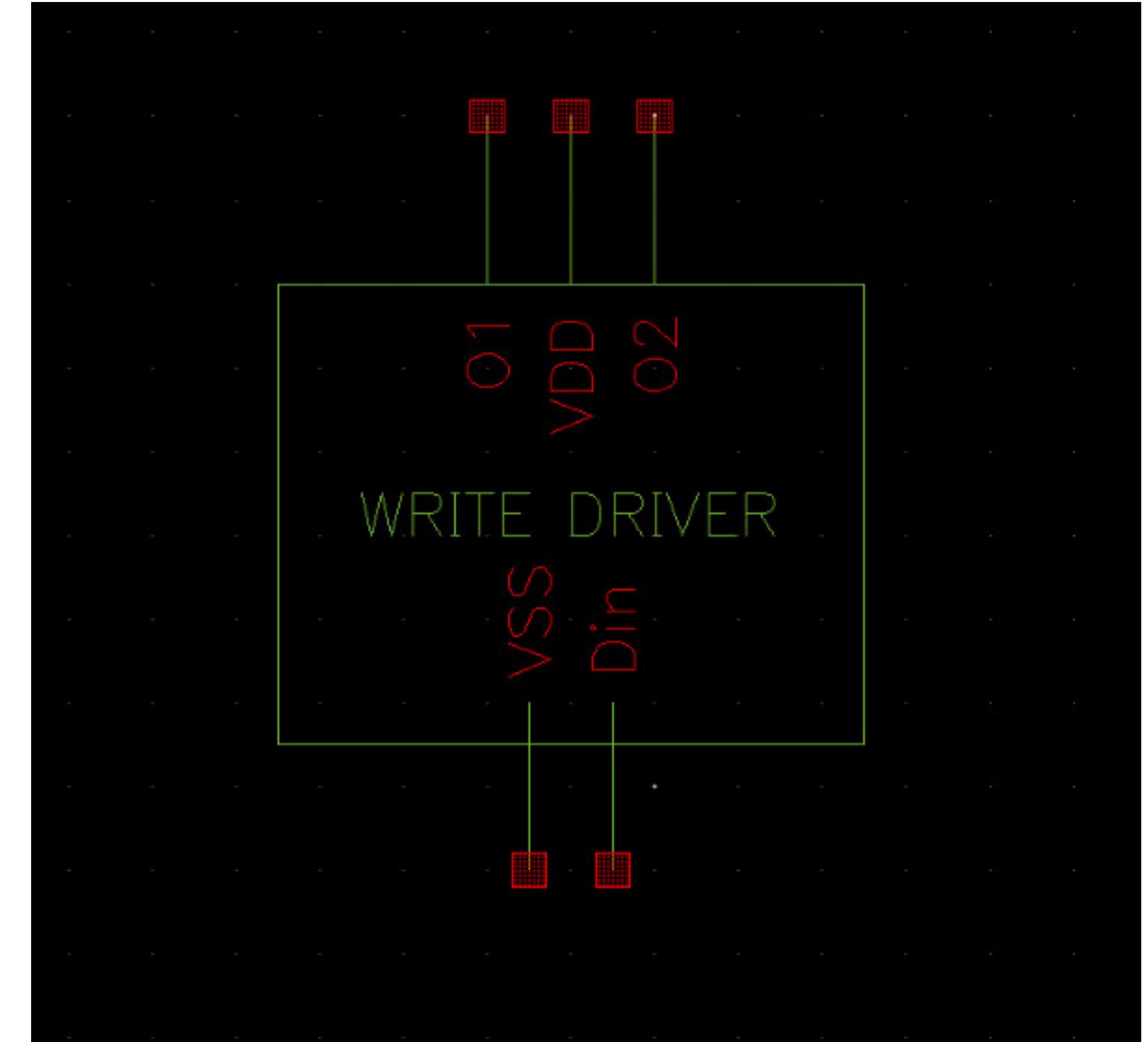
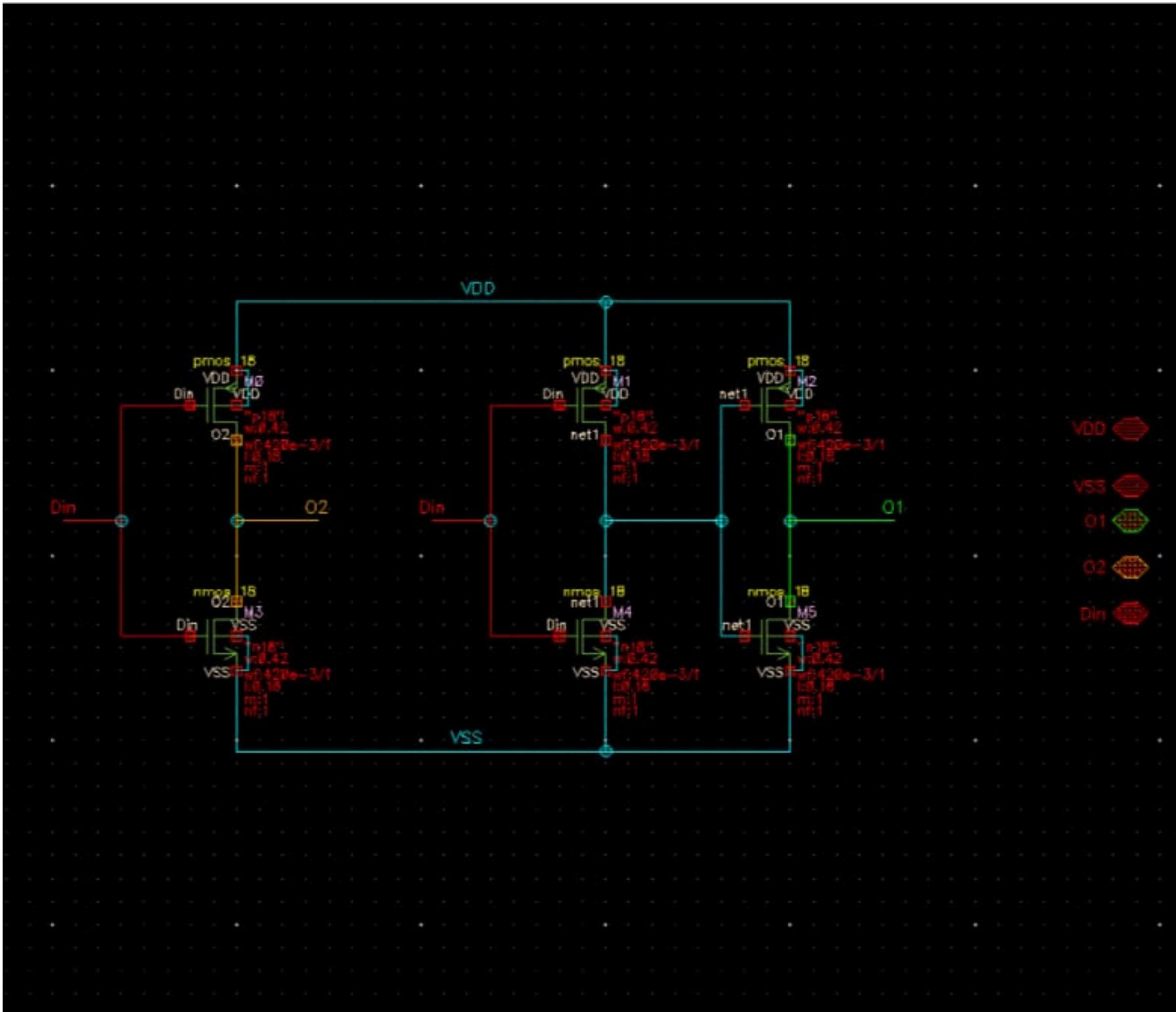
PERIPHERAL CIRCUIT LIST

- Precharge
- Write Driver
- Sense Amplifier
- IO
- Row Decoder

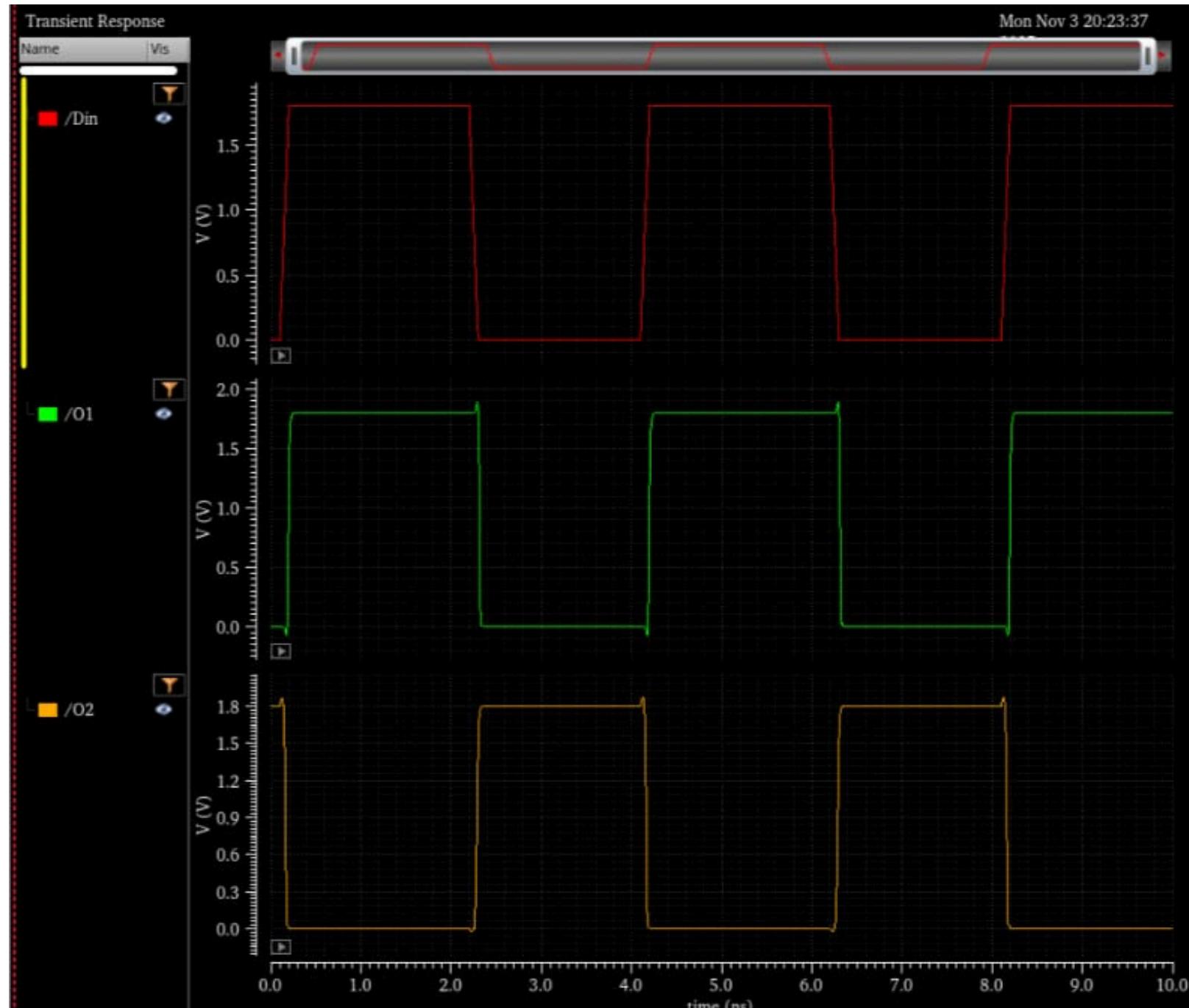
PRE CHARGE



WRITE DRIVER

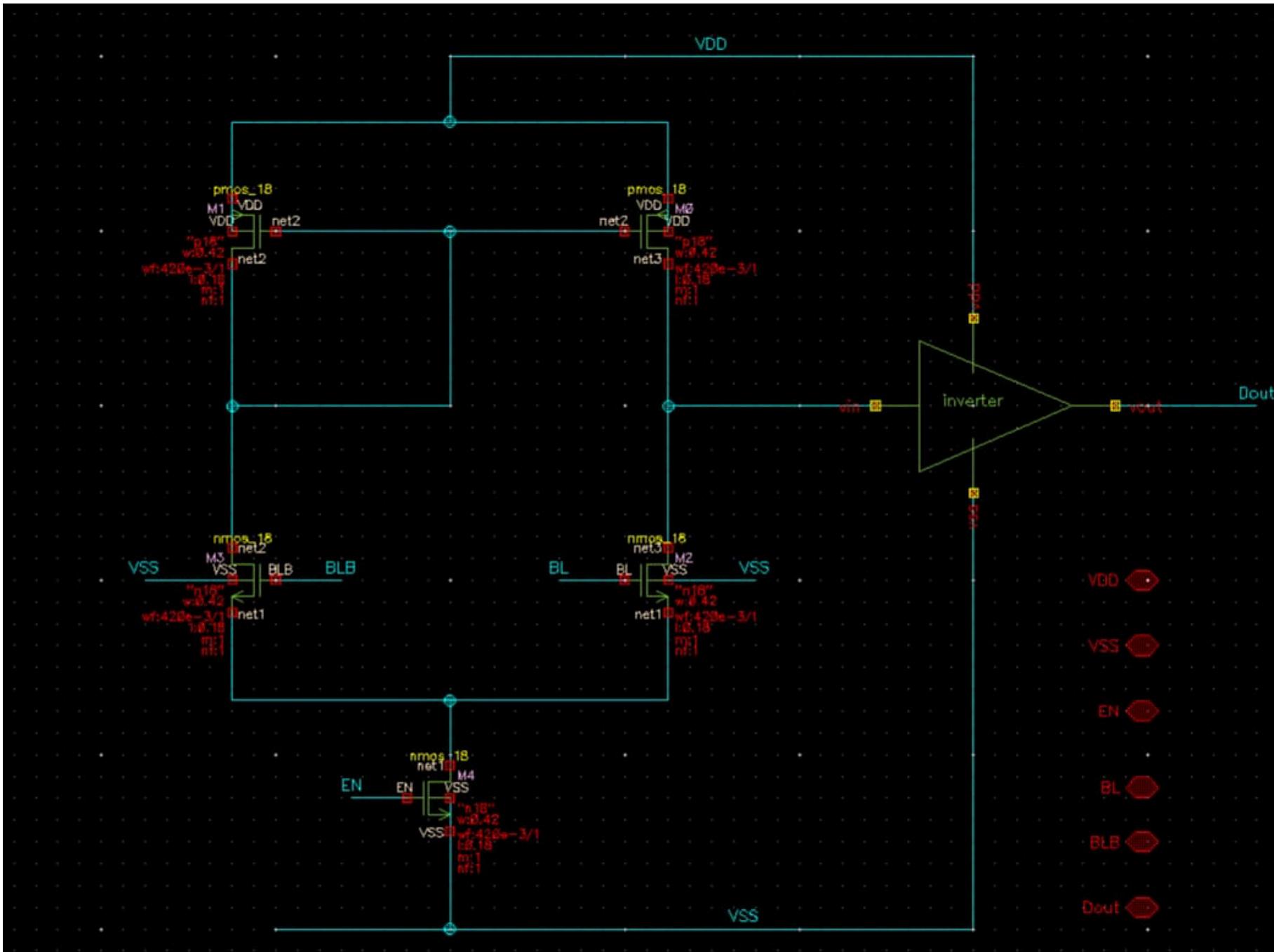


WRITE DRIVER SIMULATION

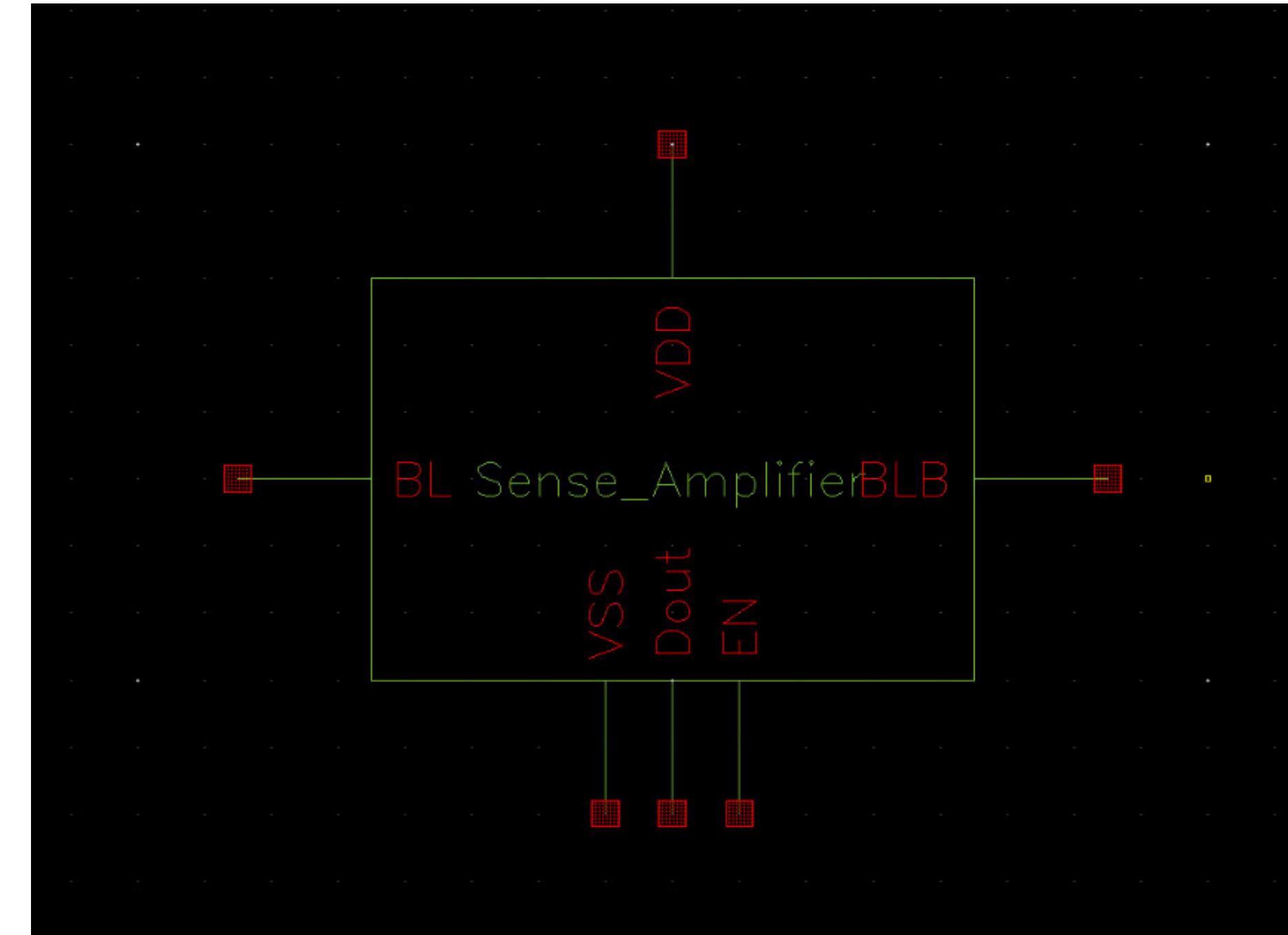


SENSE AMPLIFIER

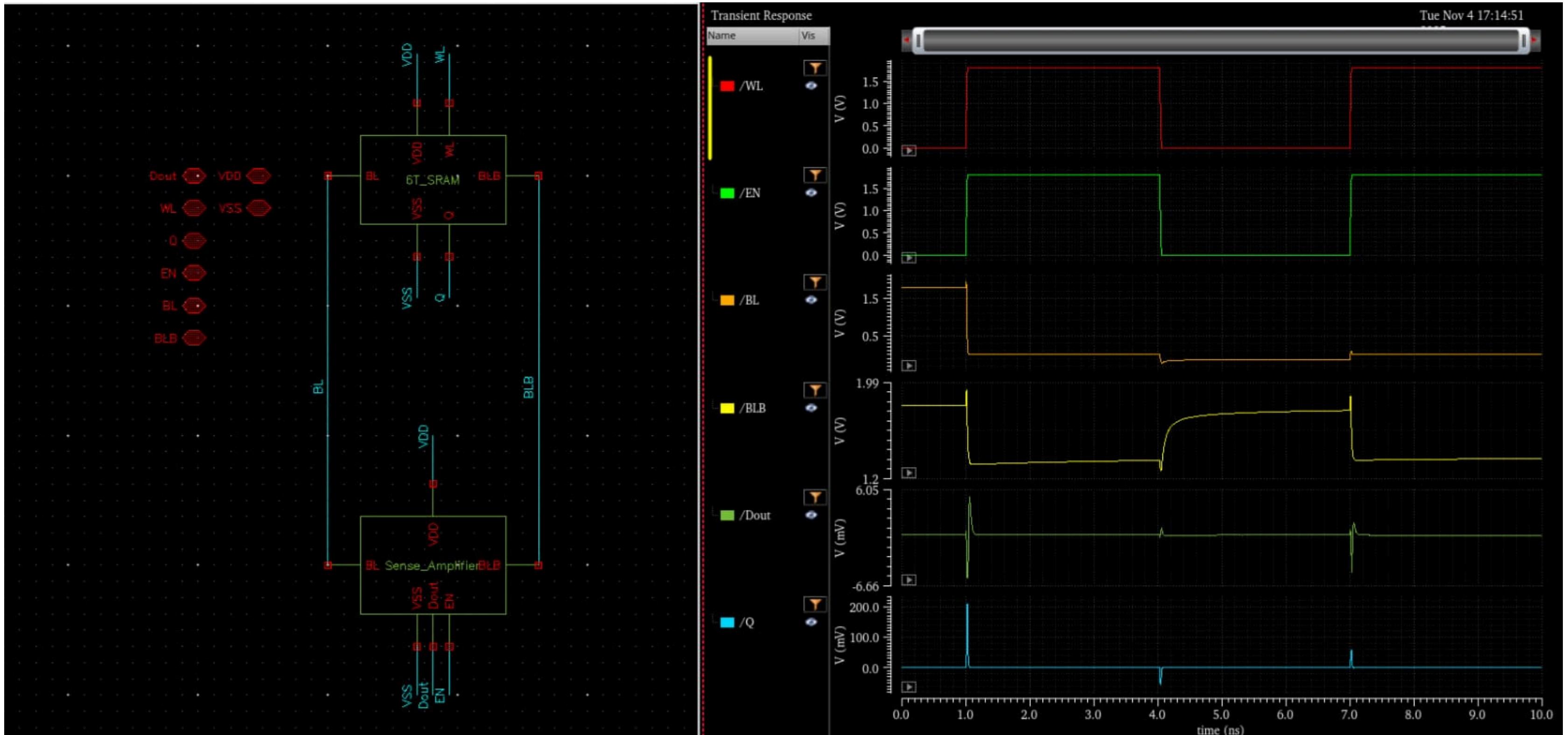
Schematic



Symbol

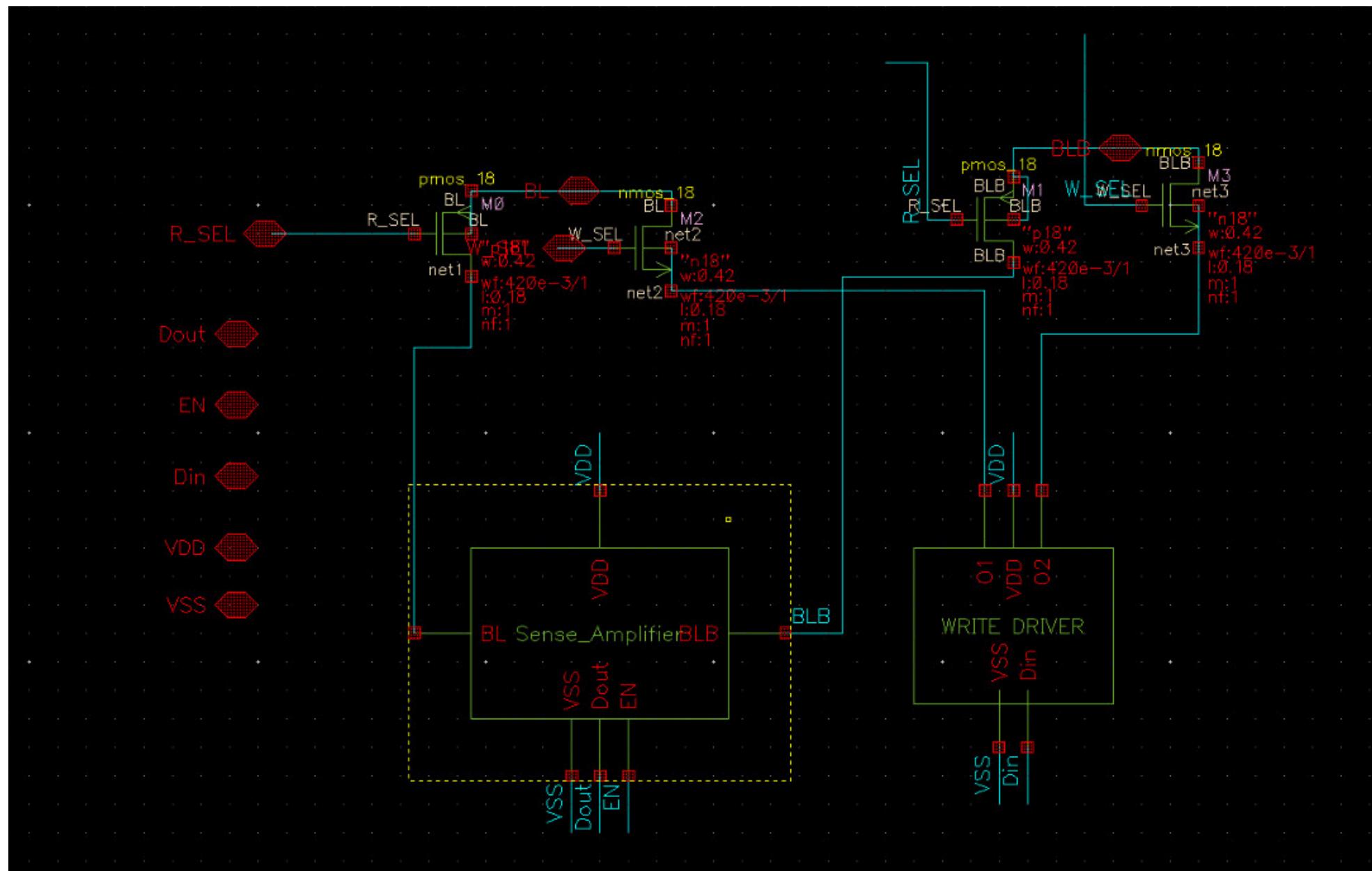


TEST BENCH & SIMULATION

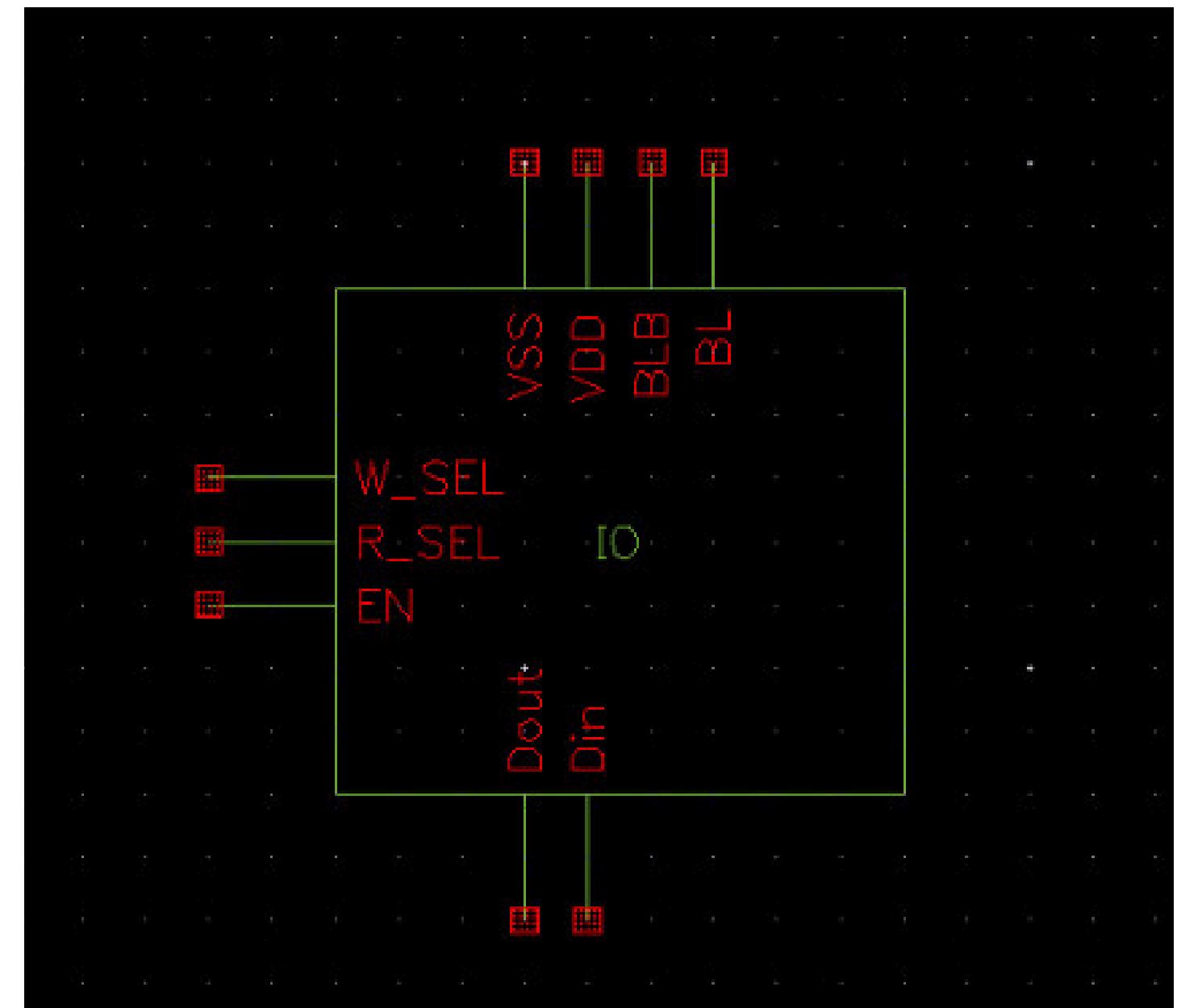


IO DEVICE

Schematic

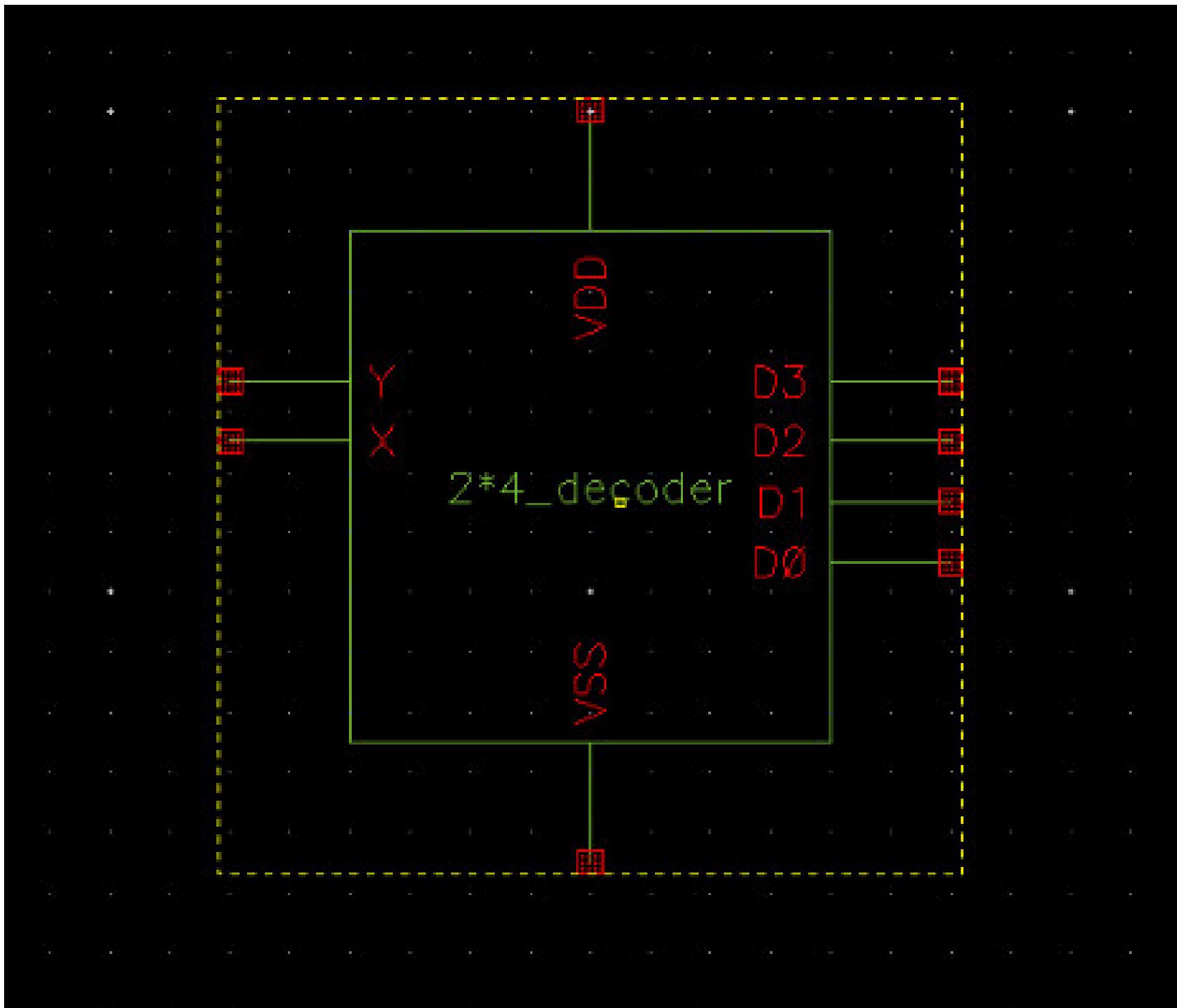


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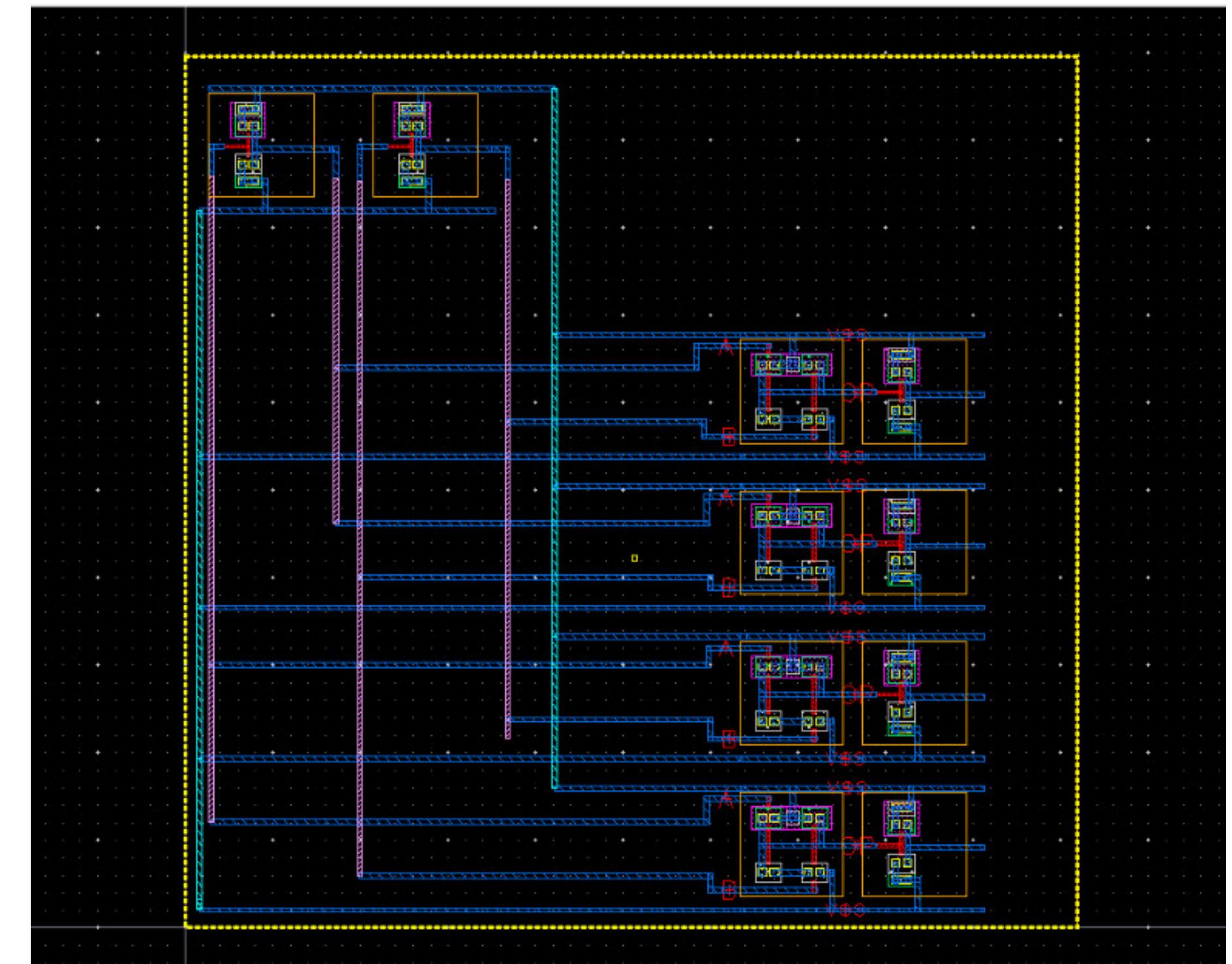


ROW DECODER

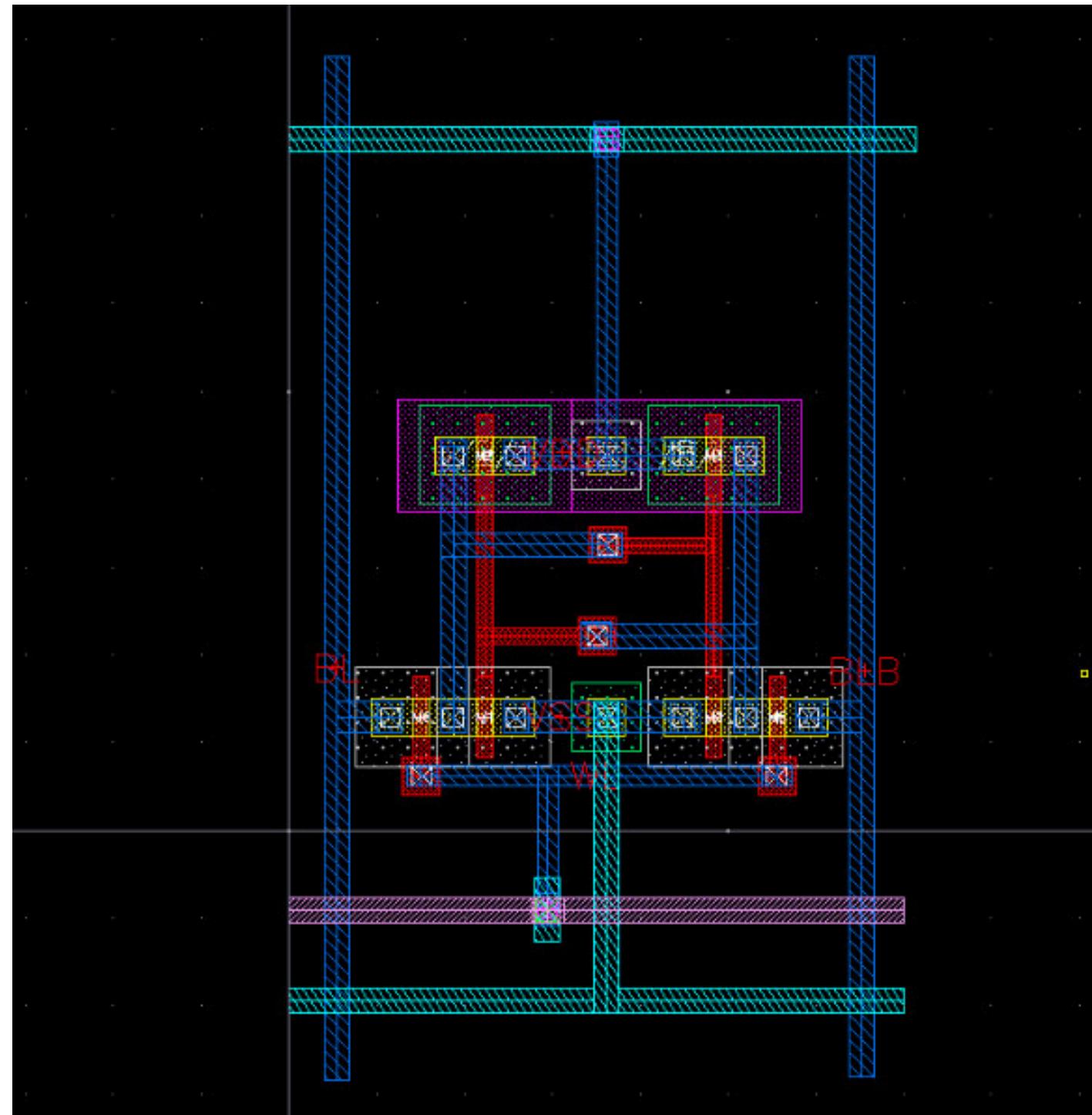
SYMBOL



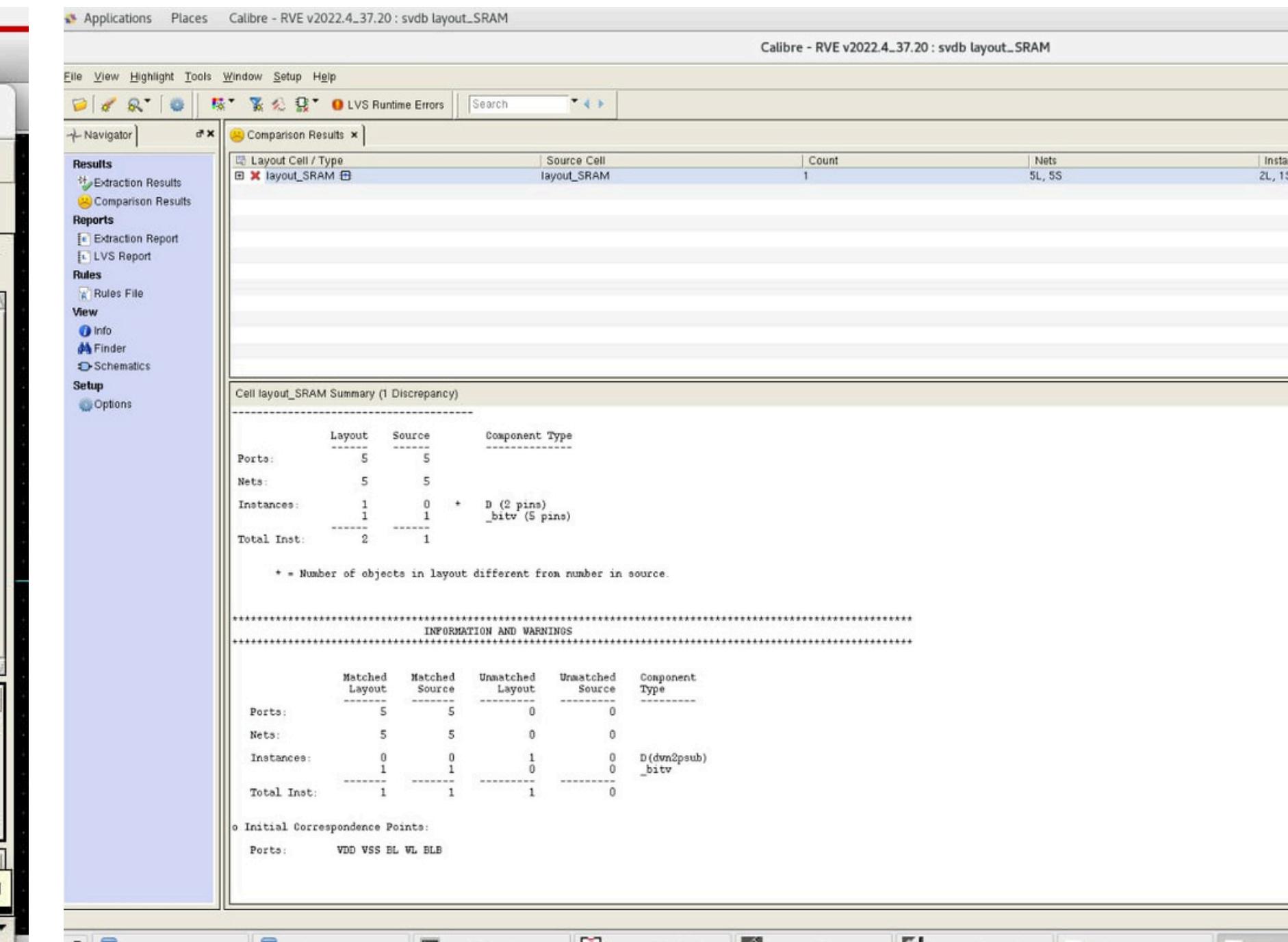
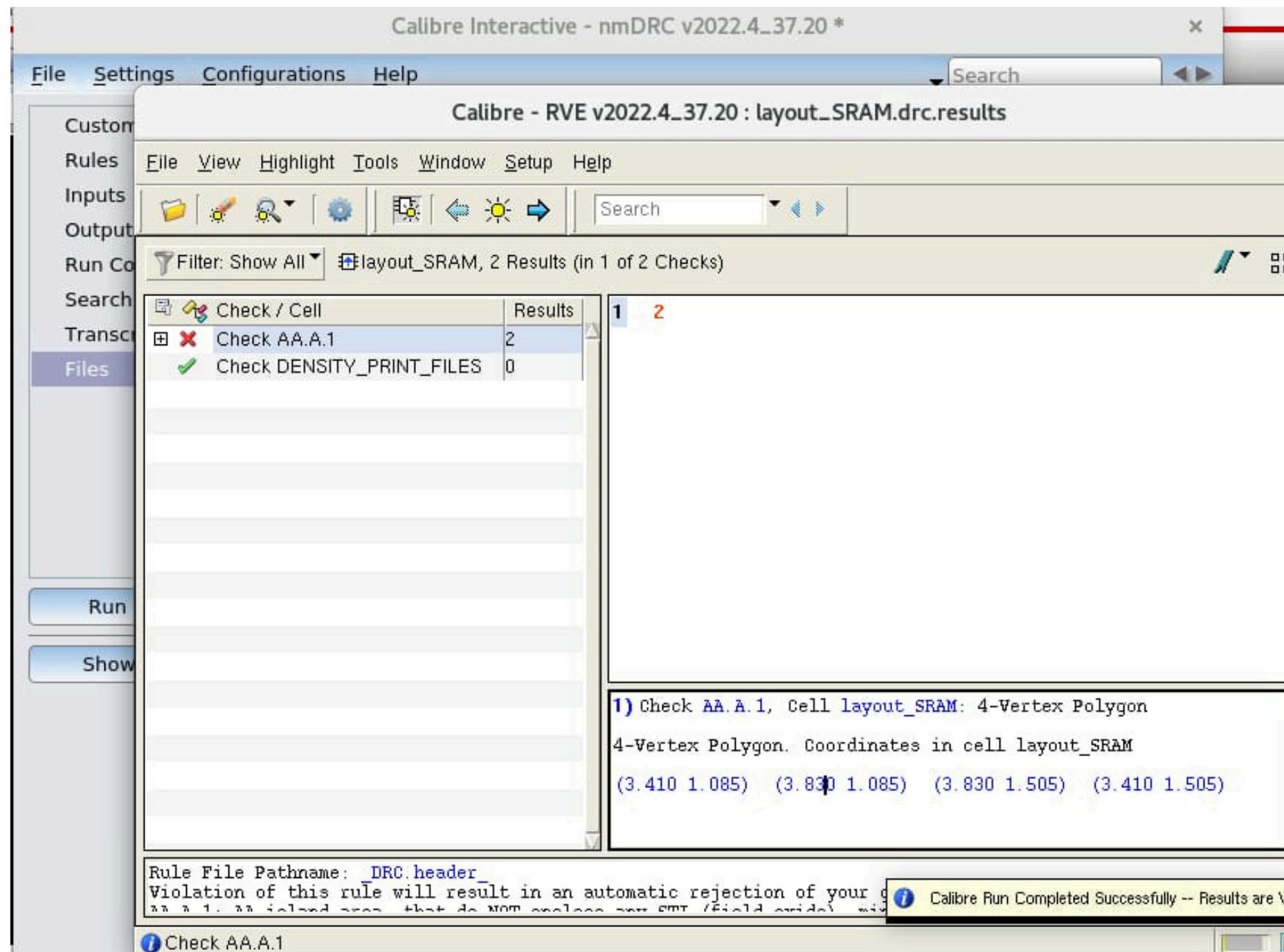
LAYOUT



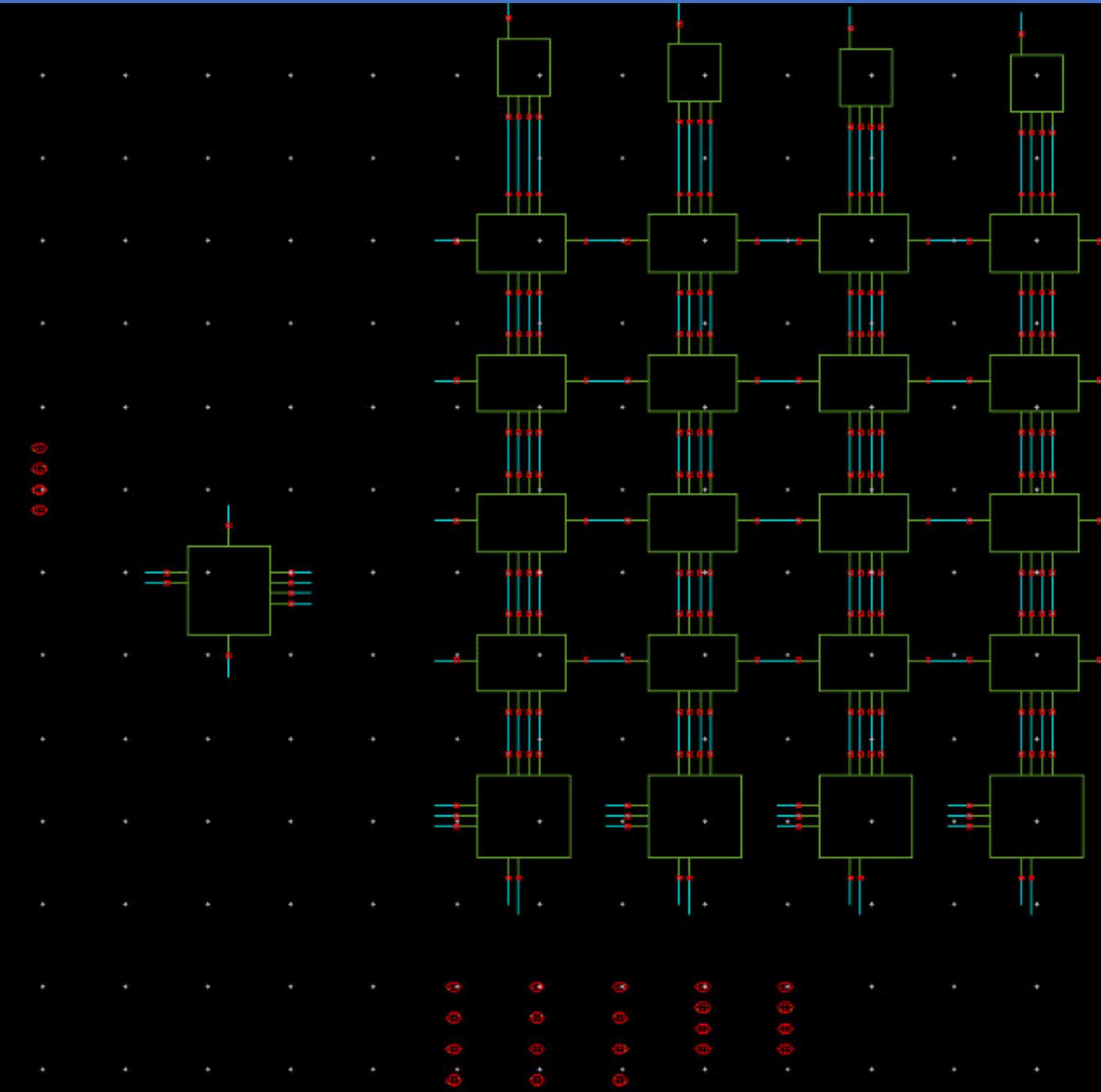
6T-SRAM LAYOUT



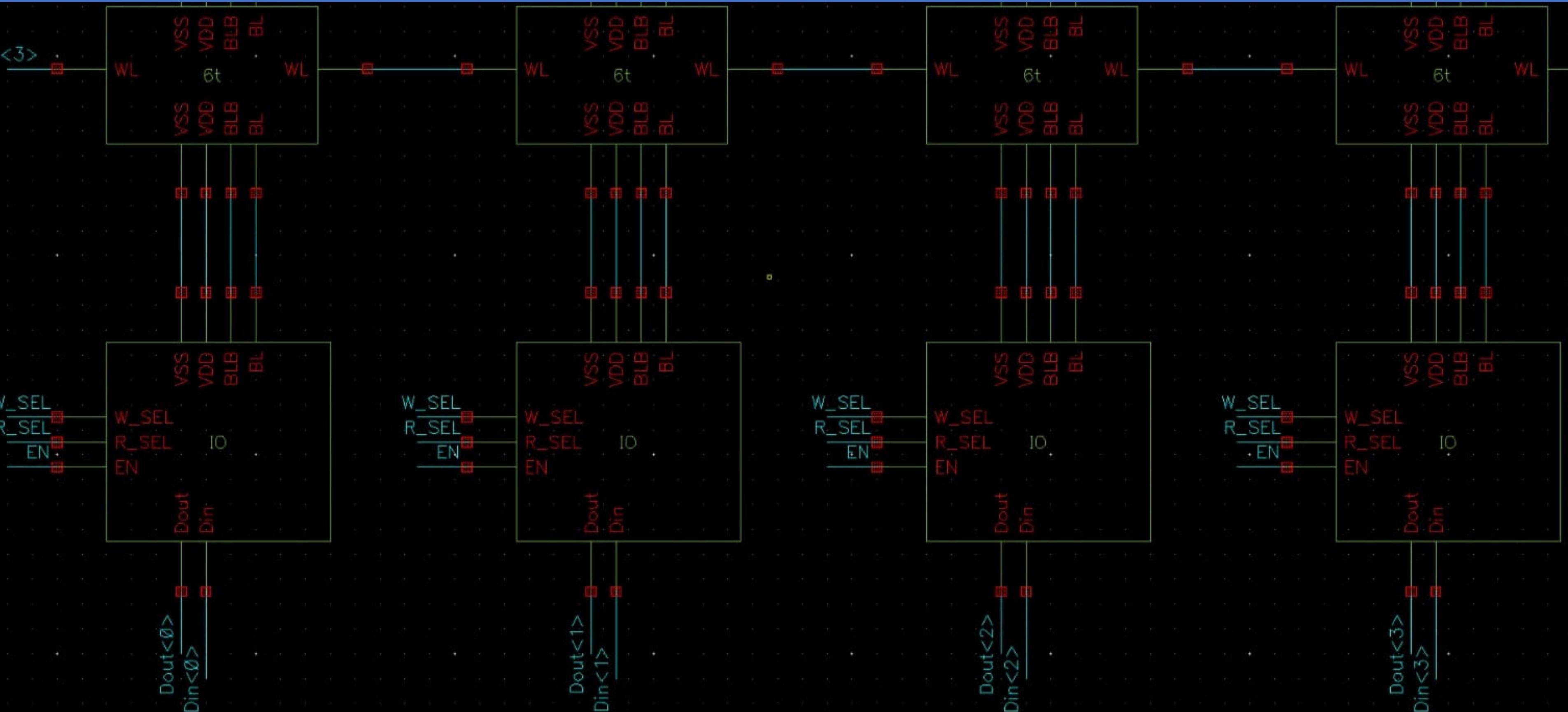
LVS AND DRC



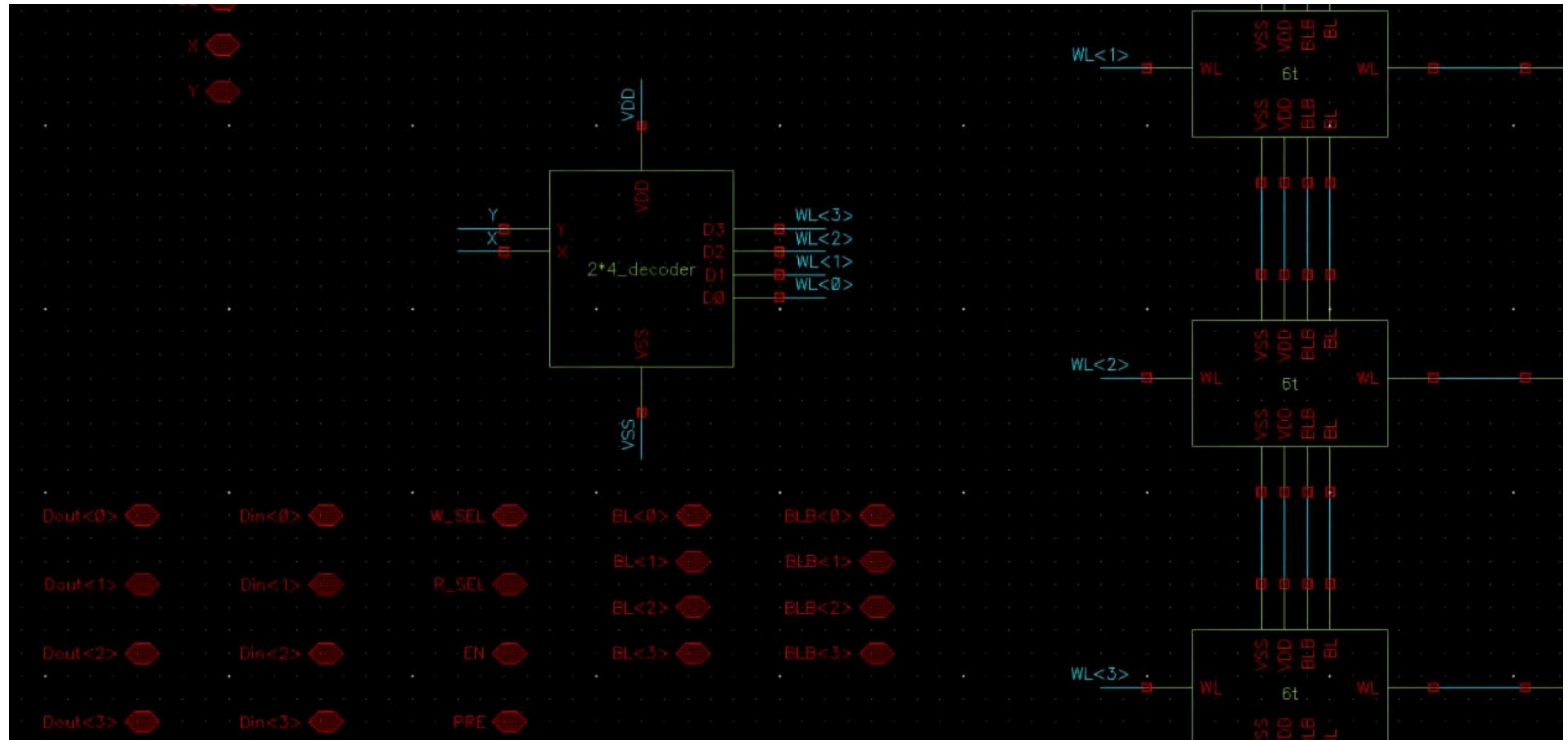
4X4 ARRAY



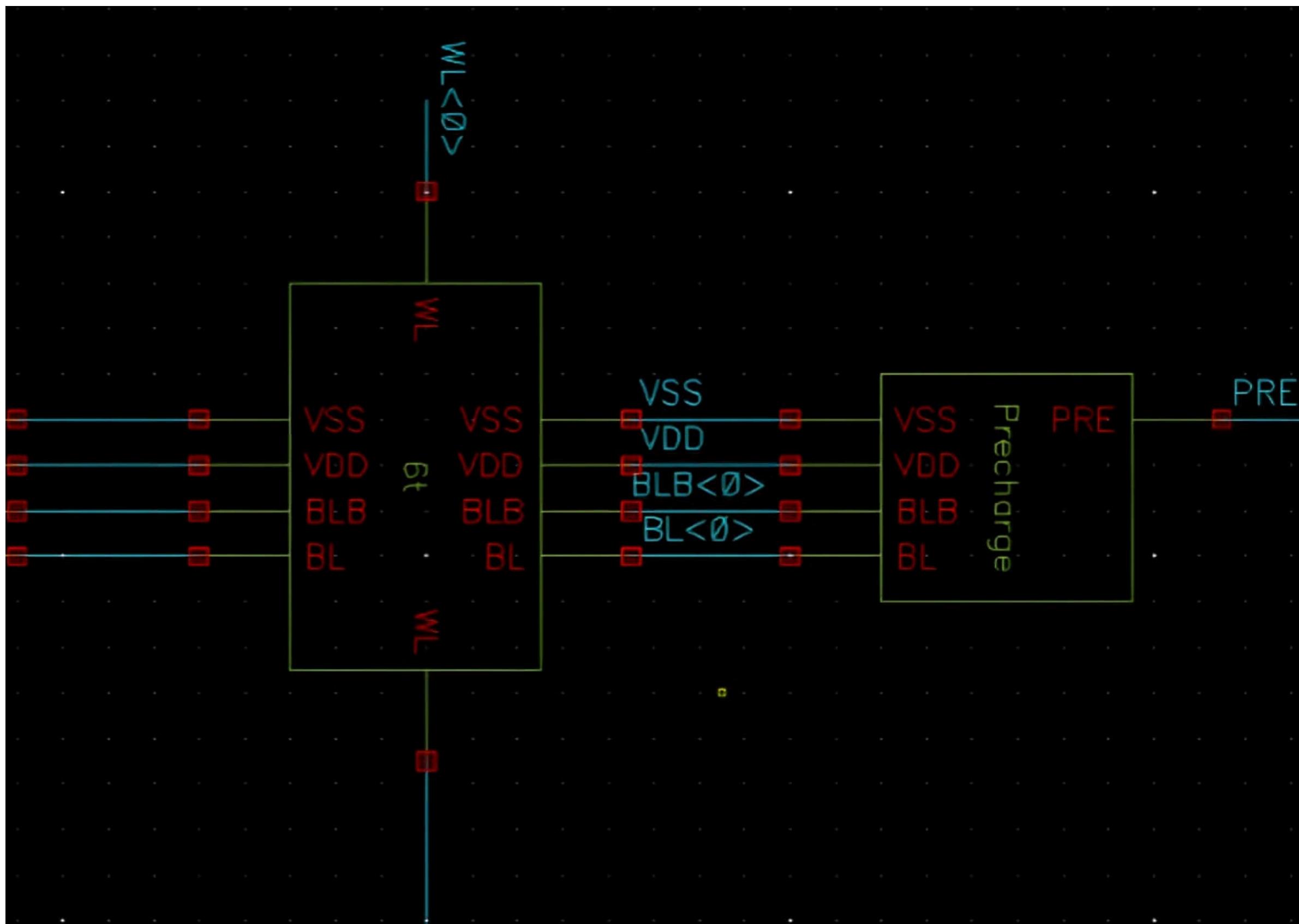
RAM ARRAY TO IO INTERFACE

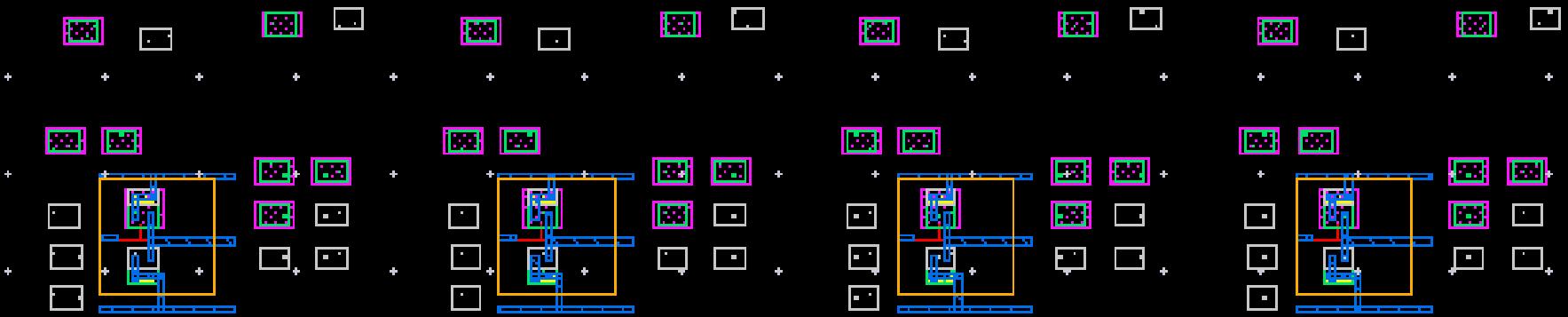
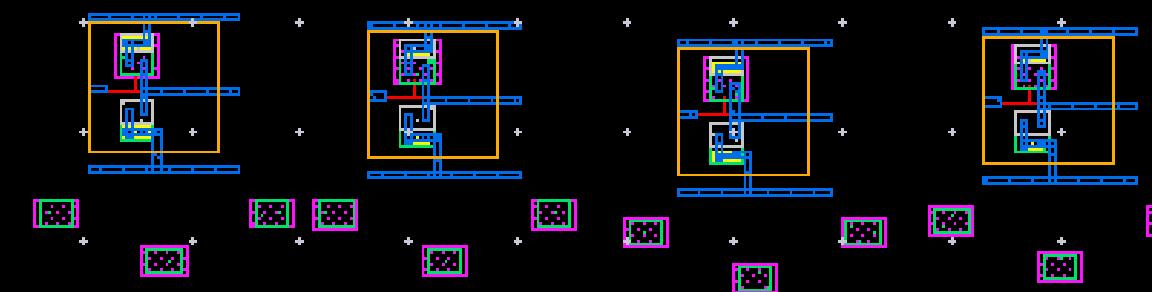
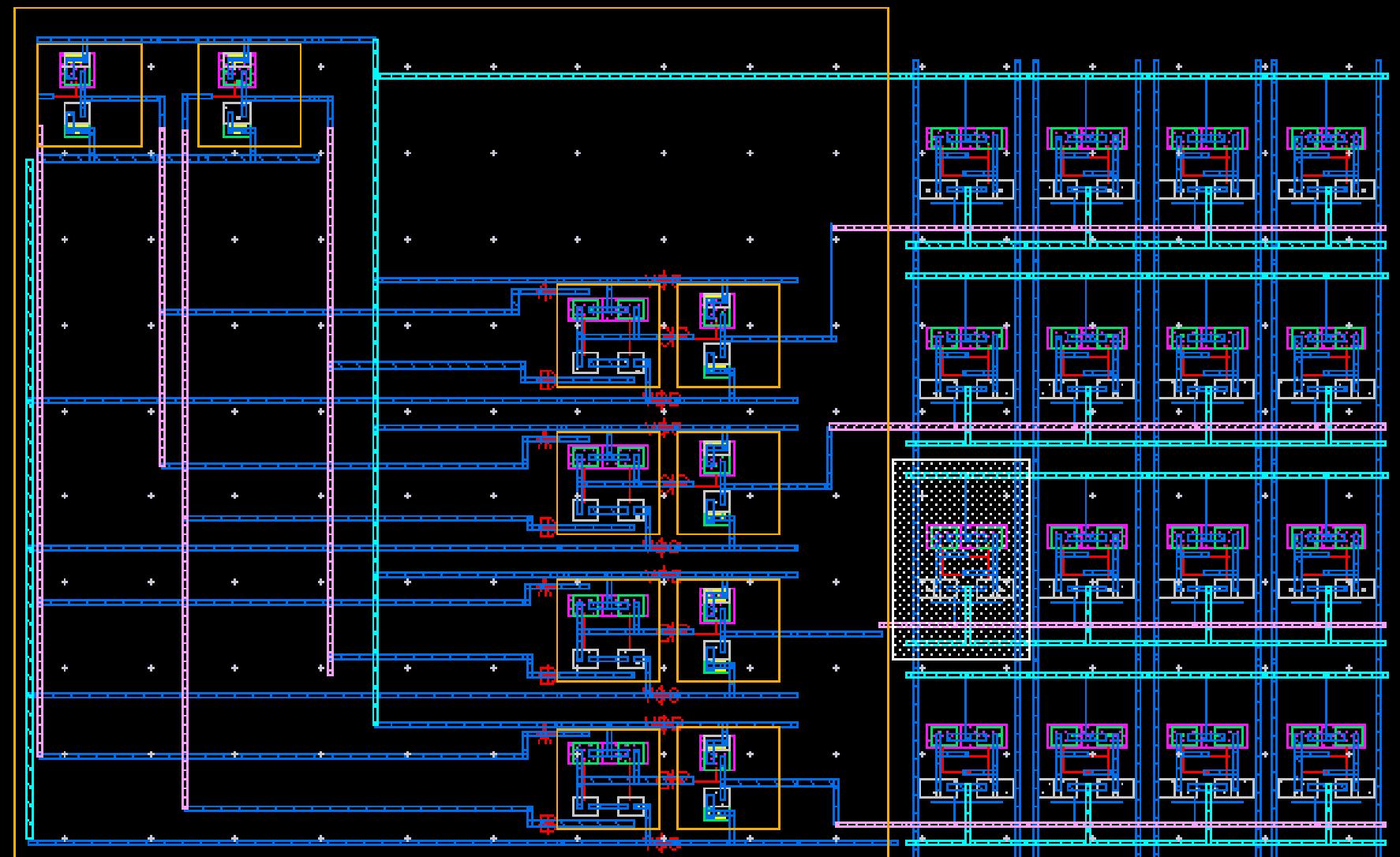


DECODER TO RAM ARRAY INTERFACE



PRECHARGE TO SRAM ARRAY INTERFACE

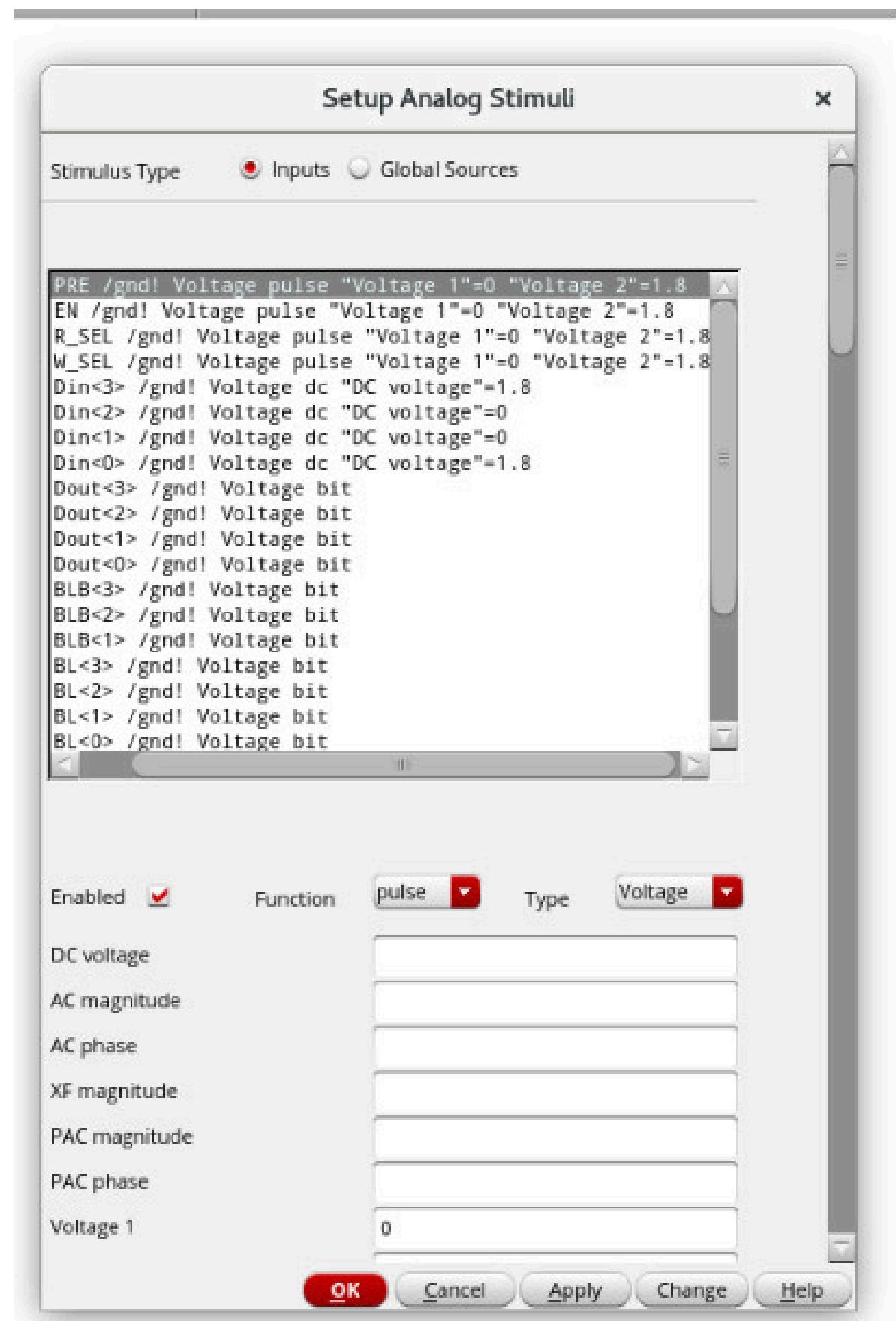




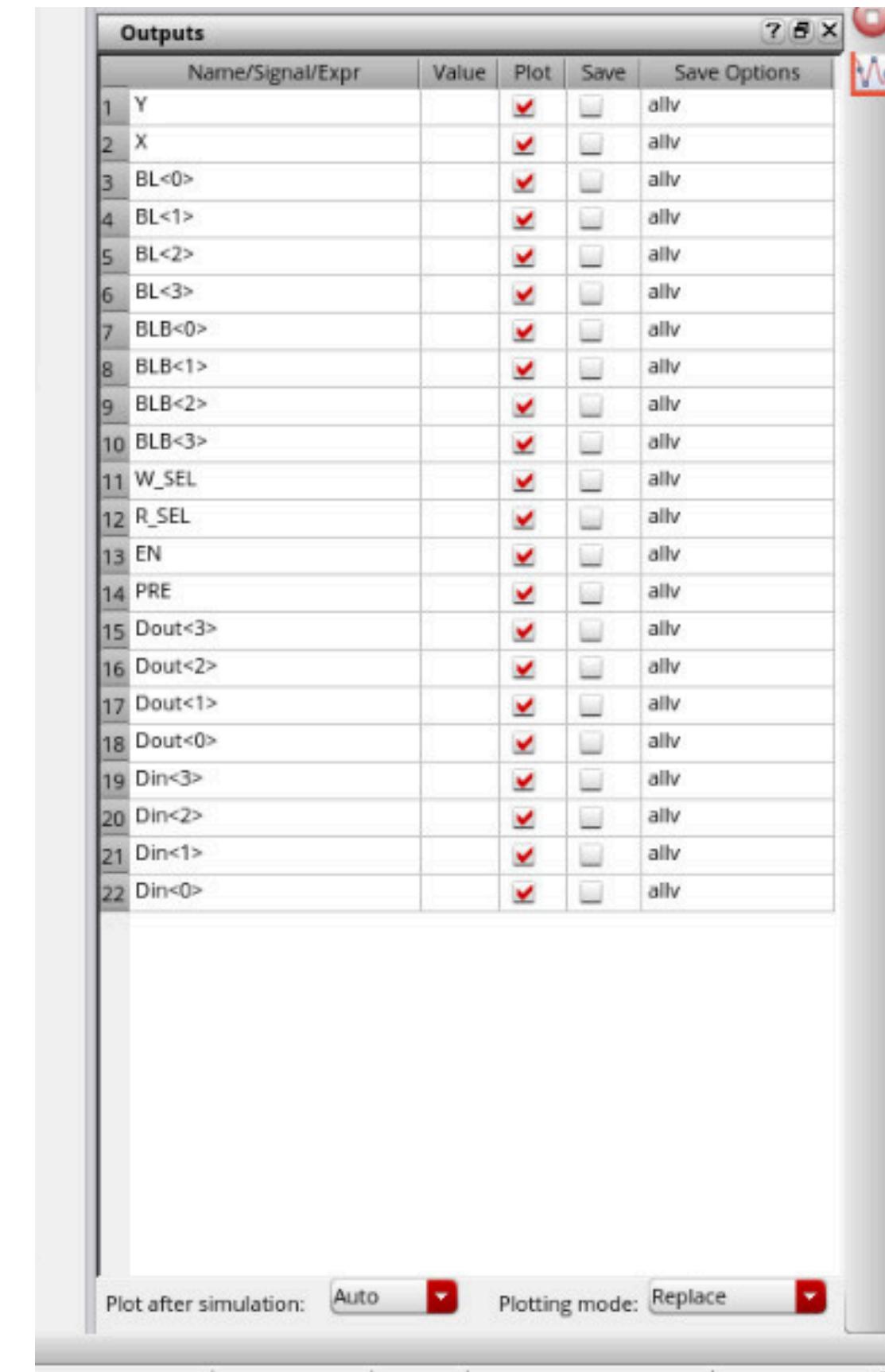
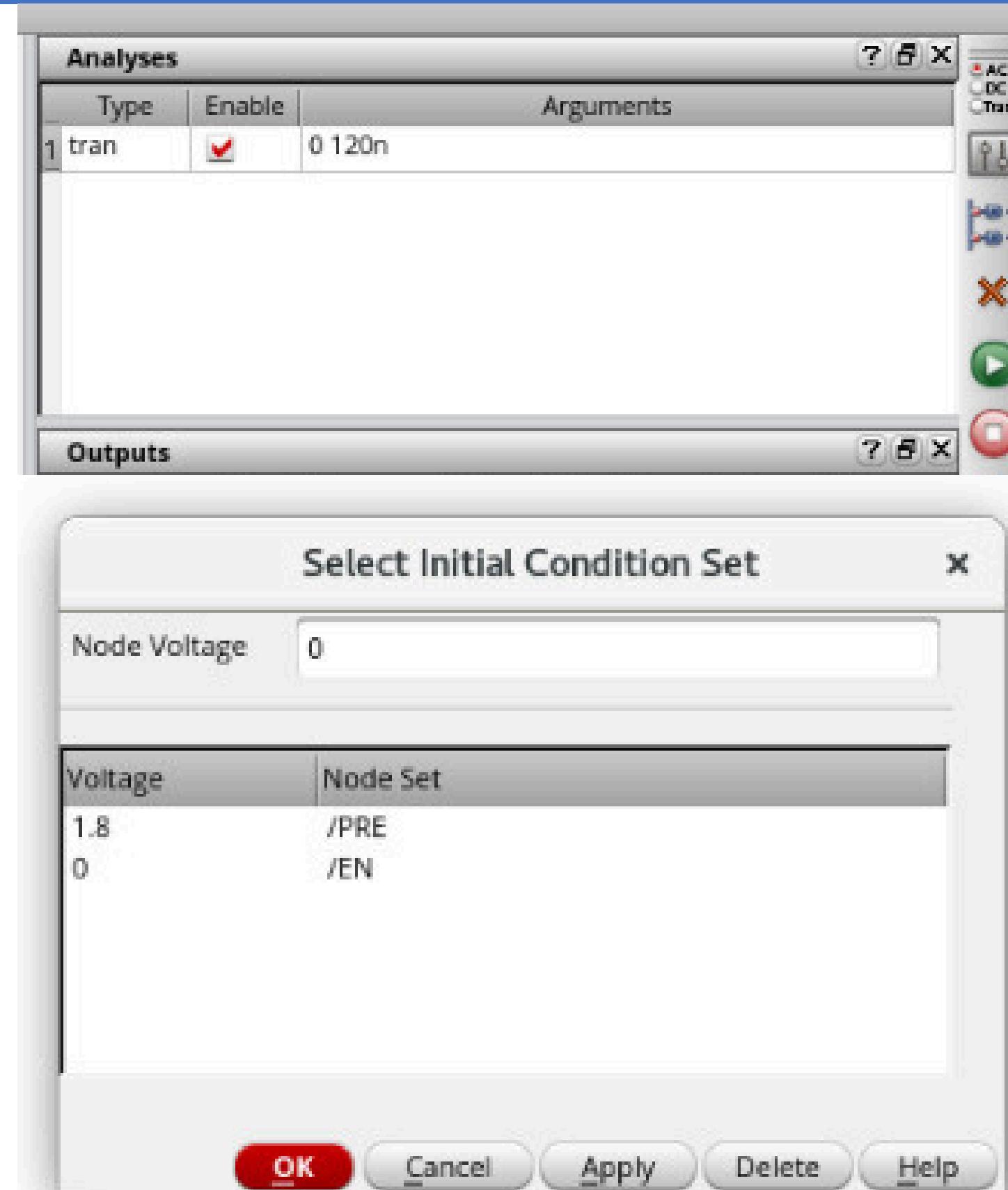
INPUTS

Signal	Delay Time	Period	Pulse Width
Precharge	10 ns	40 ns	30 ns
Enable	5 ns	50 ns	15 ns
Read Select	--	80 ns	40 ns
Write Select	--	120 ns	20 ns

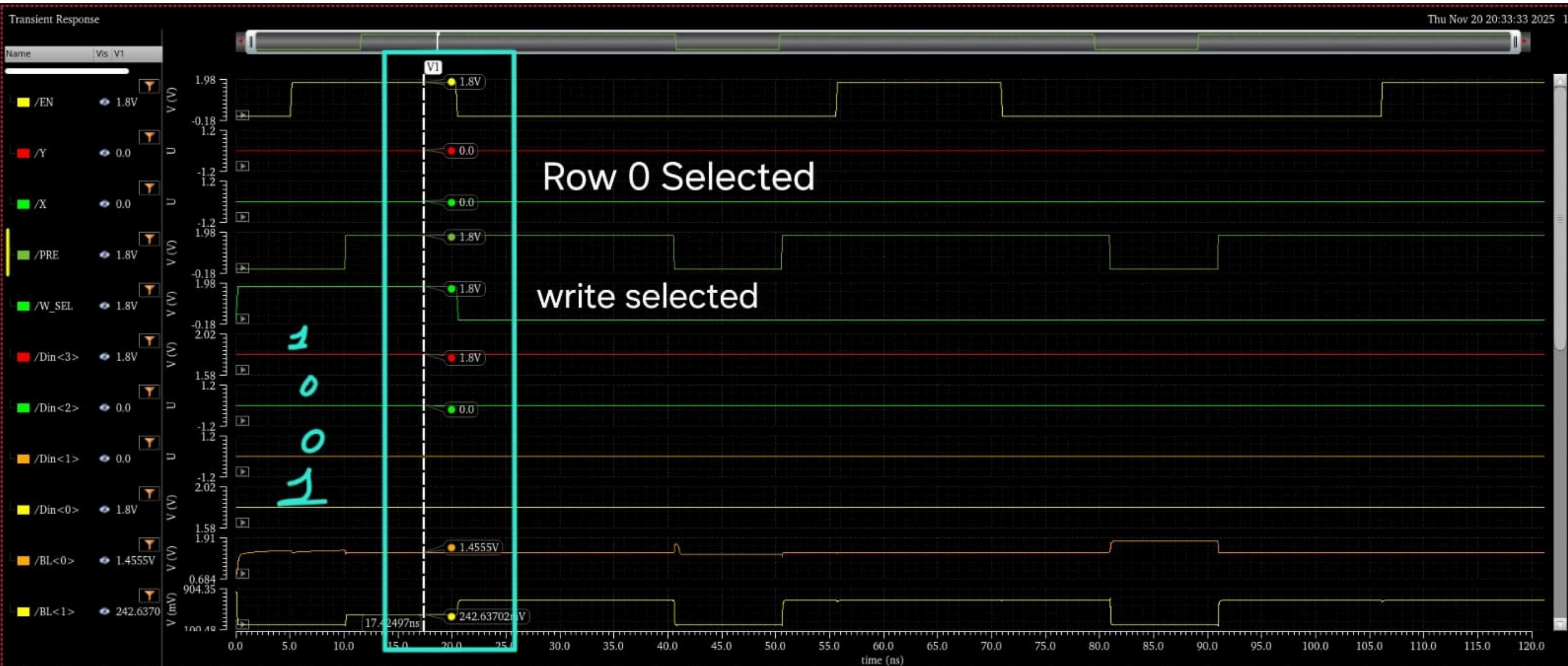
Din3:DC voltage =1.8
 Din2:DC voltage=0
 Din1:DC voltage=0
 Din0:DC voltage=1.8
 VSS:DC Voltage=0
 VDD:DC Voltage=1.8
 Y:DC Voltage=0
 X:DC Voltage=0



INITIAL CONDITIONS, ANALYSES & OUTPUTS



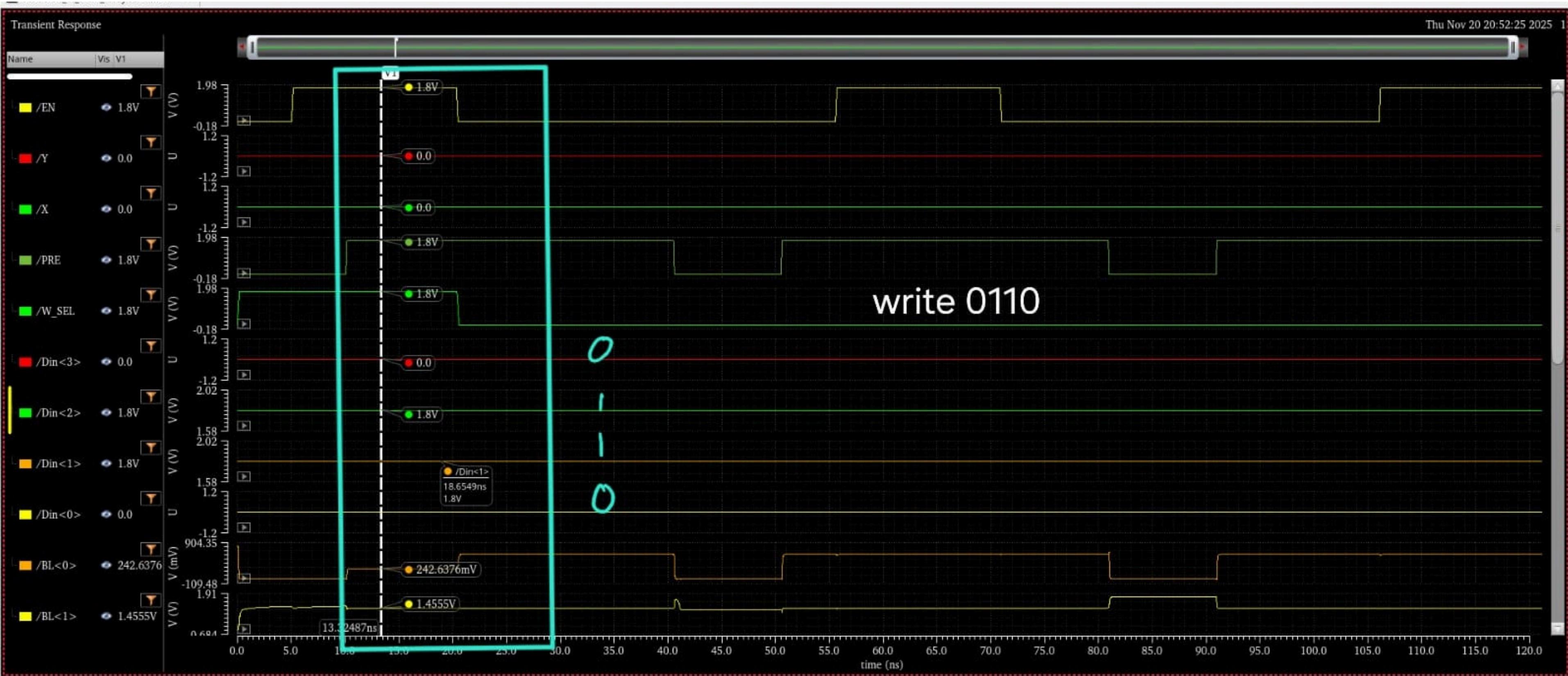
WRITE SELECT



READ SELECT



WRITE OPERATION



READ OPERATION



THANK YOU.