Lab 5 README document

1. **SOF file location:**

   `/rtl/output_files/dds_and_nios_lab.sof`

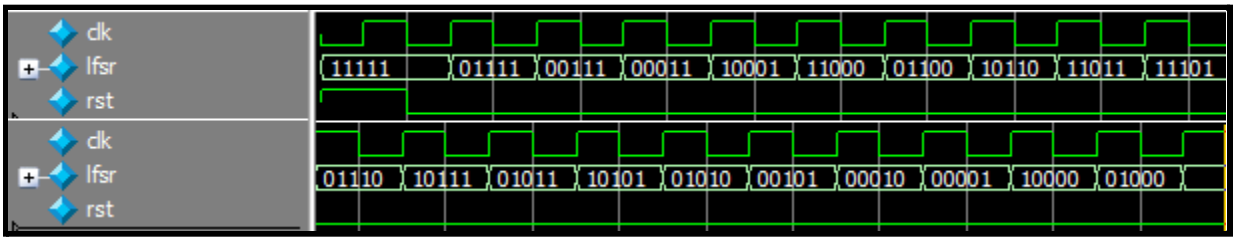
   Additionally created files for lab:

   ```
   /rtl/lfsreg.v
   /rtl/register.v
   /rtl/register12.v
   /rtl/syncron.v
   /rtl/divider.v
   ```

2. **Lab Status:** Lab is 100% functional as per the lab handout requirements.

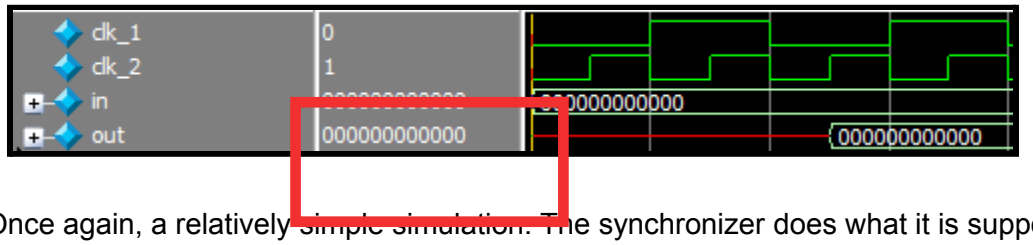
   - LFSR cycles through PN5 sequence properly.
   - ASK signal on oscilloscope works
   - BPSK signal on oscilloscope works
   - LFSR signal on oscilloscope works
   - Signals are shown on VGA monitor
   - FSK signal on oscilloscope works

3. **Simulation Screenshots:**
   LFSR Simulation



   Not much to say here, following the reset signal, the LFSR begins cycling through the PN5 sequence as per the lab handout (Confirmed to be correct).

Synchronizer Simulation



Once again, a relatively simple simulation. The synchronizer does what it is supposed to, by the third clock of clk_2 the output is synced up with the input.

4. **Simulation Information:**

   Simulation software used: ModelSim 14.1

   To run simulations:

   1. All required files for simulation are located in: `/sim/`

      The required files are:
      `lfsreg_tb.v`
      `syncron_tb.v`
      `modules_to_test.v`

      etc. (they are easily found in sim folder)

      `modules_to_test.v` includes all modules to be tested taken from the main project. The simulations run these versions of the modules, but they are functionally identical. Each testbench runs tests for the module it is named after (clock divider tested in previous labs, and thus its simulation is omitted).

      Also included in the directory are wave.do files for each testbench (named similarly).

5. **Additional Information:**

   We included a reset switch on SW[9]. It shouldn't ever be necessary, but it is there just in case.