Lab 4 README document

1. **SOF file location:**

   `/rtl/output_files/rc4.sof`

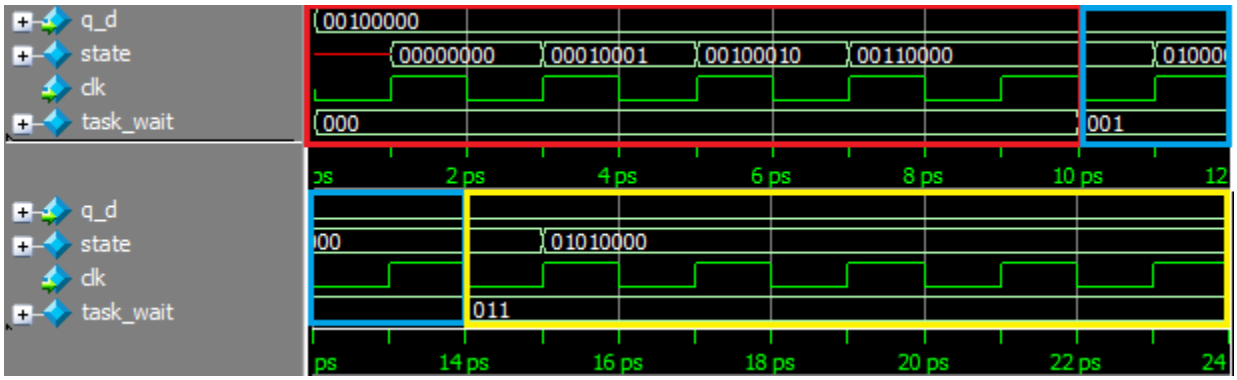
   (Converted top level file from VHDL to Verilog)
   Additionally created .v files for lab:

   `/rtl/simple_rc_solution.v` **(top-level file)**
   `/rtl/key_find_fsm.v`

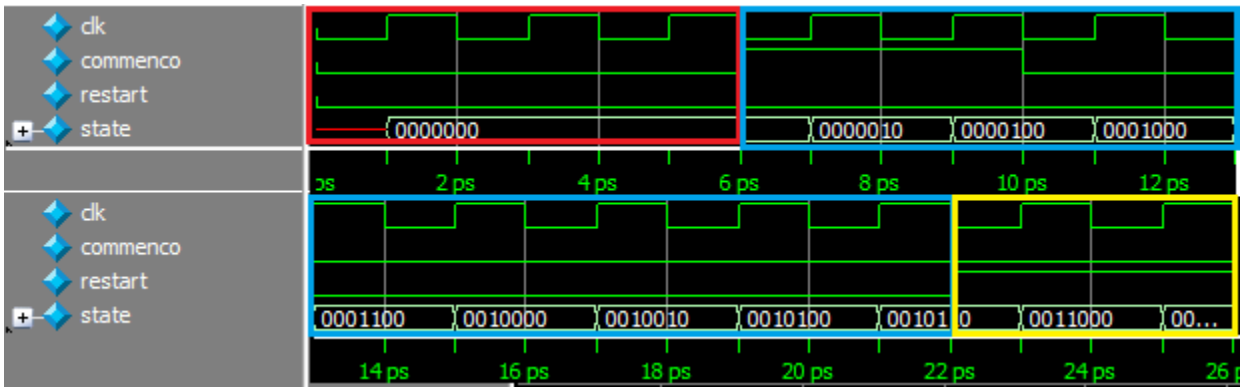
2. **Lab Status:** Lab is 100% functional as per the lab handout requirements.

   - Task 1 complete.
   - Task 2 A and B complete.
     - All messaged decrypt.
   - Task 3 complete.
     - LED[1] when decryption unsuccessful.
     - LED[0] when decryption successful.
     - HEX displays current secret_key under test.

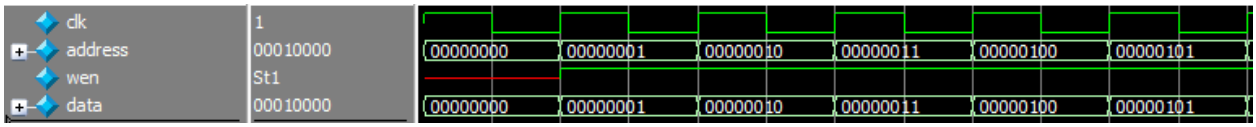
3. **Simulation Screenshots:**
   Key Find FSM Simulation (Task 3):



Task 2b Simulation:



Task 1 Simulation:



4. Simulation Information:

Simulation software used: ModelSim 14.1

To run simulations:

1. All required files for simulation are located in: `/sim/`

   The required files are: `key_find_fsm_tb.v`
   `Modules_under_test.v`

   etc. (they are easily found in sim folder)

   `modules_under_test.v` includes all modules to be tested taken from the main project. The simulations run these versions of the modules, but they are functionally identical. Each testbench runs tests for the module it is named after (divider tested in previous labs, and thus its simulation is omitted).

   Also included in the directory are wave.do files for each testbench (named similarly).

5. Additional Information:

Once the board is programmed it should automatically begin decrypting, otherwise set S[0] ON to begin decrypting.