Full sequential ATPG and fault analysis

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Introduction

The two most typical methods for pattern generation are random and deterministic. Additionally, the ATPG tools can simulate patterns from an external set and place those patterns detecting faults in a test set.

We use the Deterministic Patterns to generate all the internal test patterns for the sequential circuits given. The sequential circuits had both the normal flip flops as well as the scan chain flip flops based on the case in the first part. In the second and third part, we perform the Random Test Pattern generation using 30%, 50% and 80% of the Patterns generated in the first part. We perform the Fault simulation using the Random Patterns and compare the various metrics such as Number of Faults detected, CPU time, the Fault coverage, the Fault classes Detected, Number of Test Patterns etc. Also, in the third part, we run the Test generation for the Faults that we not detected by the Random Patterns in the second and third part and compare each of the results against each other.

We have generated the Random Test Patterns using MATLAB and modified the Verilog file containing the sequential circuits and the ATPG pattern file using Python coding.

The Sequential circuits contain the normal flip flops according to question1. The rest of the questions use the scan flip flops. While, question2 uses single scan chain flip flops, question3 and question4 use the multiple scan chains. The number of scan chains used in question3 is 10. In the case of question4, we have used two parts. Part 1 uses the multiple scan chains in question3, but the order of the flip flops is reversed. Part 2 uses the same order as question3 with the number of scan chains being 15.

Part-1: Sequential Circuit (No Scan Chain)

Here, we use the Normal D Flip Flops. We perform the Test Generation in part a using the given file CUT.v. We generate Random Patterns using 30% of total patterns detected in part a and we perform the Fault Simulation in part b. In part c, we generate random patterns using 50% and 80% of the total patterns detected in part a and perform the Fault simulation. All the random patterns that were generated are 65-bit long – 62 primary inputs and 3 global signals CK, VDD and GND.

1-a) Deterministic Test Pattern Generation

Here, we modify the tcl file using the add faults command and exclude inserting the faults inside the D Flip Flop. We use Tetramax tool to perform the Test Generation using global signals VDD and GND as constraints with values 0 and 1 respectively.

1. Total number of faults = 40432
2. Fault Statistics:

```
report_faults -summary
     Uncollapsed Stuck Fault Summary Report
 ------------------------------------------------
 fault class                     code   #faults
 ------------------------------  ----  ---------
 Detected                         DT       5199
 Possibly detected                PT       1200
 Undetectable                     UD        656
 ATPG untestable                  AU      31932
 Not detected                     ND       1445
 ------------------------------------------------
 total faults                             40432
 test coverage                            14.58%
```

3. The number of test patterns generated to detect all stuck-at fault = 23
4. Fault coverage = 12.85 %
5. Time taken for test generation by the tool = 170 minutes

1-b) Random Test Pattern Simulation Using 30% Patterns in 1-a

Here, we use 30% of 23= 8 Random patterns. We modify the ATPG.pattern file to insert the 8 65-bit Random Patterns and perform the Fault Simulation.

1. Total number of faults = 40432
2. Fault Statistics

```
     Uncollapsed Stuck Fault Summary Report
 ------------------------------------------------
 fault class                     code   #faults
 ------------------------------  ----  ---------
 Detected                         DT       1624
 Possibly detected                PT         31
 Undetectable                     UD        467
 ATPG untestable                  AU      35943
 Not detected                     ND       2367
 ------------------------------------------------
 total faults                             40432
 test coverage                             4.10%
 ------------------------------------------------
```

3. The number of test patterns used for fault simulation = 8
4. Fault coverage = 4.01 %
5. Time taken for test generation by the tool = 0.00 sec
6. List of the faults that were not detected by the random patterns : Please refer to the file *"/project /question_1b/fault.left"*

1-c) Random Test Pattern Simulation

Here, we modify the ATPG.pattern file using our script replace_pattern.py to insert the patterns. We perform Fault Simulation for both 50% as well 80% patterns

a) Using 50 %pattern

The total number of pattern generated in 1(a) is 23. Here, the circuit is fault simulated using an input pattern set of 0.5*23 = 11 random patterns.

1. Total number of faults = 40432
2. Fault Statistics

Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	1641
Possibly detected	PT	31
Undetectable	UD	467
ATPG untestable	AU	35943
Not detected	ND	2350
total faults		40432
test coverage		4.14%

3. The number of test patterns used for fault simulation = 11
4. Fault coverage = 4.05 %
5. Time taken for test generation by the tool = 0.00sec
6. List of the faults that were not detected by the random patterns.: Please refer to the file *"/project /question_1c/50percent/fault.left"*

b) Using 80 %pattern

The total number of pattern generated in 1(a) is 23. Here, the circuit is fault simulated using an input pattern set of 0.8*23 = 18 random patterns.

1. Total number of faults = 40432
2. Fault Statistics

Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	1646
Possibly detected	PT	26
Undetectable	UD	467
ATPG untestable	AU	35943
Not detected	ND	2350
total faults		40432
test coverage		4.15%

3. The number of test patterns used for fault simulation = 18
4. Fault coverage = 4.07 %
5. Time taken for test generation by the tool = 0.00 sec
6. List of the faults that were not detected by the random patterns : Please refer to the file *"/project /question_1c/80percent/fault.left"*

1-d) Test Pattern Generation for undetected faults in 1-b and 1-c

Here, we run the Test pattern generation for the list of faults not detected by the random patterns in part b and c. We use fault.left file in part b and part c to perform the Test generation.

a) For 30 % pattern

1. Total number of faults considered in this step = 2367
2. Fault-classes statistics (Number of detectable faults, Undetectable faults, etc)

fault class	code	#faults
Detected	DT	1133
Possibly detected	PT	0
Undetectable	UD	0
ATPG untestable	AU	1146
Not detected	ND	88
total faults		2367
test coverage		47.87%

3. Fault coverage = 47.87 %
4. Time taken for test generation by the tool = 105.37 sec

For 50 % pattern

1. Total number of faults considered in this step = 2350
2. Fault-classes statistics (Number of detectable faults, Undetectable faults, etc)

Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	1116
Possibly detected	PT	0
Undetectable	UD	0
ATPG untestable	AU	1146
Not detected	ND	88
total faults		2350
test coverage		47.49%

3. Fault coverage = 47.49 %
4. Time taken for test generation by the tool = 105.35 sec

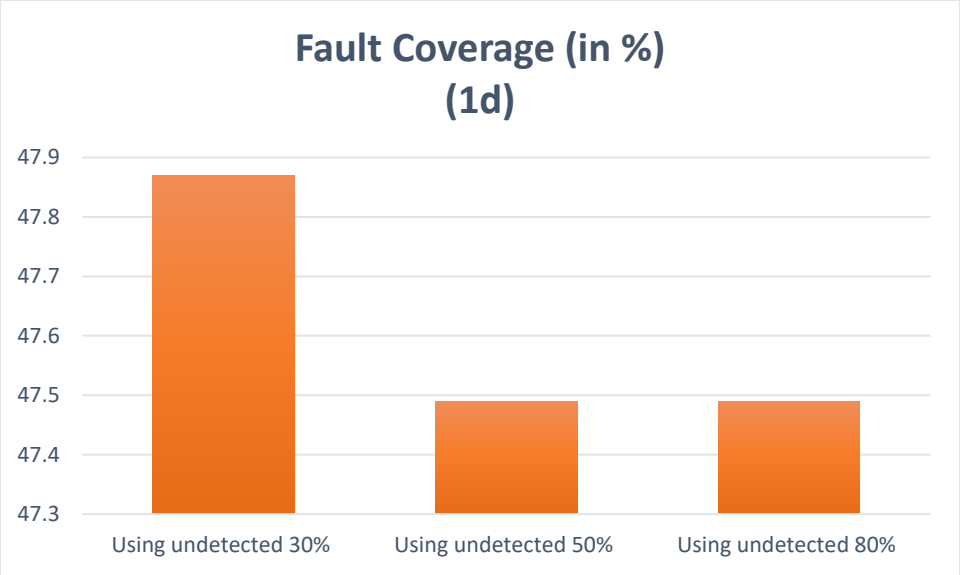
For 80 % pattern

1. Total number of faults considered in this step = 2350
2. Fault-classes statistics (Number of detectable faults, Undetectable faults, etc)

Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	1116
Possibly detected	PT	0
Undetectable	UD	0
ATPG untestable	AU	1146
Not detected	ND	88
total faults		2350
test coverage		47.49%

3. Fault coverage = 47.49 %
4. Time taken for test generation by the tool = 105.37 sec



Overall comparison

	No. of patterns used/generated	Time Taken (in min)	Number of Faults	Fault Coverage (in %)
Using Internal Patterns	23	10200	40432	12.85
Using 30% patterns	7	0.01	40432	4.01
Using 50% patterns	12	0.01	40432	4.05
Using 80% patterns	19	0.01	40432	4.07
Using undetected 30%	8	105	2367	47.87
Using undetected 50%	7	105	2350	47.49
Using undetected 80%	7	106	2350	47.49

Part-2: Sequential Circuit (Single Scan Chain)

Here, we use the Scan Flip Flops. We perform the Test Generation in part a using the modified file for the scan flip flops using single chain CUT_scan.v. We generate Random Patterns using 30% of total patterns detected in part a and we perform the Fault Simulation in part b. In part c, we generate random patterns using 50% and 80% of the total patterns detected in part a and perform the Fault simulation. Here, the GND, VDD, the scan enable SE and the scan-in input SI are added as constraints. For part b and part c, we need to generate Random Patterns for both the scan-in and the Primary inputs. The random

patterns generated for primary inputs are 67-bit long as there are total 62 primary inputs and 5 signals added constraints. The Random patterns for the scan-in are 638 bits long as the number of scan flip flops are 638. These are connected to one another like a shift register.

2-a) Deterministic Test Pattern Generation

Here, modify the tcl file to use the CUT_scan.v file and add the respective constraints mentioned above. We perform the Test Generation using the modified tcl file

1. Total number of faults = 41236
2. Fault Statistics:

```
    Uncollapsed Stuck Fault Summary Report
-----------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT      40797
Possibly detected                PT          0
Undetectable                     UD        427
ATPG untestable                  AU         12
Not detected                     ND          0
-----------------------------------------------
total faults                             41236
test coverage                            99.97%
-----------------------------------------------
```

3. The number of test patterns generated to detect all stuck-at fault = 627
4. Fault coverage = 98.93 %
5. Time taken for test generation by the tool = 2.76 sec

2-b) Random Test Pattern Simulation Using 30% Patterns in 2-a

Here, we use 30% of 627= 188 Random patterns. We modify the ATPG.pattern file to insert the Random Patterns for both scan-in and the primary inputs pi and perform the Fault Simulation.

1. Total number of faults = 41236
2. Fault Statistics

```
    Uncollapsed Stuck Fault Summary Report
-----------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT      30520
Possibly detected                PT          0
Undetectable                     UD        112
ATPG untestable                  AU          0
Not detected                     ND      10604
-----------------------------------------------
total faults                            41236
test coverage                           74.21%
-----------------------------------------------
```

3. The number of test patterns used for fault simulation = 188
4. Fault coverage = 74.01 %
5. Time taken for test generation by the tool = 0.01 sec
6. List of the faults that were not detected by the random patterns Please refer to the file *"/project /question_2b/fault.left"*

2-c) Random Test Pattern Simulation

Here, we use 50% of 627=314 random patterns. We modify the ATPG. Pattern file using our script replace_pattern.py to insert the patterns for both scan-in and pi. Similarly, we use 80% of 627= 502 random patterns for both scan-in and pi. We perform Fault Simulation for both 50% as well 80% patterns.

a) Using 50 %pattern

1. Total number of faults = 41236
2. Fault Statistics

```
    Uncollapsed Stuck Fault Summary Report
-----------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT      30909
Possibly detected                PT          0
Undetectable                     UD        112
ATPG untestable                  AU          0
Not detected                     ND      10215
-----------------------------------------------
total faults                            41236
test coverage                           75.16%
-----------------------------------------------
```

3. The number of test patterns used for fault simulation = 314
4. Fault coverage = 74.95 %
5. Time taken for test generation by the tool = 0.03 sec
6. List of the faults that were not detected by the random patterns.: Please refer to the file *"/project /question_2c/50percent/fault.left"*

b) Using 80 %pattern

1. Total number of faults = 41236
2. Fault Statistics

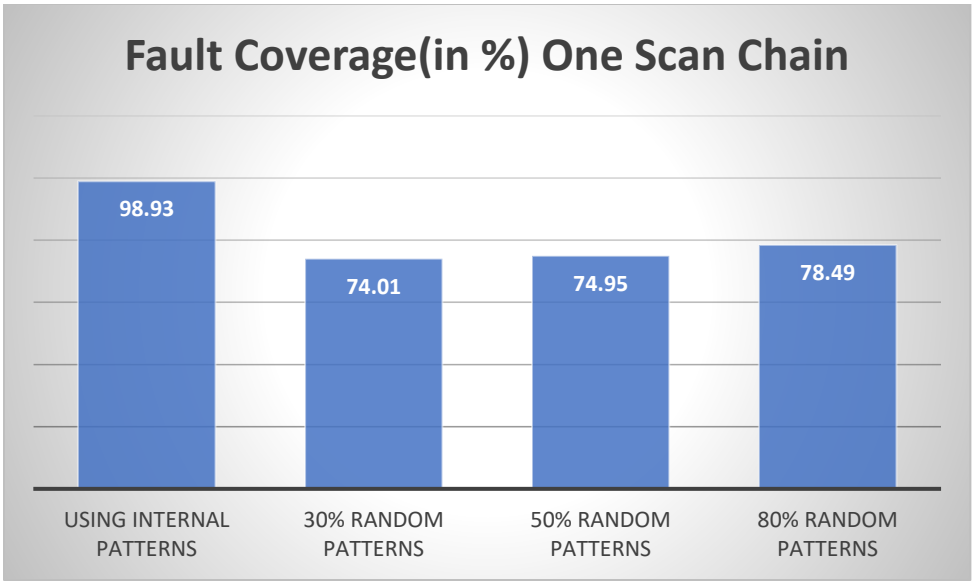
Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	32369
Possibly detected	PT	0
Undetectable	UD	112
ATPG untestable	AU	0
Not detected	ND	8755
total faults		41236
test coverage		78.71%

3. The number of test patterns used for fault simulation = 502
4. Fault coverage = 78.49 %
5. Time taken for test generation by the tool = 0.03 sec
6. List of the faults that were not detected by the random patterns : Please refer to the file *"/project /question_2c/80percent/fault.left"*

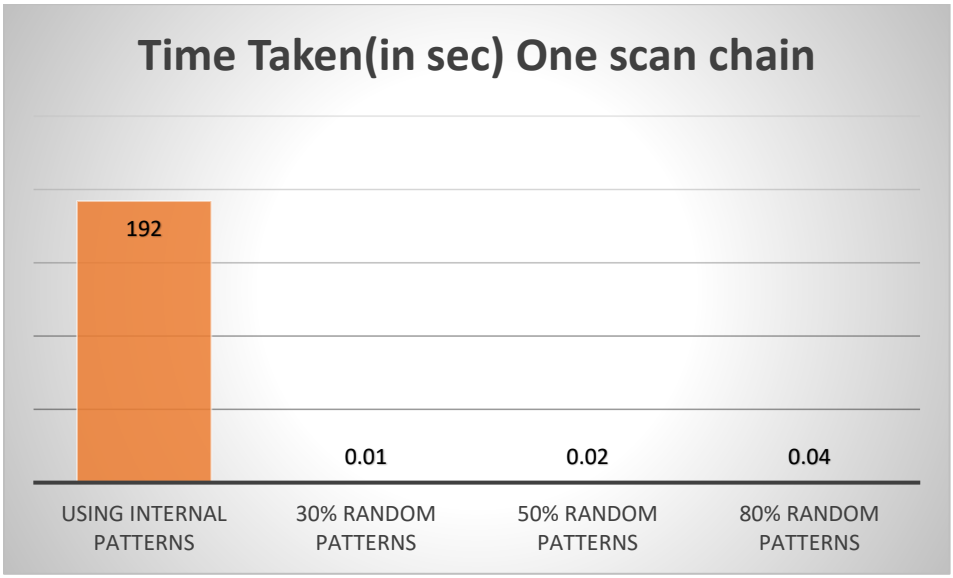
Comparison of Parameters between Q2 a, b and c

1. *Fault Coverage:*



In test generation the tool generates many patterns internally. When random patterns are used, the fault coverage decreases as patterns used by tool in detection are now constrained only to the limited number of user-provided patterns. When number of random patterns used increases, the fault coverage also increases

2. Time taken



The tool creates many patterns internally for test generation and then do fault detection. When random patterns are given, tool only needs to do detection. So, it is less time consuming. As number of patterns increases, time taken also slightly increases.

3. *Faults added*

The number of faults added are the same in all the cases above because the circuit remains unchanged

2-d) Test Pattern Generation for undetected faults in 2-b and 2-c

Here, we run the Test pattern generation for the list of faults not detected by the random patterns in part b and c. We use fault.left file in part b and part c to perform the Test generation.

a) For 30 % pattern

1. Total number of faults considered in this step = 10604
2. Fault-classes statistics (Number of detectable faults, Undetectable faults, etc)

Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	10277
Possibly detected	PT	0
Undetectable	UD	315
ATPG untestable	AU	12
Not detected	ND	0
total faults		10604
test coverage		99.88%

3. Fault coverage = 96.91 %
4. Time taken for test generation by the tool = 2.74 sec

b) For 50 % pattern

1. Total number of faults considered in this step = 10215
2. Fault-classes statistics (Number of detectable faults, Undetectable faults, etc)

Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	9888
Possibly detected	PT	0
Undetectable	UD	315
ATPG untestable	AU	12
Not detected	ND	0
total faults		10215
test coverage		99.88%

3. Fault coverage = 96.79 %
4. Time taken for test generation by the tool = 2.73 sec

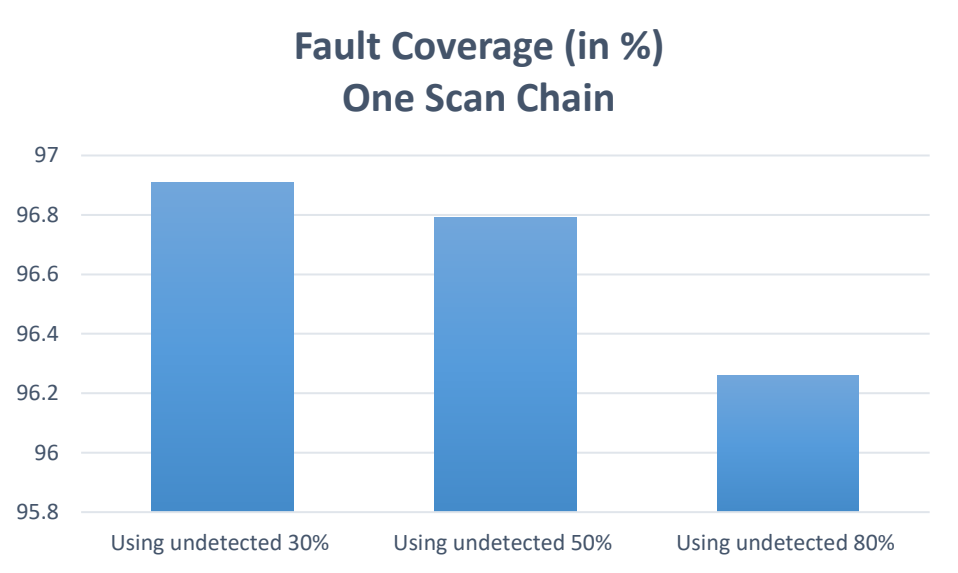
c) For 80 % pattern

1. Total number of faults considered in this step = 8755
2. Fault-classes statistics (Number of detectable faults, Undetectable faults, etc)

Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	8428
Possibly detected	PT	0
Undetectable	UD	315
ATPG untestable	AU	12
Not detected	ND	0
total faults		8755
test coverage		99.86%

3. Fault coverage = 96.29 %
4. Time taken for test generation by the tool = 2.74 sec



Overall COmparison

	No. of patterns used/generated	Time Taken (in sec)	Number of Faults	Fault Coverage (in %)
Using Internal Patterns	627	192	41236	98.93
Using 30% patterns	188	0.01	41236	74.01
Using 50% patterns	314	0.02	41236	74.95
Using 80% patterns	502	0.04	41236	78.49
Using undetected 30%	574	194	10604	96.91
Using undetected 50%	550	193	10215	96.79
Using undetected 80%	530	194	8755	96.26

Part-3: Sequential Circuit (10 Scan Chains)

Here, we use the Scan Flip Flops in multiple scan chains. We perform the Test Generation in part a using the modified file for the scan flip flops using single chain CUT_multiple_scan.v. We generate Random Patterns using 30% of total patterns detected in part a and we perform the Fault Simulation in part b. In part c, we generate random patterns using 50% and 80% of the total patterns detected in part a and perform the Fault simulation. Here, the GND, VDD, the scan enable SE and the ten different scan-in input SI's are added as constraints. For part b and part c, we need to generate Random Patterns for both the scan-in and the Primary inputs. The random patterns generated for primary inputs are 76-bit long as

there are total 62 primary inputs and 10 scan-in signals, clock, VDD, GND and Scan enable SE are added constraints. We have 9 scan chains with 64 flip flops each and the tenth scan chain has 62 flip flops. Hence, the random patterns given to scan-in inputs are 64-bit long. All the scan chains have 10 different scan-in inputs SI1, SI2, SI3, SI4, SI5, SI6, SI7, SI8, SI9 and SI10 and 10 different scan-out outputs SO1, SO2, SO3, SO4, SO5, SO6, SO7, SO8, SO9, SO10. All the scan-chains have a common scan enable SE.

3-a) Deterministic Test Pattern Generation

Here, modify the tcl file to use the CUT_multiple_scan.v file and add the respective constraints mentioned above. We perform the Test Generation using the modified tcl file

1. Total number of faults = 41272
2. Fault Statistics:

Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	40833
Possibly detected	PT	0
Undetectable	UD	427
ATPG untestable	AU	12
Not detected	ND	0
total faults		41272
test coverage		99.97%

3. The number of test patterns generated to detect all stuck-at fault = 656
4. Fault coverage = 98.93 %
5. Time taken for test generation by the tool = 2.74 sec

3-b) Random Test Pattern Simulation Using 30% Patterns in 3-a

Here, we use 30% of 657= 197 Random patterns. We modify the ATPG.pattern file to insert the Random Patterns for both scan-in and the primary inputs pi and perform the Fault Simulation

1. Total number of faults = 41272
2. Fault Statistics

```
    Uncollapsed Stuck Fault Summary Report
-----------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT      30123
Possibly detected                PT          0
Undetectable                     UD        112
ATPG untestable                  AU          0
Not detected                     ND      11037
-----------------------------------------------
total faults                            41272
test coverage                           73.19%
-----------------------------------------------
```

3. The number of test patterns used for fault simulation = 197
4. Fault coverage = 72.98 %
5. Time taken for test generation by the tool = 0.02 sec
6. List of the faults that were not detected by the random patterns Please refer to the file *"/project /question_3b/fault.left"*

3-c) Random Test Pattern Simulation

Here, we use 50% of 657=328 random patterns. We modify the ATPG. Pattern file using our script replace_pattern.py to insert the patterns for both scan-in and pi. Similarly, we use 80% of 627= 525 random patterns for both scan-in and pi. We perform Fault Simulation for both 50% as well 80% patterns.

a) Using 50 %pattern

1. Total number of faults = 41272
2. Fault Statistics

```
    Uncollapsed Stuck Fault Summary Report
-----------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT      30729
Possibly detected                PT          0
Undetectable                     UD        112
ATPG untestable                  AU          0
Not detected                     ND      10431
-----------------------------------------------
total faults                            41272
test coverage                           74.66%
-----------------------------------------------
```

3. The number of test patterns used for fault simulation = 328
4. Fault coverage = 74.45 %
5. Time taken for test generation by the tool = 0.03 sec
6. List of the faults that were not detected by the random patterns.: Please refer to the file *"/project /question_3c/50percent/fault.left"*

b) Using 80 %pattern

1. Total number of faults = 41272
2. Fault Statistics

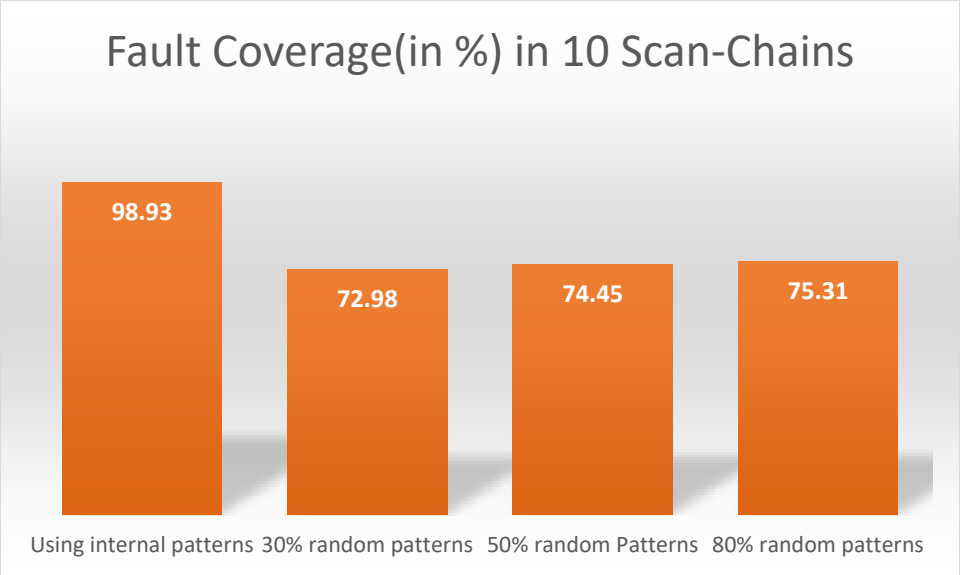
Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	31086
Possibly detected	PT	0
Undetectable	UD	112
ATPG untestable	AU	0
Not detected	ND	10074
total faults		41272
test coverage		75.52%

3. The number of test patterns used for fault simulation = 525
4. Fault coverage = 75.31%
5. Time taken for test generation by the tool = 0.04 sec
6. List of the faults that were not detected by the random patterns : Please refer to the file *"/project /question_3c/80percent/fault.left"*

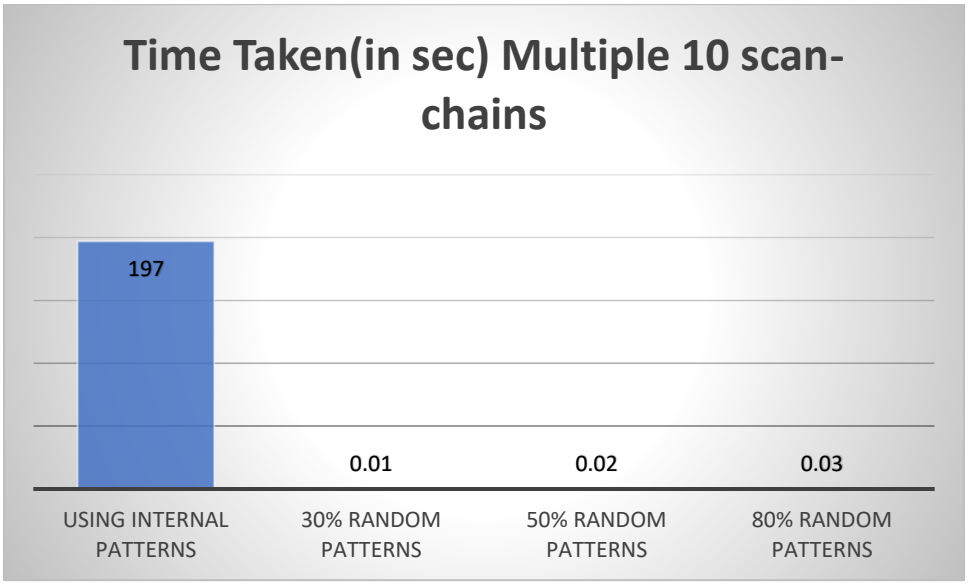
Comparison of Parameters between Q3 a, b and c

1. *Fault Coverage:*



In test generation the tool generates many patterns internally. When random patterns are used, the fault coverage decreases as patterns used by tool in detection are now constrained only to the limited number of user-provided patterns. When number of random patterns used increases, the fault coverage also increases

2. Time taken



The tool creates many patterns internally for test generation and then do fault detection. When random patterns are given, tool only needs to do detection. So, it is less time consuming. As number of patterns increases, time taken also slightly increases.

3. Faults added

The number of faults added are the same in all the cases above because the circuit remains unchanged

3-d) Test Pattern Generation for undetected faults in 3-b and 3-c

Here, we run the Test pattern generation for the list of faults not detected by the random patterns in part b and c. We use fault.left file in part b and part c to perform the Test generation.

a) For 30 % pattern

1. Total number of faults considered in this step = 11037
2. Fault-classes statistics (Number of detectable faults, Undetectable faults, etc)

Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	10710
Possibly detected	PT	0
Undetectable	UD	315
ATPG untestable	AU	12
Not detected	ND	0
total faults		11037
test coverage		99.89%

3. Fault coverage = 97.05 %
4. Time taken for test generation by the tool = 2.74 sec

b) For 50 % pattern

1. Total number of faults considered in this step = 10431
2. Fault-classes statistics (Number of detectable faults, Undetectable faults, etc)

Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	10104
Possibly detected	PT	0
Undetectable	UD	315
ATPG untestable	AU	12
Not detected	ND	0
total faults		10431
test coverage		99.88%

3. Fault coverage = 96.86 %
4. Time taken for test generation by the tool = 2.75 sec

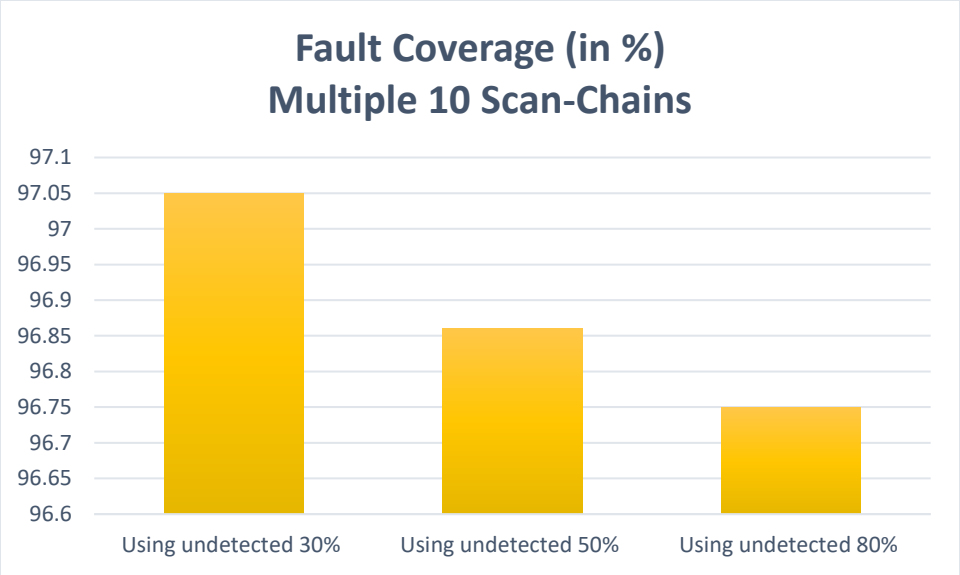
c) For 80 % pattern

1. Total number of faults considered in this step = 10074
2. Fault-classes statistics (Number of detectable faults, Undetectable faults, etc)

Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	9747
Possibly detected	PT	0
Undetectable	UD	315
ATPG untestable	AU	12
Not detected	ND	0
total faults		10074
test coverage		99.88%

3. Fault coverage = 96.75 %
4. Time taken for test generation by the tool = 2.74 sec



Overall Comparison

	No. of patterns used/generated	Time Taken (in sec)	Number of Faults	Fault Coverage (in %)
Using Internal Patterns	656	197	41272	98.93
Using 30% patterns	197	0.01	41272	72.98
Using 50% patterns	328	0.02	41272	74.45
Using 80% patterns	512	0.03	41272	75.31
Using undetected 30%	599	194	11037	97.05
Using undetected 50%	558	195	10431	96.86
Using undetected 80%	540	194	10074	96.75

Part-4: Sequential Circuit (10 Scanchains in Reverse)

Here, we use the Scan Flip Flops in multiple scan chains with the order of flip flops reversed that is the flip flops are connected from bottom to top and the scan-out comes out of the top flip flop in the respective scan-chain. We perform the Test Generation in part a using the modified file for the scan flip

flops using single chain CUT_reverse_scan.v. We generate Random Patterns using 30% of total patterns detected in part a and we perform the Fault Simulation in part b. In part c, we generate random patterns using 50% and 80% of the total patterns detected in part a and perform the Fault simulation. Here, the GND, VDD, the scan enable SE and the ten different scan-in input SI's are added as constraints. For part b and part c, we need to generate Random Patterns for both the scan-in and the Primary inputs. The random patterns generated for primary inputs are 76-bit long as there are total 62 primary inputs and 10 scan-in signals, clock, VDD, GND and Scan enable SE are added constraints. We have 9 scan chains with 64 flip flops each and the tenth scan chain has 62 flip flops. Hence, the random patterns given to scan-in inputs are 64-bit long. All the scan chains have 10 different scan-in inputs SI1, SI2, SI3, SI4, SI5, SI6, SI7, SI8, SI9 and SI10 and 10 different scan-out outputs SO1, SO2, SO3, SO4, SO5, SO6, SO7, SO8, SO9, SO10. All the scan-chains have a common scan enable SE.

4-a) Deterministic Test Pattern Generation

Here, modify the tcl file to use the CUT_reverse_scan.v file and add the respective constraints mentioned above. We perform the Test Generation using the modified tcl file.

1. Total number of faults = 41272
2. Fault Statistics:

Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	40425
Possibly detected	PT	40
Undetectable	UD	427
ATPG untestable	AU	380
Not detected	ND	0
total faults		41272
test coverage		99.02%

3. The number of test patterns generated to detect all stuck-at fault = 619
4. Fault coverage = 97.94 %
5. Time taken for test generation by the tool = 2.78 sec

4-b) Random Test Pattern Simulation Using 30% Patterns in 4-a

Here, we use 30% of 619= 186 Random patterns. We modify the ATPG.pattern file to insert the Random Patterns for both scan-in and the primary inputs pi and perform the Fault Simulation.

1. Total number of faults = 41272
2. Fault Statistics

```
report_faults -summary
     Uncollapsed Stuck Fault Summary Report
 ------------------------------------------------
 fault class                     code   #faults
 ------------------------------  ----  ---------
 Detected                         DT      29698
 Possibly detected                PT          4
 Undetectable                     UD        112
 ATPG untestable                  AU        345
 Not detected                     ND      11113
 ------------------------------------------------
 total faults                             41272
 test coverage                            72.16%
 ------------------------------------------------
```

3. The number of test patterns used for fault simulation = 186
4. Fault coverage = 71.95 %
5. Time taken for test generation by the tool = 0.02 sec
6. List of the faults that were not detected by the random patterns Please refer to the file *"project /question_4b/fault.left"*

4-c) Random Test Pattern Simulation

Here, we use 50% of 619=310 random patterns. We modify the ATPG. Pattern file using our script replace_pattern.py to insert the patterns for both scan-in and pi. Similarly, we use 80% of 619= 495 random patterns for both scan-in and pi. We perform Fault Simulation for both 50% as well 80% patterns.

a) Using 50 %pattern

1. Total number of faults = 41272
2. Fault Statistics

```
     Uncollapsed Stuck Fault Summary Report
 ------------------------------------------------
 fault class                     code   #faults
 ------------------------------  ----  ---------
 Detected                         DT      30364
 Possibly detected                PT          4
 Undetectable                     UD        112
 ATPG untestable                  AU        345
 Not detected                     ND      10447
 ------------------------------------------------
 total faults                             41272
 test coverage                            73.78%
 ------------------------------------------------
```

3. The number of test patterns used for fault simulation = 310
4. Fault coverage = 73.57 %
5. Time taken for test generation by the tool = 0.03 sec
6. List of the faults that were not detected by the random patterns.: Please refer to the file *"project /question_4c/50percent/fault.left"*

b) Using 80 %pattern

1. Total number of faults = 41272
2. Fault Statistics

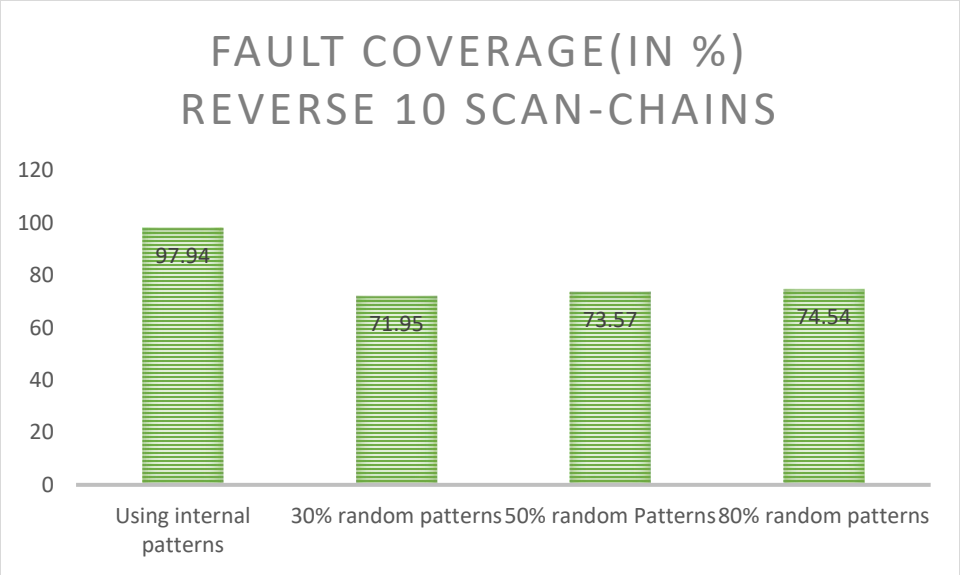
Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	30765
Possibly detected	PT	2
Undetectable	UD	112
ATPG untestable	AU	345
Not detected	ND	10048
total faults		41272
test coverage		74.75%

3. The number of test patterns used for fault simulation = 495
4. Fault coverage = 74.54 %
5. Time taken for test generation by the tool = 0.03 sec
6. List of the faults that were not detected by the random patterns : Please refer to the file *"/project /question_4c/80percent/fault.left"*

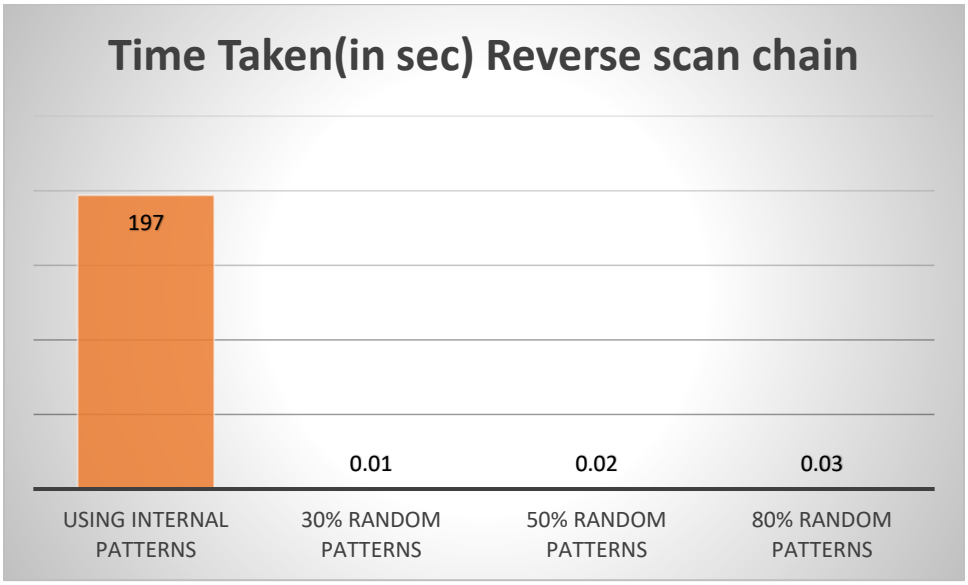
Comparison of Parameters between Q4 a, b and c

1. *Fault Coverage:*



In test generation the tool generates many patterns internally. When random patterns are used, the fault coverage decreases as patterns used by tool in detection are now constrained only to the limited number of user-provided patterns. When number of random patterns used increases, the fault coverage also increases

2. *Time taken*



The tool creates many patterns internally for test generation and then do fault detection. When random patterns are given, tool only needs to do detection. So, it is less time consuming. As number of patterns increases, time taken also slightly increases.

3. *Faults added*

The number of faults added are the same in all the cases above because the circuit remains unchanged

4-d) Test Pattern Generation for undetected faults in 4-b and 4-c

Here, we run the Test pattern generation for the list of faults not detected by the random patterns in part b and c. We use fault.left file in part b and part c to perform the Test generation

a) For 30 % pattern

1. Total number of faults considered in this step = 11113
2. Fault-classes statistics (Number of detectable faults, Undetectable faults, etc)

Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	10723
Possibly detected	PT	2
Undetectable	UD	315
ATPG untestable	AU	73
Not detected	ND	0
total faults		11113
test coverage		99.31%

3. Fault coverage = 96.49 %
4. Time taken for test generation by the tool = 2.75 sec

b) For 50 % pattern

1. Total number of faults considered in this step = 10447
2. Fault-classes statistics (Number of detectable faults, Undetectable faults, etc)

Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	10057
Possibly detected	PT	2
Undetectable	UD	315
ATPG untestable	AU	73
Not detected	ND	0
total faults		10447
test coverage		99.27%

3. Fault coverage = 96.26 %
4. Time taken for test generation by the tool = 2.80 sec

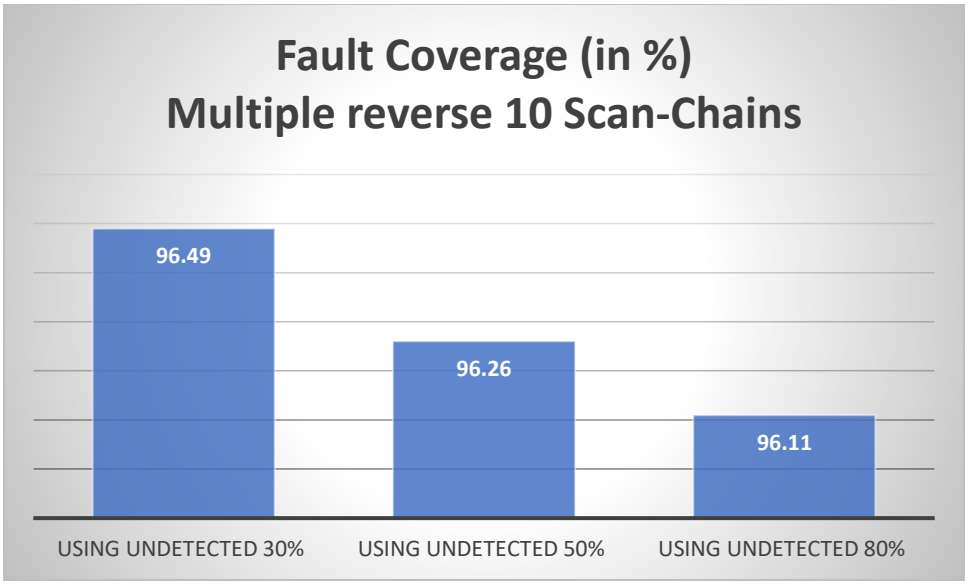
c) For 80 % pattern

1. Total number of faults considered in this step = 10048
2. Fault-classes statistics (Number of detectable faults, Undetectable faults, etc)

Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	9658
Possibly detected	PT	2
Undetectable	UD	315
ATPG untestable	AU	73
Not detected	ND	0
total faults		10048
test coverage		99.24%

3. Fault coverage = 96.11 %
4. Time taken for test generation by the tool = 2.73 sec



Overall Comparison

	No. of patterns used/generated	Time Taken (in sec)	Number of Faults	Fault Coverage (in %)
Using Internal Patterns	619	197	41272	97.94
Using 30% patterns	186	0.01	41272	71.95
Using 50% patterns	310	0.02	41272	73.57
Using 80% patterns	495	0.03	41272	74.54
Using undetected 30%	576	195	11113	96.49
Using undetected 50%	539	200	10447	96.26
Using undetected 80%	510	193	10048	96.11

Part-5: Sequential Circuit (15 Scanchain)

Here, we use the Scan Flip Flops in multiple scan chains with the order of flip flops same as question 3 that is the flip flops are connected from top to bottom and the scan-out comes out of the bottom flip flop in the respective scan-chain. We perform the Test Generation in part a using the modified file for the scan flip flops using single chain CUT_15_scanchain.v. We generate Random Patterns using 30% of total patterns detected in part a and we perform the Fault Simulation in part b. In part c, we generate random patterns using 50% and 80% of the total patterns detected in part a and perform the Fault simulation. Here, the GND, VDD, the scan enable SE and the fifteen different scan-in input SI's are added

as constraints. For part b and part c, we need to generate Random Patterns for both the scan-in and the Primary inputs. The random patterns generated for primary inputs are 81-bit long as there are total 62 primary inputs and 15 scan-in signals, clock, VDD, GND and Scan enable SE are added constraints. We have 9 scan chains with 43 flip flops each and the fifteenth scan chain has 36 flip flops. Hence, the random patterns given to scan-in inputs are 43-bit long. All the scan chains have 15 different scan-in inputs SI1, SI2, SI3, SI4, SI5, SI6, SI7, SI8, SI9, SI10, SI11, SI12, SI13, SI14 and SI15 and 15 different scan-out outputs SO1, SO2, SO3, SO4, SO5, SO6, SO7, SO8, SO9, SO10, SO11, SO12, SO13, SO14 and SO15. All the scan-chains have a common scan enable SE.

5-a) Deterministic Test Pattern Generation

Here, modify the tcl file to use the CUT_15_scanchain.v file and add the respective constraints mentioned above. We perform the Test Generation using the modified tcl file

1. Total number of faults = 41292
2. Fault Statistics:

Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	40853
Possibly detected	PT	0
Undetectable	UD	427
ATPG untestable	AU	12
Not detected	ND	0
total faults		41292
test coverage		99.97%

3. The number of test patterns generated to detect all stuck-at fault = 651
4. Fault coverage = 98.93 %
5. Time taken for test generation by the tool = 2.74 sec

5-b) Random Test Pattern Simulation Using 30% Patterns in 5-a

Here, we use 30% of 651= 196 Random patterns. We modify the ATPG.pattern file to insert the Random Patterns for both scan-in and the primary inputs pi and perform the Fault Simulation.

1. Total number of faults = 41292
2. Fault Statistics

```
    Uncollapsed Stuck Fault Summary Report
-----------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT      29905
Possibly detected                PT          0
Undetectable                     UD        112
ATPG untestable                  AU          0
Not detected                     ND      11275
-----------------------------------------------
total faults                             41292
test coverage                            72.62%
-----------------------------------------------
```

3. The number of test patterns used for fault simulation = 196
4. Fault coverage = 72.42 %
5. Time taken for test generation by the tool = 0.02 sec
6. List of the faults that were not detected by the random patterns Please refer to the file *"/project /question_5b/fault.left"*

5-c) Random Test Pattern Simulation

Here, we use 50% of 651=326 random patterns. We modify the ATPG. Pattern file using our script replace_pattern.py to insert the patterns for both scan-in and pi. Similarly, we use 80% of 651= 521 random patterns for both scan-in and pi. We perform Fault Simulation for both 50% as well 80% patterns

a) Using 50 %pattern

1. Total number of faults = 41292
2. Fault Statistics

```
    Uncollapsed Stuck Fault Summary Report
-----------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT      31153
Possibly detected                PT          0
Undetectable                     UD        112
ATPG untestable                  AU          0
Not detected                     ND      10027
-----------------------------------------------
total faults                             41292
test coverage                            75.65%
-----------------------------------------------
```

3. The number of test patterns used for fault simulation = 326
4. Fault coverage = 75.44 %
5. Time taken for test generation by the tool = 0.03 sec
6. List of the faults that were not detected by the random patterns.: Please refer to the file *"/project /question_5c/50percent/fault.left"*

b) Using 80 %pattern

1. Total number of faults = 41292
2. Fault Statistics

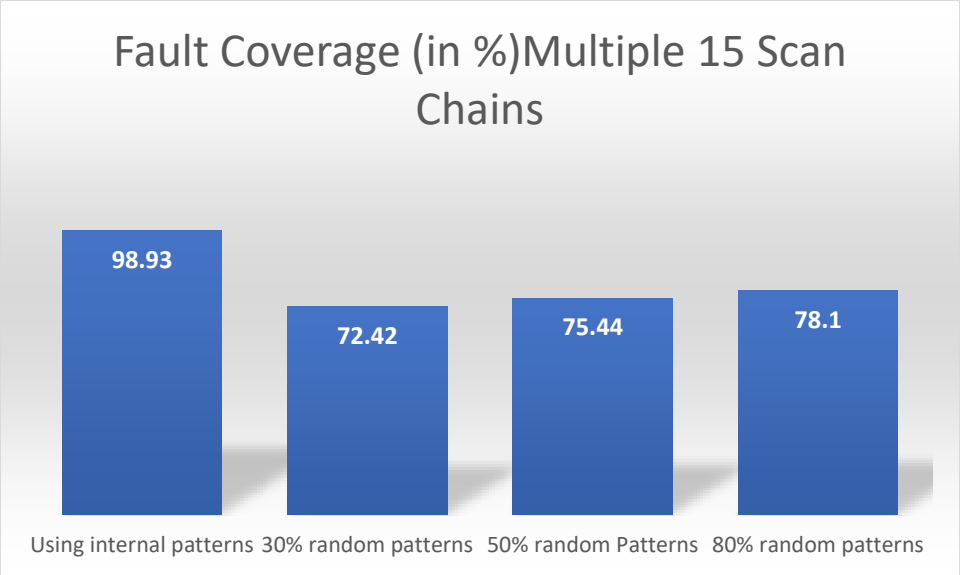
Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	32250
Possibly detected	PT	0
Undetectable	UD	112
ATPG untestable	AU	0
Not detected	ND	8930
total faults		41292
test coverage		78.31%

3. The number of test patterns used for fault simulation = 521
4. Fault coverage = 78.1 %
5. Time taken for test generation by the tool = 0.03 sec
6. List of the faults that were not detected by the random patterns : Please refer to the file *"/project /question_5c/80percent/fault.left"*

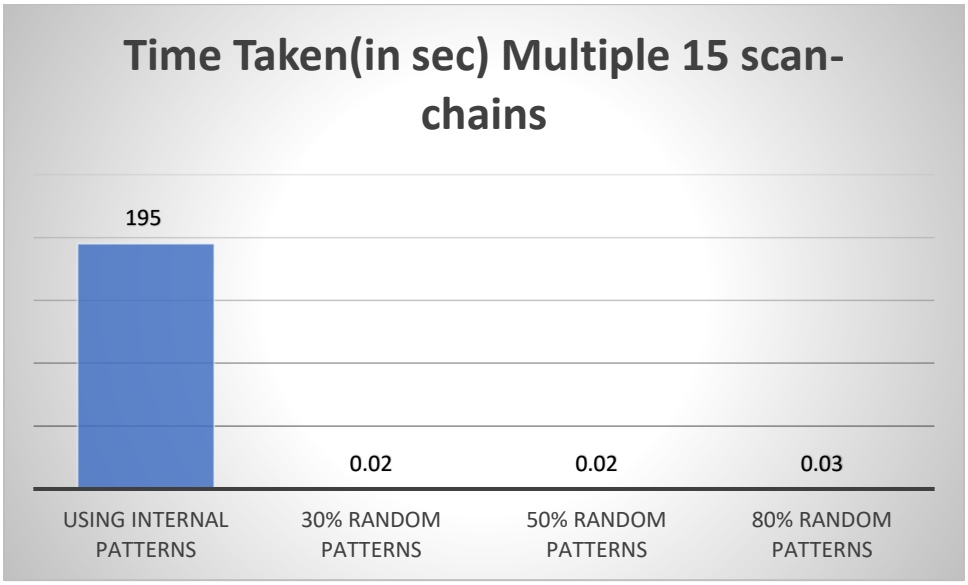
Comparison of Parameters between Q5 a, b and c

1. *Fault Coverage:*



In test generation the tool generates many patterns internally. When random patterns are used, the fault coverage decreases as patterns used by tool in detection are now constrained only to the limited number of user-provided patterns. When number of random patterns used increases, the fault coverage also increases

2. *Time taken*



The tool creates many patterns internally for test generation and then do fault detection. When random patterns are given, tool only needs to do detection. So, it is less time consuming. As number of patterns increases, time taken also slightly increases.

3. *Faults added*

The number of faults added are the same in all the cases above because the circuit remains unchanged

5-d) Test Pattern Generation for undetected faults in 5-b and 5-c

Here, we run the Test pattern generation for the list of faults not detected by the random patterns in part b and c. We use fault.left file in part b and part c to perform the Test generation.

a) For 30 % pattern

1. Total number of faults considered in this step = 11275
2. Fault-classes statistics (Number of detectable faults, Undetectable faults, etc)

Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	10948
Possibly detected	PT	0
Undetectable	UD	315
ATPG untestable	AU	12
Not detected	ND	0
total faults		11275
test coverage		99.89%

3. Fault coverage = 97.09 %
4. Time taken for test generation by the tool = 2.73 sec

b) For 50 % pattern

1. Total number of faults considered in this step = 10027
2. Fault-classes statistics (Number of detectable faults, Undetectable faults, etc)

Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	9700
Possibly detected	PT	0
Undetectable	UD	315
ATPG untestable	AU	12
Not detected	ND	0
total faults		10027
test coverage		99.88%

3. Fault coverage = 96.73 %
4. Time taken for test generation by the tool = 2.73 sec

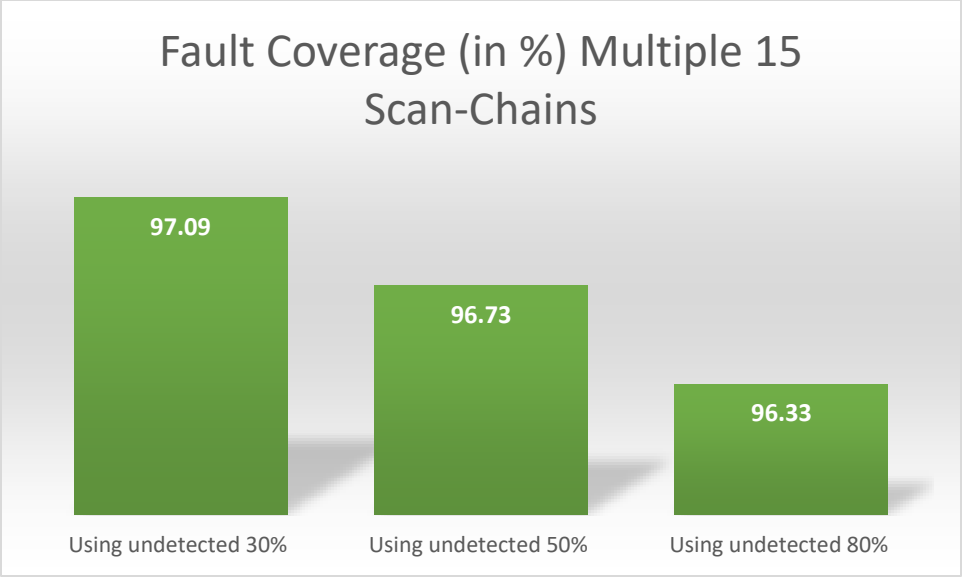
c) For 80 % pattern

1. Total number of faults considered in this step = 8930
2. Fault-classes statistics (Number of detectable faults, Undetectable faults, etc)

Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	8603
Possibly detected	PT	0
Undetectable	UD	315
ATPG untestable	AU	12
Not detected	ND	0
total faults		8930
test coverage		99.86%

3. Fault coverage = 96.33 %
4. Time taken for test generation by the tool = 2.88 sec



Overall Comparison

	No. of patterns used/generated	Time Taken (in sec)	Number of Faults	Fault Coverage (in %)
Using Internal Patterns	651	195	41292	98.93
Using 30% patterns	192	0.02	41292	72.42
Using 50% patterns	326	0.02	41292	75.44
Using 80% patterns	521	0.03	41292	78.1
Using undetected 30%	574	193	11275	97.09
Using undetected 50%	557	193	10027	96.73
Using undetected 80%	517	208	8930	96.33

Comparison between Q1,Q2,Q3,Q4 and Q5

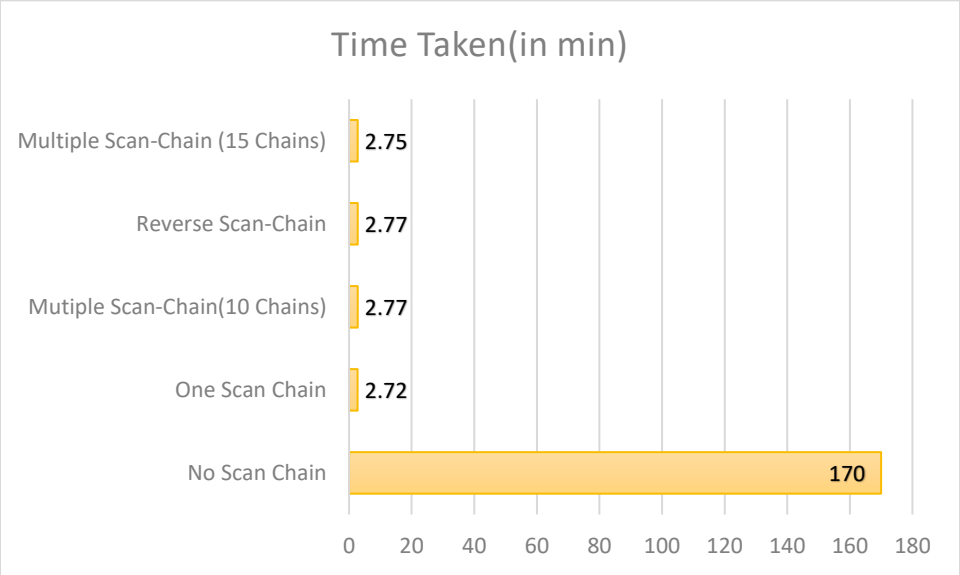
1. Test generation Statistics based on faults added internally by tool (Q1a , 2a, 3a, 4a, 5a)

	Total Faults	Test Patterns Generated	Fault Coverage (in%)	Time Taken for test generation (in min)
No scan chain	40432	23	12.85	170
One scan chain	41236	627	98.93	2.72
Multiple 10 scan-chains	41272	656	98.93	2.77
Reverse scan chain	41272	619	97.94	2.77
Multiple 15 scan-chains	41292	651	98.93	2.75

2. Test Generation for undetected Faults Statistics Comparison (Based on 30% case only) [Q1d, 2d, 3d, 4d, 5d]

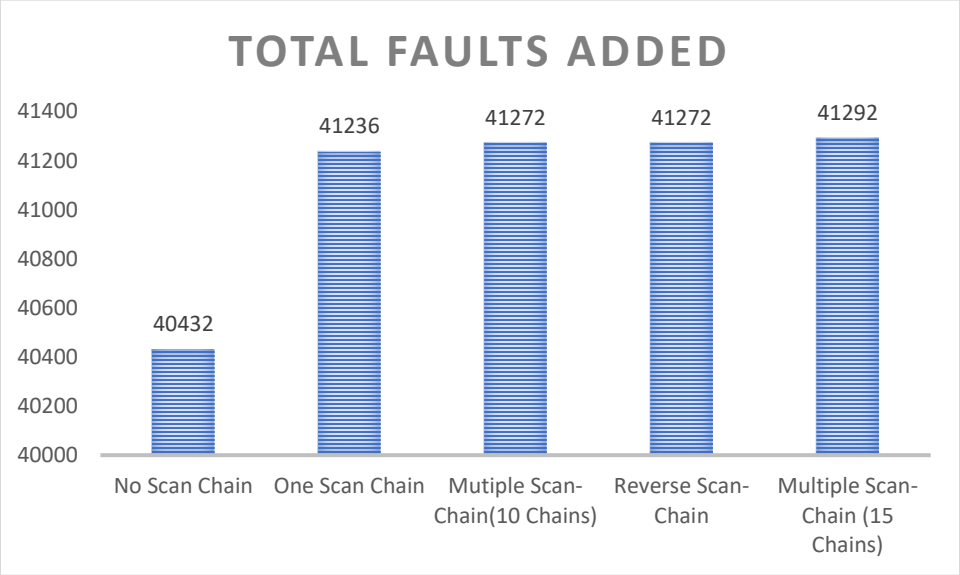
	Total Faults	Fault Coverage	Time Taken for test generation	Detected Faults	Undetectable Faults	ATPG Untestable
No scan chain	2367	47.86	1.45	1133	0	1146
One scan chain	10604	96.91	2.74	10277	315	12
Multiple 10 scan-chains	11307	97.03	2.74	10710	315	12
Reverse scan chains	11113	96.49	2.75	10723	315	73
Multiple 15 scan-chains	11275	97.09	2.73	10948	315	12

3. Time Taken for Test Generation



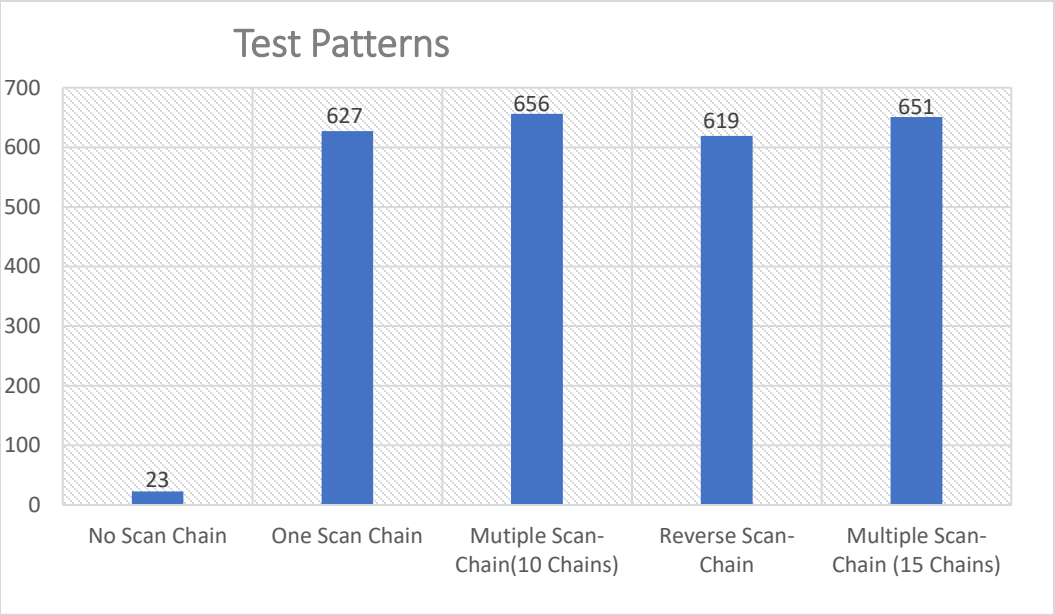
Without scan chain, pattern generation is done by duplication of combinational circuit. This is more time consuming. Test generation took 2 hrs 40 min for creating test patterns. When scan chain is added, no replication is needed as tool generates patterns for FF initial states. So time for test generation is less

4. Total Faults added



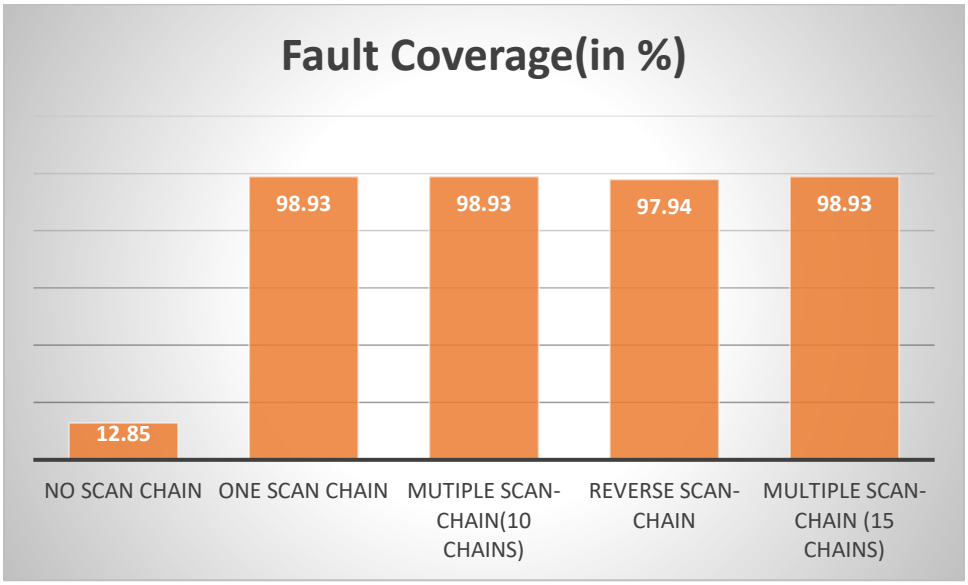
Number of faults added are increasing as the complexity of the circuit is increasing. When the scan chains are added, more PI and PO are created. So the number of fault locations increases.

5.Number of Test patterns generated in Test Generation



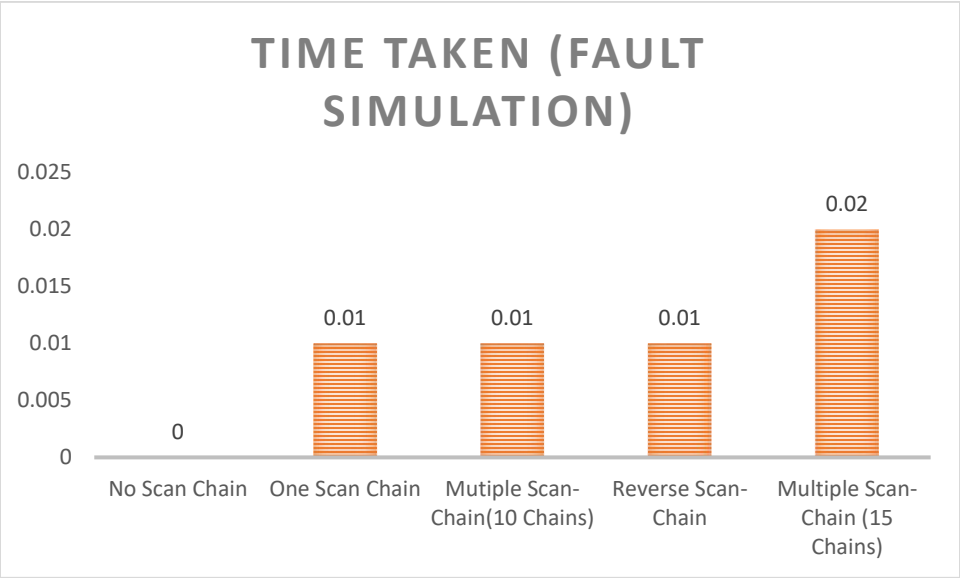
When no scan chain is used, the patterns are found by replication of combinational circuit. Since FF outputs are unknown, TMAX can generate very less patterns that can detected faults. When scan chains are added, the tools creates patterns for scan inputs. SO more faults are detected , ie, number of patterns is also higher with scan chains

6.Fault Coverage in Test Generation



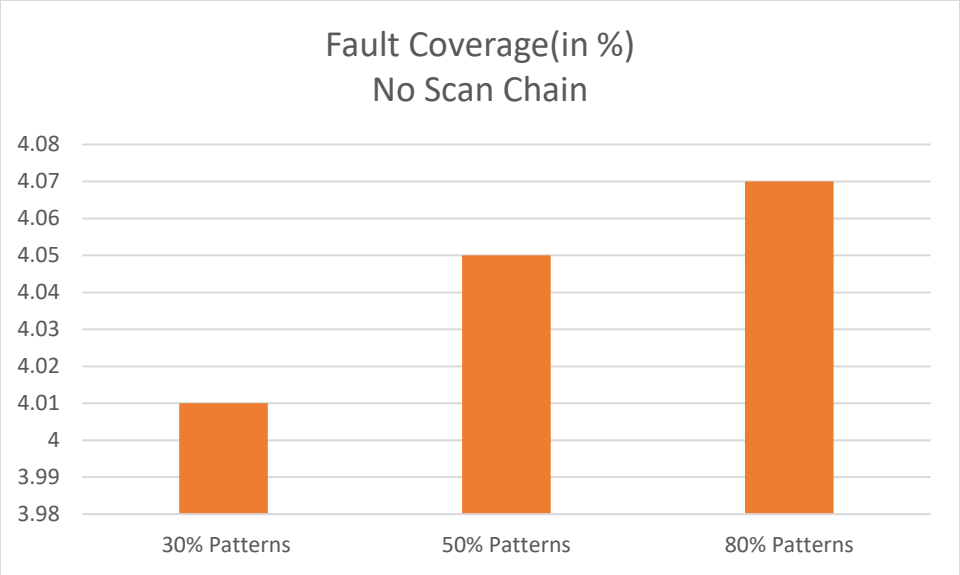
When no scan chain is present, Faults are found by replications of combinational circuit. Very less number of faults are detected here as the initial state of Flipflops are unknown. So fault coverage is less. When scan chain is added, tool generates pattern for scan input as well to assign initial state of FF. So, fault coverage increases.

7. Time taken in fault simulation

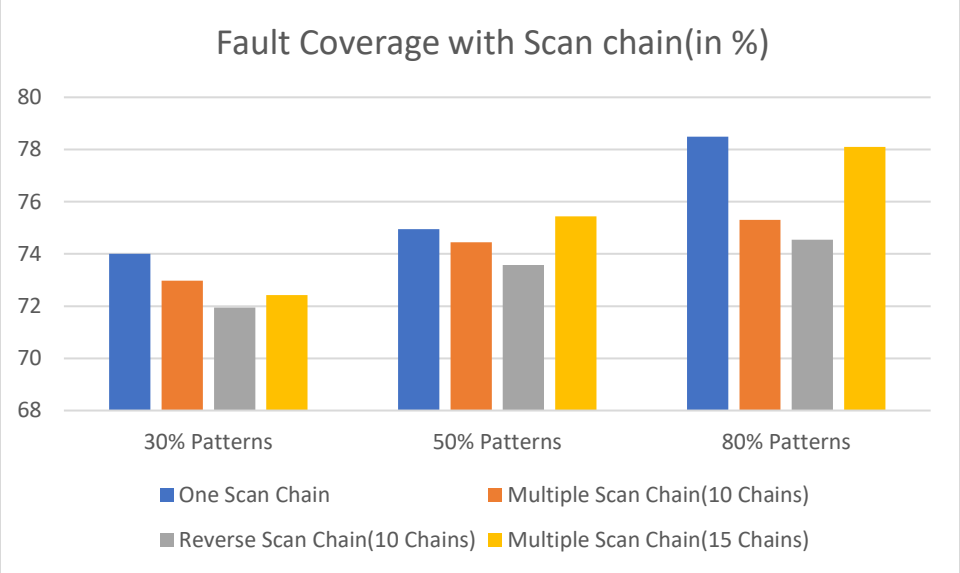


In fault simulation, the user provided patterns are used by tool for detect faults. When scan chains are added, we are giving more number of patterns- ie pattern for both primary input and for scan input. Due to this, the time taken increases.

8. Fault Coverage in Fault Simulation (With and without scanchain)



As seen in the above and below graphs, as the number of input random patterns increases, the fault coverage also increases.



In fault simulation using random patterns, we see a slight dip in fault coverage moving from one scanchain to multiple scanchain. This could be because , the combination of random scan pattern and random PI pattern specified in input STIL file could lead to detection of less faults.