Driver Circuit of MZI Modulator for PICs

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***Abstract*— A CMOS-based optical modulator driver circuit is designed and characterized for plasma-dispersion effect-based Mach-Zehnder Modulator. The transient response of anode and cathode drivers for the P-N carrier depletion-based phase shifter is simulated on the Synopsys platform. These design parameters of driver circuits are useful to achieve about 5-7 Gbps data modulation in the optical domain.**

Keywords—Modulator driver, CMOS, Transient response, PN-based Mach-Zehnder Modulator, PICs

I. INTRODUCTION

The carrier depletion-based PN junction phase-shifter used in the Mach-Zehnder Interferometer (MZI) for optical modulation has provided a promising solution for extremely high data rate optical modulation on CMOS compatible Photonic Integrated Circuits (PICs) [1]. The change in refractive index in the PN junction is achieved by supplying necessary electrical voltage variations in CMOS-based modulator driver circuits. A typical PN-junction-based Mach-Zehnder Optical modulator is shown in Fig. 1, consisting of Y-splitter, PN junction rib-waveguide, and asymmetric arms made of 500x220nm silicon waveguide, 4-port directional coupler. Fig. 2 shows the GDS-II layout drawn on KLayout using SIEPIC-pdk (process-design-kit) [5-6] of MZM using Grating couplers as input/output devices. Fig. 3 shows the block diagram of MZM showing the sections of Anode and Cathode drivers, which have been considered to be designed in this article[2].

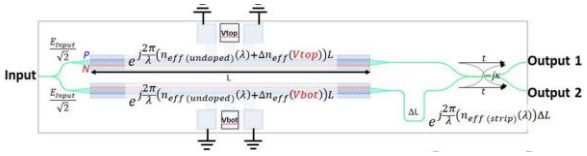

Fig. 1. PN-carrier depletion based Optical Modulator [1]

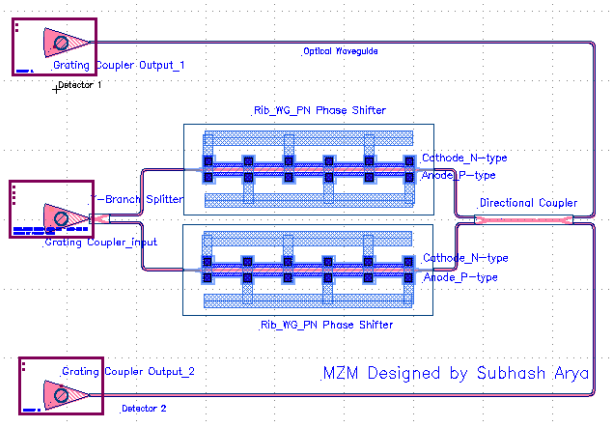

Fig. 2. GDS-II Layout of MZM using SIEPIC-pdk and tool [5-6]

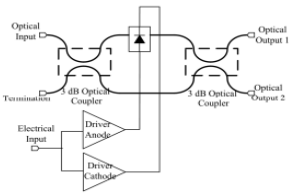

Fig. 3. The architecture of MZM, including Modulator Drivers [2]

II. MODULATOR DRIVER CIRCUITS

A. *Driver cathode circuit input to PN-phase shifter*

The asymmetric driver circuit was developed by R. Rakowski et al. [3], and was implemented for the MZI modulator by Audrey Michard et al. [2]. The topology of the anode driver is based on an inverter chain. However, an additional circuit enables to reduce the high voltage level under the built-in potential since PN-junction is working in reversed biased conditions. The detailed circuit of the anode terminal is shown in Fig. 4 (a), which consists of M_{p1} to M_{p6} p-channel and M_{n1} to M_{n6} n-channel MOSFETs. The design parameters for circuit simulation have been taken from [2]. Fig. 4(b) shows the schematic of anode and cathode driver circuits on Synopsis schematic viewer as per ref [2]

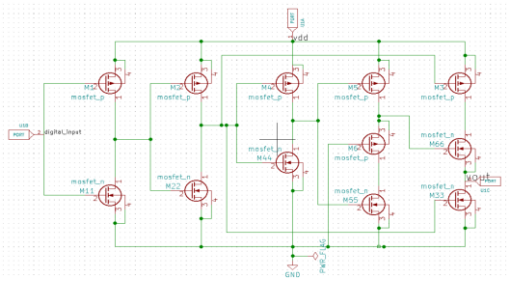

Fig. 4(a). Circuit diagram of modulator for anode terminal in PN-phase shifter realized on eSim [2]

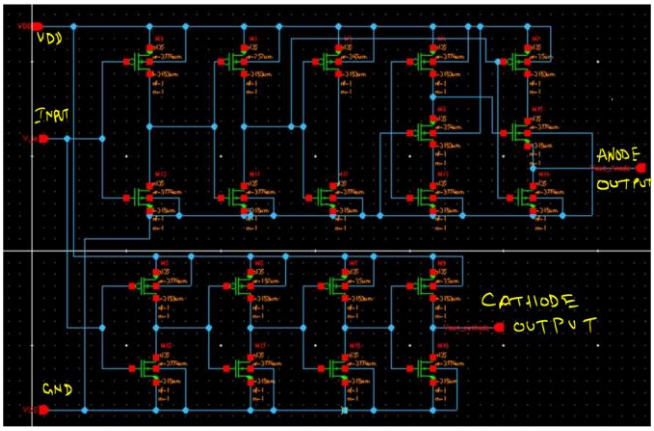

Fig. 4(b). The schematic of anode and cathode driver circuits on Synopsis schematic viewer as per ref [2]

B. Driver Circuit for cathode terminal in PN-phase Shifter

The driver circuit for the cathode terminal is used to shape input signals and drive a high capacitive load. The circuit consists of a chain of four CMOS inverters, as shown in Fig 4(b) lower portion, of which parameters were determined using the logical effort method [4].

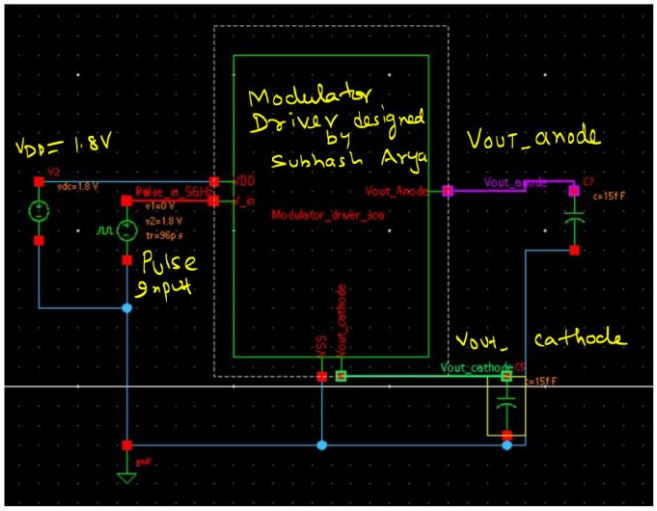

Fig. 5. Symbol of the schematic of modulator driver with its external input and output ports and voltages

III. Simulation Results and Discussion

The modulator asymmetric driver circuits for anode and cathode terminals are implemented in Synposis simulation software to characterize the transient response. Following are the steps described in brief, which I followed to get the transient response of driver circuits:

Step 1: The cloud-based server provided each user a terminal on Unix operating system to remotely access it using confidential credentials.

Step 2: A complete video course on designing 10 bit DAC on the Synopsis platform explained by Mr. Sameer was beneficial, which I followed comprehensively.

Step 3: I created a folder modularo_driver_sca on the desktop and then created a library followed by importing SAED pdk32 nm in the folder.

Step 4: I opened CUSTOME COMPILER and then created a custom library name ***mod_driv_sca***, created a cell name ***mod_driv***, and after that new schematic view on which the driver circuits were drawn using pdk and various tools available on canvas as shown in Fig. 4(b).

Step 5: A design rule check using the check and save button was done, and warnings and errors were removed by revisiting the circuits on schematic view. Once No rule violations are found in "***mod_driv_sca/mod_driv/schematic***," then create the symbol of entire circuits as shown in Fig. 5.

Step 6. A testbench was created, namely "***mod_sca_testbench***" schematic in which external voltage sources such as VDD, GND, Pulse, capacitors etc., were added, and simulation parameters were fed at appropriate places.

Step 7. A TestSuite was open on the PrimeSim test bench, and transient analysis mode was selected with its start time of 0.01 ns to 3 ns. After that, in the simulation menu, the Netlist and Run command was executed to generate a netlist of the schematic and plot the transient response of driver circuits.

Step 8. Finally, we observe the relation between input pulse and two output signals at anode and cathode terminals in the WaveView tab of Synopsys/PrimeSim_Testbench and record the results, and analyze it.

The anode/cathode driver's transient response is shown in Fig. 6 (a) as per the circuit implemented in eSim. The faster response of driver circuits is essential for high-speed modulation. The carrier depletion-based PN junction implanted in MZI arms is operated in the reverse biased condition to maximize the plasma-dispersion effect. That effect led to a change in refractive index of the waveguide through which the optical carrier signal at 1550 nm is propagating. The change in refractive index is controlled by the modulator driver circuit. In this article, an asymmetric circuit for anode and cathode terminals have been implemented. It is desired that cathode terminal signals should give full swing to keep P N junction is reversed bias; however, the anode terminal voltage should not increase above to build-in-potential of 0.8V. These conditions have been observed in Fig. 6(b) in which red colour curve shows the pulse signal with a 5GHz signal. The cathode terminal voltage follows the pulse signal. In contrast, the anode terminal voltage follows pulse but less than 0.8V to keep the PN junction reverse biased condition.

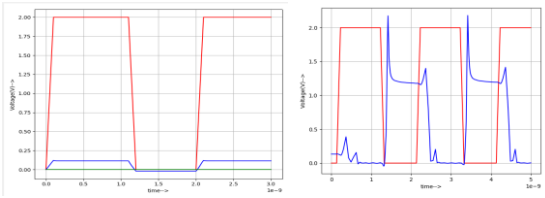

Fig. 6 (a). The transient response of anode and cathode drivers respectively implemented on eSim.

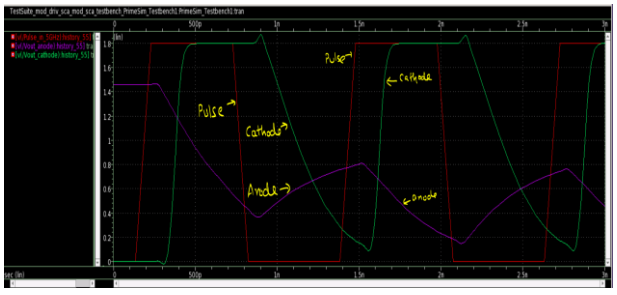

Fig.6 (b). The transient response of anode (violet color curve) and cathode (gree color curve) drivers with respect to change in pulse (red color curve), respectively implemented on Synopsys

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[5] https://www.klayout.de/intro.html (visited on 27 Feb. 2022)

[6] https://github.com/SiEPIC/SiEPIC_EBeam_PDK (visited on 27 Feb. 2022)

Resources:

1. Netlist
2. Log file generated