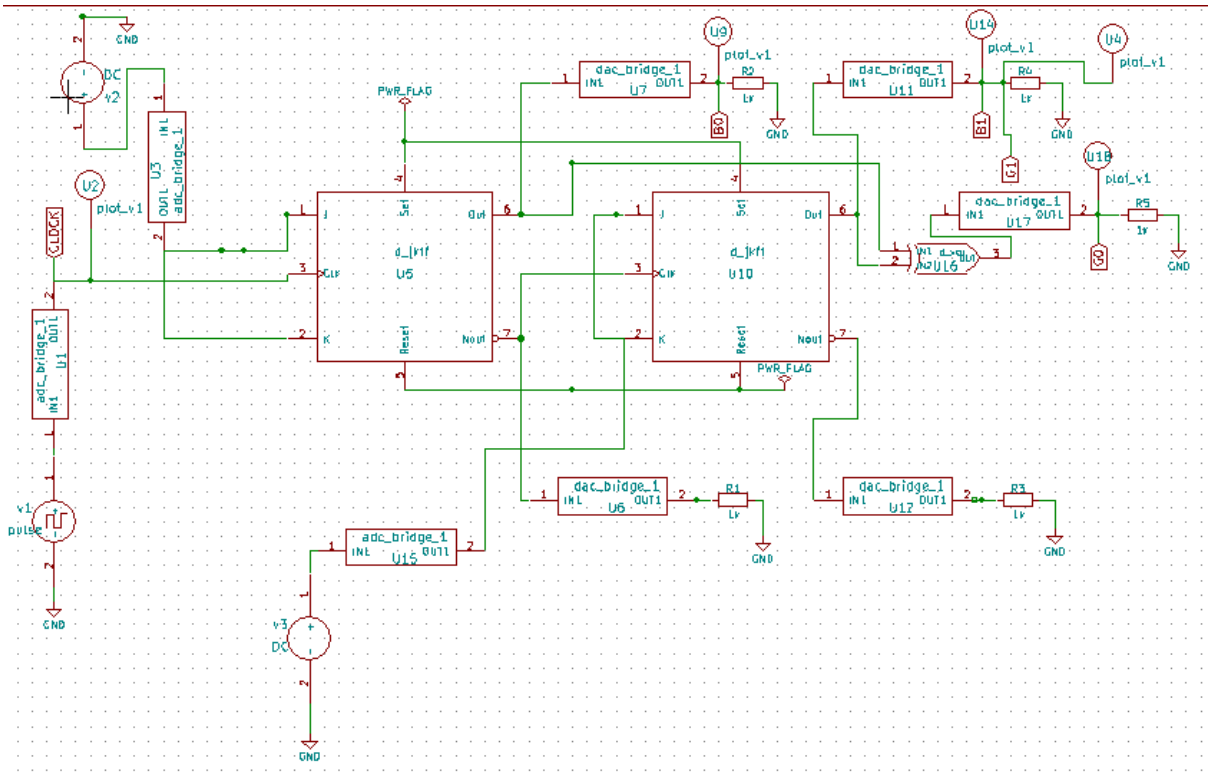
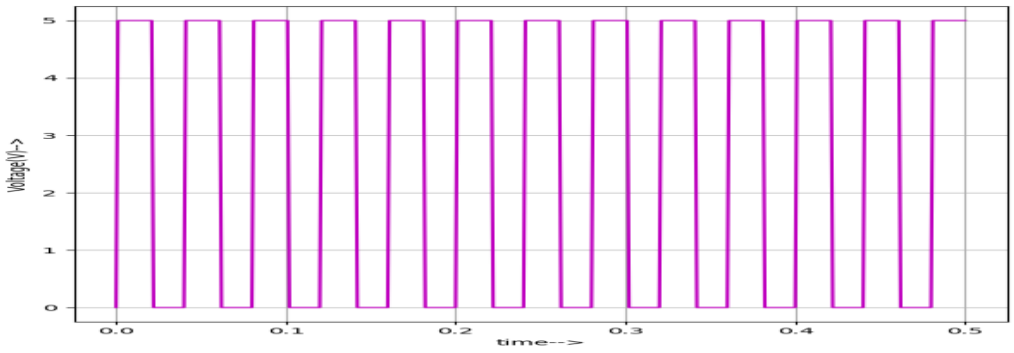
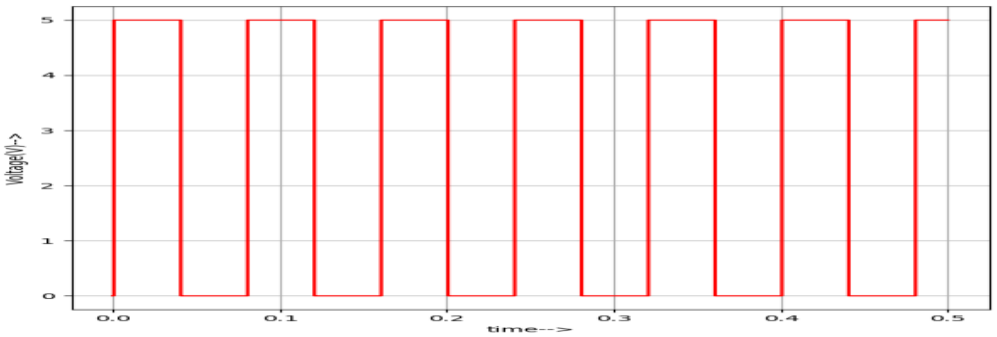


Fig. 2-bit Asynchronous Counter followed by the 2-bit Binary to Gray Code Circuit Schematic drawn on eSim

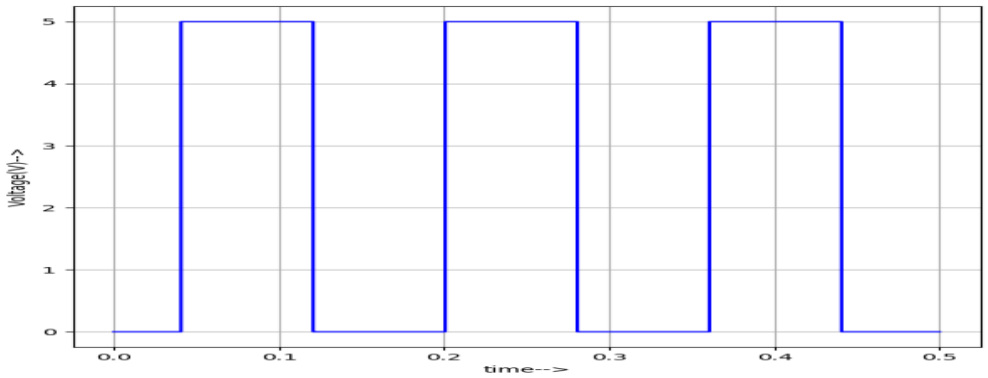
Timing Diagram of two bit asynchronous counter followed by the 2-bit binary to gray code converter timing signals.



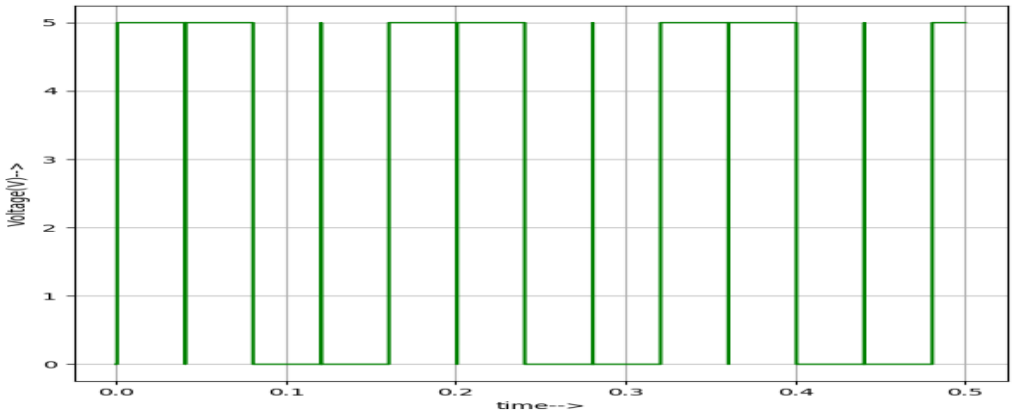
(a): Clock applied to first JK Flip-flop



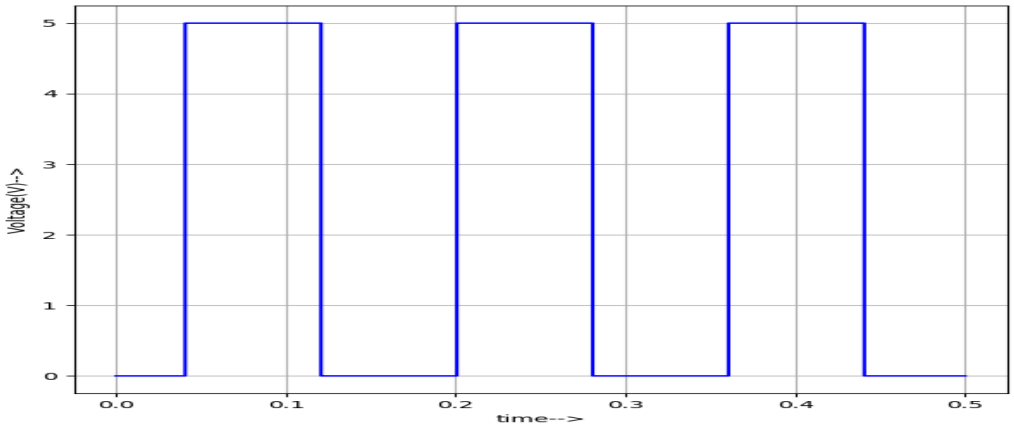
(b): LSB (Bo or Q0) is the output of 2-bit asynchronous counter from first JK Flip-flop



(c): MSB (B1or Q1) is the output of the 2-bit asynchronous counter from the second JK Flip-flop



(d): LSB (Go) is the output of 2-bit Binary to Gray Code Converter i.e. B0 XOR B1)



(e): MSB (G1) is the output of 2-bit Binary to Gray Code Converter i.e. G1 =B1)