# National Sun Yat-Sen University
# ASSEMBLY LANGUAGE AND MICROCOMPUTER
# Homework #2
# Tested on 10/28/2021

1. Find any two processors names of ARM processor cores.

2. List six ARM exception modes.

3. List the procedures the ARM system will take to handle the exceptions.

4. Explain what load-store architecture means.

5. Explain what 3-address instructions means.

6. Explain what ***word-alignment*** means.

7. How many ARM's visible registers in total ?

8. Assume r1=#&00201080 and r2=#&0000FFAB, find out the values of r0 in binary format for the following instructions:
   (a) ADD r0, r1, r2
   (b) SUBS r0, r2, r1
   (c) BIC r0, r1, r2
   (d) ANDS r0, r2, #12
   (e) ADD r0, r1, r2, ASR #2

9. Suppose r0=0x0, r1=0xF0000001, r2=0xF0000000, C=1, N=0, Z=0, V=0, please find out the corresponding resulting r0 value of the following instructions. You should also provide the resulting conditional code value (C N Z V).
   (a) ADDS r0, r1, r2.
   (b) ADC r0, r1, r2.
   (c) SUBS r0, r1, r2.
   (d) SBC r0, r1, r2.
   (f) BIC r0, r1, r2.
   (h) ADD r0, r1, r2, LSL #1
   (i) CMP r1, r2
   (j) MOV r0, r2 RRX.

10. Specify a single ARM instruction to implement each of the following statements:
    (a) r0 = 63*r1 (r1 can be divided by 4.)
    (b) r2=mem16[r1]; r1=r1-8 ;
    (c) Compare registers r6 and r9 only if Z is clear.

11. Write two short ARM codes to implement the following C statement. The first one cannot use instructions with conditional execution, but can use conditional branches. The second code can use ARM instructions with conditional execution without restriction. You should use as fewer number of instructions as possible for both implementations.

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if ((r1>r2) && (r3<r4)) r5--;
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12. Describe the difference between ADR and ADRL

13. What should we write in the ARM program if we want to set r1 to the value of 0x87654321?

14. For each of the following multiple register store instructions, write a short code to restore these register values by loading the data back from the memory. You should try to use the minimum number of instructions.
    (a) STMIA r9!, {r0, r5, r1}
    (b) STMIB r9, {r5, r1, r0}
    (c) STMED r9!, {r0, r1, r5}
    (d) STMED r9, {r5, r0, r1}

15. Discuss what kind of ARM instruction that would typically be placed at memory address 0x4 in an embedded system based on an ARM7TDMI processor.

16. Tell whether or not the following constants can be loaded into an ARM7TDMI register without creating a literal pool and using only a single instruction:
    (a) 0x12340000
    (b) 0x77777777
    (c) 0xFFFFFFFF
    (d) 0xFFFFFFFE