**Lab Report 5**

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Group 8

# Aim:-

1. Making a SR latch.

B) Making a JK Master-Slave Flip-Flop.

C) Making a 4-bit Up-Down Counter.

Part A (SR Latch)

Electronic Components Used :

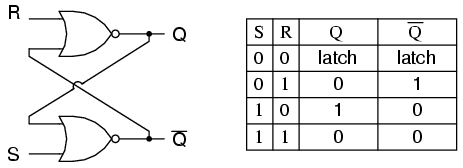
Arduino Uno, Breadboard, Quad Gate NOR gate(74HC02), two LEDs, two 1 KΩ resistors, Push Button, and connecting wires.

### Reference Circuit:-

Diagram

Description automatically generated

### PC: https://www.allaboutcircuits.com/textbook/digital/chpt-10/s-r-latch/



(Even though 11 is a forbidden state we get a stable output of 00, latch is considered to be the undefined random state)

This circuit has two inputs S & R and two outputs Q(t) & Q’(t). The upper NOR gate has two inputs R & complement of present state, Q’(t) and produces next state, Q(t+1).Similarly, the lower NOR gate has two inputs S & present state, Q(t) and produces complement of next state, Q’(t+1). We know that a 2-input NOR gate produces an output, which is the complement of another input when one of the input is ‘0’.

Similarly, it produces ‘0’ output, when one of the input is ‘1’.

If S = 1, then next state Q(t+1) will be equal to ‘1’ irrespective of present state, Q(t) values.

If R = 1, then next state Q(t+1) will be equal to ‘0’ irrespective of present state, Q(t) values.

At any time, only of those two inputs should be ‘1’. If both inputs are ‘1’, then the next state Q(t+1) value is undefined.

### Procedure: -

1. Drag The Required Components onto the Workspace fin Tinker CAD and make the connections according to the Reference Diagram.
2. Start Simulation, and press the Push Button to Set the initial state of Q as 0, so as to nudge it to start the simulation time on Tinker CAD.
3. Input to be fed into Serial Monitor

### Conclusion:-

Thus, the Hypothesis is true. The Latch will operate correctly as long as the forbidden Input 11 is not entered.

Link: https://www.tinkercad.com/things/iyE3PAsXycX-5-a/editel?sharecode=oIrjL1k4h25cvfMrLp-j-zjiAj2TuM9KqxXQaMua\_4Q

**Part B** (JK Master Slave Flip-Flop)

Electronic Components Used:-

Arduino Uno R3, Breadboard,Hex Inverter(74HC04), Triple Input

NAND Gate(74HC10), Two Double Input NAND gate ICs(74HC00),LEDs,1 KΩ Resistors, 470 KΩ Resistor, Clock IC(555),Capacitor(2µF),PushButtons and Connecting Wires.

Reference Circuit:

Diagram

Description automatically generated

(The JK flip-flop internals are shown in the image below)

PC: Lab 5 pdf

Diagram

Description automatically generated

Diagram

Description automatically generated

### Procedure: -

Set up the Master latch then set up the Slave latch

Test if they work

Forward outputs from master latch to slave latch and test the combined result.

Send the outputs of slave latch back to master latch and implement the nudge switch.

Start Simulation and Press the Nudge Pushbuttons to set the master and Slave Latches initially.

Enter desired input in the Serial Monitor.

Observation:

(PC: Lab 5 pdf)

Table

Description automatically generated

Therefore, The State Table of JK Master-Slave Latch is as follows.

Link: https://www.tinkercad.com/things/h5pPF8AUBYA-copy-of-5b/editel?sharecode=9vy4QgccKZiQFEUC4k3Lmb4mchsA-TzqyeEG3oI0\_oo

## **Part C** (**4 Bit Up-Down Counter )**

Electronic Components Used:-

Arduino Uno R3, Breadboard, 1 KΩ Resistors, LEDs and Connecting wires.

Reference Circuit:

Diagram

Description automatically generated

### Procedure: -

Drag down the required Components to the Workspace in TinkerCAD and make Connections According to The reference

Circuit.

Input The code into the Starter Code Space Provided and Run Simulation.

Observation:

The ripple counter first goes UP from 0 (0000) to 15 (1111), then goes DOWN from 15 to 0, then goes UP, and this cycle repeats until the simulation is stopped.

Conclusion:

4 bit Up-Down Ripple Counter is now working

Link: https://www.tinkercad.com/things/aFsvqeJxxoU-5c/editel?sharecode=94lUl-1ErxvqHI\_7ryvFBcvXkIGRWgwBKSzMnRbeSoM