MINOR PROJECT REPORT

ON

QUANTITATIVE ANALYSIS OF SHORT CHANNEL EFFECT IN FETS

SUBMITTED IN PARTIAL FULFILLMENT FOR THE AWARD OF DEGREE OF

BACHELOR OF TECHNOLOGY

IN

ELECTRONICS AND COMMUNICATION ENGINEERING

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December, 2023

CERTIFICATE

This is to certify that the minor project report entitled, "**QUANTATIVE ANALYSIS OF SHORT CHANNEL EFFECTS IN FETs"** submitted by Aakarshita Srivastava and Aryan Aggarwal of Bachelor of Technology Degree in Electronics and Communication Engineering of the Jaypee Institute of Information Technology, Noida has been carried out by them under my supervision and guidance. This work has not been submitted partially or wholly to any other University or Institute for the award of any other degree or diploma.

Signature of Supervisor

Name of the Supervisor: Dr. Archana Pandey

Date: 1st December, 2023

DECLARATION

We hereby declare that this submission is our own work and that, to the best of our knowledge and beliefs, it contains no material previously published or written by another person nor material which has been accepted for the award of any other degree or diploma from a university or other institute of higher learning, except where due acknowledgment has been made in the text.

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ABSTRACT

The relentless pursuit of improved performance, power efficiency, and compactness has compelled the semiconductor industry to continually reduce the size of MOSFETs, pushing the boundaries of what is technologically feasible. However, in this pursuit of miniaturization lies a formidable challenge - the emergence and intensification of **Short Channel Effects** (SCEs). **As transistors continue to shrink in size, the impact of SCEs on device performance, power consumption, and reliability has become more pronounced**. To address this issue, it is crucial to conduct a comprehensive quantitative analysis of these effects and their implications using Sentaurus TCAD software.

ACKNOWLEGEMENT

We would like to place on record my deep sense of gratitude to **Dr. Archana Pandey**, ECE faculty at Jaypee Institute of Information Technology, India for her generous guidance, help, inspiration and constructive suggestions. New ideas and direction from her made it possible for us to sail through various areas of our project which further helped us to make it better.

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INTRODUCTION

1.1 Field Effect Transistor

The concept of the field effect transistor is based around the concept that charge on a nearby object can attract charges within a semiconductor channel. It essentially operates using an electric field effect - hence the name. The FET consists of a semiconductor channel with electrodes at either end referred to as the drain and the source. A control electrode called the gate is placed in very close proximity to the channel so that its electric charge is able to affect the channel. In this way, the gate of the FET controls the flow of carriers (electrons or holes) flowing from the source to drain. It does this by controlling the size and shape of the conductive channel. The semiconductor channel where the current flow occurs may be either P-type or N-type. This gives rise to two types or categories of FET known as P-Channel and N-Channel FETs. In addition to this, there are two further categories. Increasing the voltage on the gate can either deplete or enhance the number of charge carriers available in the channel. As a result, there are enhancement mode FET and depletion mode FETs.

1.1.1 Field Effect Transistor: History

Before the first FETs were introduced into the electronic components market, the concept of these semiconductor devices had been known for a number of years. There had been many difficulties in realising this type of device and making it work. Some of the early concepts for the field effect transistor were outlined in a paper by Lilienfeld in 1926, and in another paper by Heil in 1935. The next foundations were set in place during the 1940s at Bell Laboratories where the semiconductor research group was set up. This group investigated a number of areas pertaining to semiconductors and semiconductor technology, one of which was a device that would modulate the current flowing in a semiconductor channel buy placing an electric field close to it. During these early experiments, the researchers were unable to make the idea work, turning their ideas to another idea and ultimately inventing another form of semiconductor electronics component: the bipolar transistor. After this much of the semiconductor research was focussed on improving the bipolar transistor, and the idea for a field effect transistor was not fully investigated for some while. Now FETs are very widely used, providing the main active element in many integrated circuits. Without these electronic components electronics technology would be very different to what it is now.

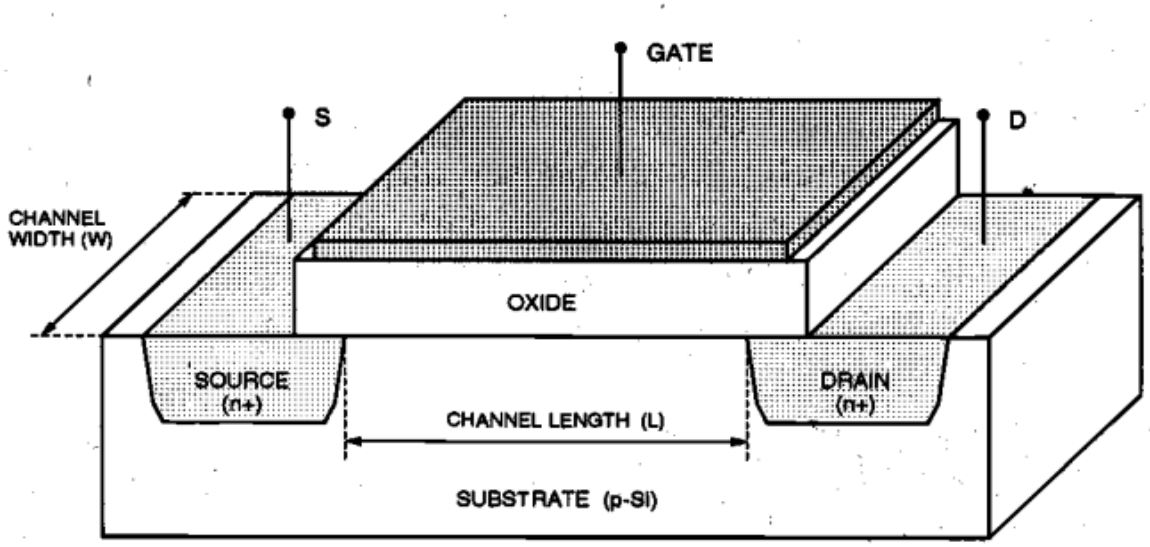
1.2 Mos Transistor

The MOS Field Effect Transistor (MOSFET) is the fundamental building block of MOS and CMOS digital integrated circuits. Compared to the bipolar junction transistor (BJT), the MOS transistor occupies a relatively smaller silicon area, and its fabrication involves fewer processing steps. These technological advantages, together with the relative simplicity of MOSFET operation, have helped make the MOS transistor the most widely used switching device in LSI and VLSI circuits.

1.2.1 The Metal Oxide Semiconductor (MOS) Structure

The basic structure of an n-channel MOSFET is shown in Fig. 3.8. This four-terminal device consists of a p-type substrate, in which two n+ diffusion regions, the drain and the source, are formed. The surface of the substrate region between the drain and the source is covered with a thin oxide layer, and the metal (or polysilicon) gate is deposited on top of this gate dielectric. The midsection of the device can easily be recognized as the basic MOS structurewhich was examined in the previous sections. The two n+ regions will be the current-conducting terminals of this device. Note that the device structure is completely symmetrical with respect to the drain and source regions; the different roles of these two regions will be defined only in conjunction with the applied terminal voltages and the direction of the current flow.

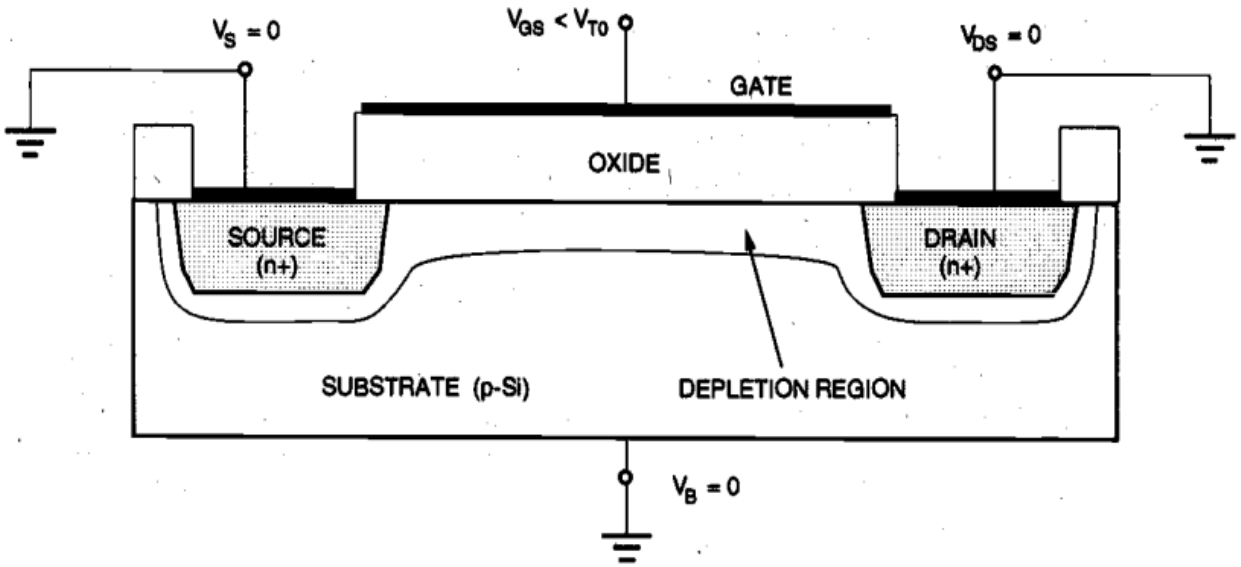
A conducting channel will eventually be formed through applied gate voltage in the section of the device between the drain and the source diffusion regions. The distance between the drain and source diffusion regions is the channel length L, and the lateral extent of the channel (perpendicular to the length dimension) is the channel width W.



1.2.2 The MOS System under External Bias

Assume that the substrate voltage is set at VB = 0, and let the gate voltage be the controlling parameter. Depending on the polarity and the magnitude of VG, three different operating regions can be observed for the MOS system: accumulation, depletion, and inversion. If a negative voltage VG is applied to the gate electrode, the holes in the p-type substrate are attracted to the semiconductor-oxide interface. The majority carrier concentration near the surface becomes larger than the equilibrium hole concentration in the substrate; hence, this condition is called carrier accumulation on the surface . While the hole density near the surface increases as a result of the applied negative gate bias, the electron (minority carrier) concentration decreases as the negatively charged electrons are pushed deeper into the substrate.

Now consider the next case in which a small positive gate bias VG is applied to the gate electrode. Since the substrate bias is zero, the oxide electric field will be directed towards the substrate in this case. The majority carriers, i.e., the holes in the substrate, will be repelled back into the substrate as a result of the positive gate bias, and these holes will leave negatively charged fixed acceptor ions behind. Thus, a depletion region is created near the surface. Note that under this bias condition, the region near the semiconductor-oxide interface is nearly devoid of all mobile carriers.



The simplest bias condition that can be applied to the n-channel enhancement-type MOSFET is shown in Fig: 1.2 The source, the drain, and the substrate terminals are all connected to ground. A positive gate-to-source voltage VGS is then applied to the gate in order to create the conducting channel underneath the gate. With

this bias arrangement, the channel region between the source and the drain diffusions behaves exactly the same as for the simple MOS. For small gate voltage levels, the majority carriers (holes) are repelled back into the substrate, and the surface of the p-type substrate is depleted. Since the surface is devoid of any mobile carriers, current conduction between the source and the drain is not possible.

1.3 MOSFET Scaling and Small-Geometry Effects

The design of high-density chips in MOS VLSI (Very Large-Scale Integration) technology requires that the packing density of MOSFETs used in the circuits is as high as possible and, consequently, that the sizes of the transistors are as small as possible.

The reduction of the size, i.e., the dimensions of MOSFETs, is commonly referred to as scaling. It is expected that the operational characteristics of the MOS transistor will change with the reduction of its dimensions. Also, some physical limitations eventually restrict the extent of scaling that is practically achievable.

There are two basic types of size-reduction strategies: full scaling (also called constant-field scaling) and constant voltage scaling.

1.3.1 Full Scaling (Constant-Field Scaling)

This scaling option attempts to preserve the magnitude of internal electric fields in the MOSFET, while the dimensions are scaled down by a factor of S. To achieve this goal, all potentials must be scaled down proportionally, by the same scaling factor. Note that this potential scaling also affects the threshold voltage Vo.

Quantity	Before Scaling	After Scaling
Channel length	L	$L' = L/S$
Channel width	W	$W' = W/S$
Gate oxide thickness	t_{ox}	$t_{ox}' = t_{ox}/S$
Junction depth	x_j	$x_j' = x_j/S$
Power supply voltage	V_{DD}	$V_{DD}' = V_{DD}/S$
Threshold voltage	V_{T0}	$V_{T0}' = V_{T0}/S$
Doping densities	N_A N_D	$N_A' = S \cdot N_A$ $N_D' = S \cdot N_D$

1.3.2 Constant-Voltage Scaling

While the full scaling strategy dictates that the power supply voltage and all terminal voltages be scaled down proportionally with the device dimensions, the scaling of voltages may not be very practical in many cases. In particular, the peripheral and interface circuitry may require certain voltage levels for all input and output voltages, which in turn would necessitate multiple power supply voltages and complicated level shifter arrangements. For these reasons, constant-voltage scaling is usually preferred over full scaling.

Quantity	Before Scaling	After Scaling
Dimensions	W, L, t_{ox}, x_j	reduced by S $(W' = W/S, \ldots)$
Voltages	V_{DD}, V_T	remain unchanged
Doping densities	N_A, N_D	increased by S^2 $(N_A' = S^2 \cdot N_A, \ldots)$

In constant-voltage scaling, all dimensions of the MOSFET are reduced by a factor of S, as in full scaling. The power supply voltage and the terminal voltages, on the other hand, remain unchanged. The doping densities must be increased by a factor of s2 in order to preserve the charge-field relations.

1.4 Short Channel Effects

As a working definition, a MOS transistor is called a short-channel device if its channel length is on the same order of magnitude as the depletion region thicknesses of the source and drain junctions. Alternatively, a MOSFET can be defined as a short-channel device if the effective channel length approximately equal to the source and drain junction depth x. The short-channel effects that arise in this case are attributed to two physical phenomena:

1. **the limitations imposed on electron drift characteristics in the channel, and**
2. **the modification of the threshold voltage due to the shortening channel length.**

Note that the lateral electric field Ey along the channel increases, as the effective channel length is decreased. While the electron drift velocity Vd in the channel is proportional to the electric field for lower field values, this drift velocity tends to saturate at high channel electric fields. For channel electric fields of E = 105 V/cm and higher, the electron drift velocity in the channel reaches a saturation value of about vd(sat) = 107 'cm/s. This velocity saturation has very significant implications upon the current-voltage characteristics of the short-channel MOSFET. Consider the saturation-mode drain current, under the assumption that carrier velocity in the channel has already reached its limit value. The effective channel length Lef will be reduced due to channel-length shortening.

Carrier velocity saturation actually reduces the saturation-mode current below the current value predicted by the conventional long-channel current equations. The current is no longer a quadratic function of the gate-to-source voltage VGS, and it is virtually independent of the channel length. Also note that under these conditions, the device is defined to be in saturation when the carrier velocity in the channel approaches about 90% of its limit value.

In short-channel MOS transistors, the carrier velocity in the channel is also a function of the normal (vertical) electric-field component Ex. Since the vertical field influences the scattering of carriers (collisions suffered by the carriers) in the surface region, the surface mobility is reduced with respect to the bulk mobility.

We consider the modification of the threshold voltage due to short-channel effects. The threshold voltage expression was derived for a long-channel MOSFET. Specifically, the channel depletion region was assumed to be created only by the applied gate voltage, and the depletion regions associated with the drain and source pn-junctions were neglected. The shape of this gate-induced bulk (channel) depletion region was assumed to be rectangular, extending from the source to the drain. In short-channel MOS transistors, however, the n' drain and source diffusion regions in the p-type substrate induce a significant amount of depletion charge; consequently, the long-channel threshold voltage expression derived earlier overestimates the depletion charge supported by the gate voltage. The threshold voltage value found is therefore larger than the actual threshold voltage of the short-channel MOSFET.

Chapter-2
LITERATURE SURVEY

2.1 Threshold Voltage Calculation in Ultrathin-Film SOI MOSFETs Using the Effective Potential

2.1.1 Abstract

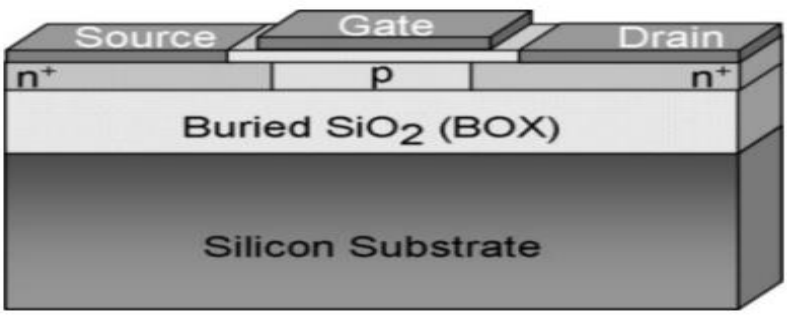
In this paper, we include this effective potential model in Monte Carlo calculations of the threshold voltage of ultrathin SOI MOSFETs. We find that the effective potential recovers the expected trend in threshold voltage shift with decreasing silicon thickness, down to a thickness of approximately 3 nm.

2.1.2 Introduction

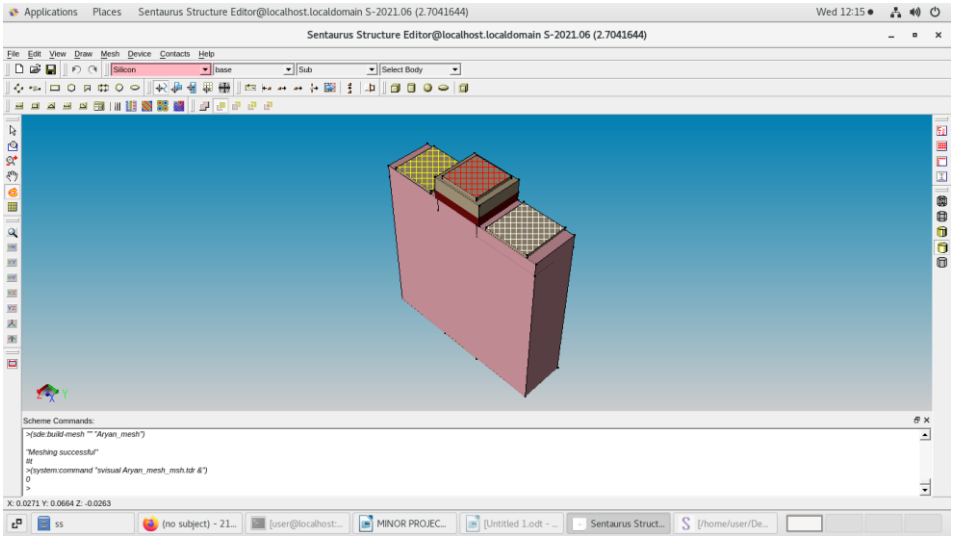
It is well known that simulations of current bulk MOSFETs need to incorporate some type of method to account for the quantum mechanical effects of carrier confinement in the inversion layer, which influence the gate capacitance and threshold voltage [1], [2]. Similar quantum effects are seen in silicon-on-insulator (SOI) MOSFETs, especially such devices built on ultrathin SOI layers. In addition to the inversion layer confinement, the carriers in these thin SOI layers are confined by the gate and buried-oxide (BOX) interfaces.

2.1.3 Structure Information

The gate length was taken to be 40 nm, the source and drain lengths were 50 nm each, the gate oxide was 7 nm with a 2-nm source and drain overlap, the channel doping was constant at NA=1 x 10^17cm^-3, the source/drain doping was constant at 2 x 10^19 cm^-3, and there was a 10 nm spacer region between the gate and the source/drain contacts. The silicon film thickness was varied over range of 2–10 nm for different simulations.



SOI device schematic.



2.1.4 Results

The silicon film thickness decreased below a certain point, the threshold voltage should increase, due to an elevation in the ground-state energy in the channel. We calculated the threshold voltage for a range of silicon film thicknesses and compared the results with the data.

2.1.5 Conclusion

We have examined the use of the effective potential in calculating the threshold voltage over a range of film thicknesses. We find that using the inversion layer density to determine the threshold voltage provides smoother results with less simulation time, though this method may not be applicable to all situations. Also, with a thin enough silicon film, the confining potential is strongly influenced by the potential well formed between the gate and buried-oxide layers. In these cases, we find that the effective potential provides reasonable results for the threshold voltage for silicon films as thin as 3 nm. Below this thickness, however, the confinement effects from the oxide layers surpasses the confinement from the inversion layer, and the effective potential simulations show a higher threshold voltage than calculations.

2.1.6 Reference

We extracted our basic MOS structure from this paper. The dimensions of each Gate, Drain, Source and oxide layer of our structure are taken accordingly. The overlap between gate source and drain mentioned is also taken into account. We made our structure design by taking into account all these parameters and then decided the x, y, z coordinates of the structures accordingly.

2.2 Design, Simulation and Characterization of 50nm p-well MOSFET Using Sentaurus TCAD Software

2.2.1 Abstract

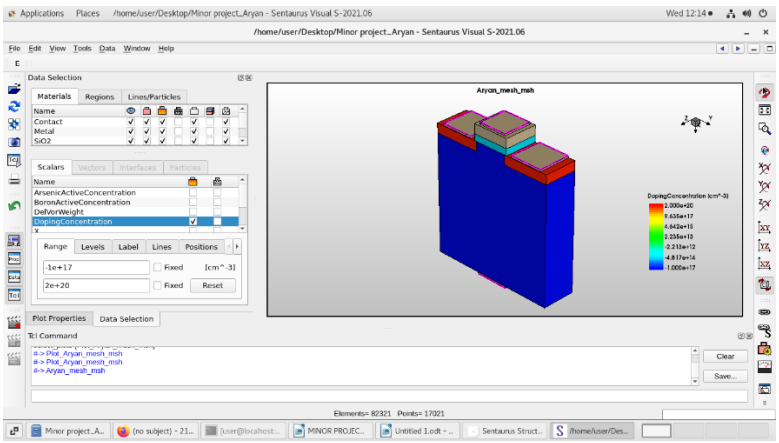
Device 50nm p-well MOSFET was designed, developed and optimized based on 90nm recipe using Sentaurus TCAD Software. In this project, there are two sub-programs used which are Sentaurus Process and Sentaurus Device. Sentaurus Process is a simulation process which in designing the semiconductor technology. While Sentaurus Device work as a device simulator to find the characteristic for each semiconductor design.

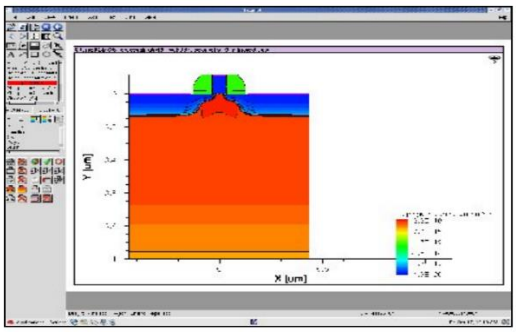
2.2.2 Introduction

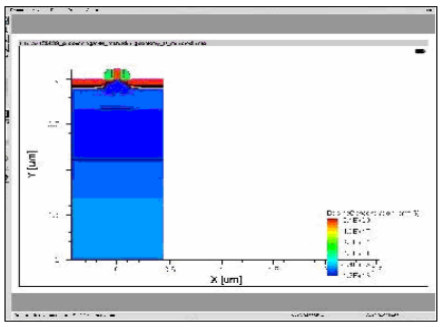
The MOS (Metal Oxide Semiconductor) transistor is the most promising active component for silicon VLSI circuits at the present time. There are a number of reasons for this choice. First, it is self – isolating, so that the devices can placed side by side on a chip without the needs for providing isolation tubs. As a result, it is considerably smaller than its bipolar counterpart, and requires less processing steps [1]. Furthermore, it can be made in bulk silicon, thus avoiding the costly epitaxial growth. However, epitaxial structures are increasingly used in high – density application, to minimize latch–up problems, caused by devices interactions through a common substrate.

2.2.3 Designing

Designing p-well CMOS semiconductor must go through several processes. The designing process involves modifying the recipe of MOSFET 90nm to MOSFET50nm. The first process is the simulation of fabrication process 50nm MOSFET which is done using Sentaurus Process. Then, the process for structure and mesh are done onto fabricated MOSFET using Sentaurus Structure Editor. The final step is electrical testing using Sentaurus Device.







2.2.4 Result and Analysis

The results for process and device simulation are shown in figure 1-6. The graphs display in two dimensions (2D) in INSPECT and TECPLOT SV tools in Sentaurus TCAD.

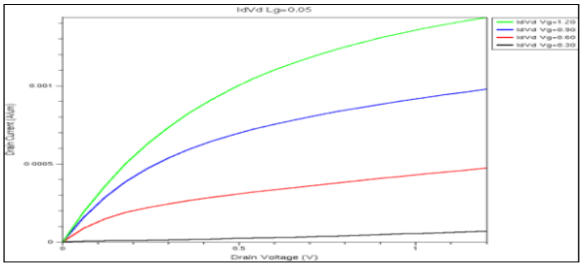


Figure 5: I_D (Drain Current)-V_D (Drain Voltage) graph for 50nm NMOS transistor

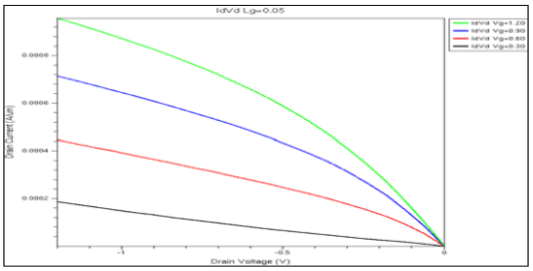


Figure 6: I_D (Drain Current) -V_D (Drain Voltage) graph for 50nm PMOS transistor

2.2.5 Conclusion

The development of 50nm p-well CMOS transistor using Sentaurus TCAD software is successful. The design of 50nm p-well MOSFET transistor is done in two main parameters are obtained and analysed which are Threshold Voltage (Vth), Drain Saturation Current (Idsat) and Leakage Current (Ioff).

2.2.6 Reference

We used this paper to analyse the characteristics of Sentaurus TCAD Software. It described all the steps of Doping and Meshing. It also showed us the diverse use of Sentaurus TCAD as well as the basic structure of Mosfet. We saw different plots in the paper to get an insight of how Sentaurus TCAD would work.

2.3 Gate Length Effect on NMOS Electrical Characteristics Using TCAD

2.3.1 ABSTRACT

The concept of device scaling in silicon transistor has consistently resulted in better device density and performance. In conventional MOSFETs, control of Iofffor scaled devices requires very thin gate dielectrics and high doping concentrations. The industry roadmap for CMOS technology predictsphysical limitations as well as practical technological will become barriers to continuous scaling. As the downscale of CMOS technology approaches physical limitations, the need arises for alternative device structures. NMOS traditionally has been the dominant MOS technology. Relative to CMOS, NMOS shows higher speed, higher power technology with lower cost and higher functional density.

2.3.2 Introduction

Silicon CMOS has emerged as the predominant technology in semiconductor industry. It has been continuously scaled down in terms of size but higher capacity and complexity. As device size as came into nanoscale regime, therefore novel structure is needed. Conventional MOSFET also suffers from higher leakage current, short channel effect and doping uniformity. NMOS structure is proposed in order to reduce the leakage current and offer better handling of short channel effect. The purpose of this paper is to show NMOS structure is able to eliminate the problems in conventional MOSFET and to prepare for nanoscale device. In this paper, the effect the gate length on the transistor characteristicis shown by means of simulation work using the Sentaurus TCAD software.

2.3.3 Experimental Procedure

MOSFETs operate in such a way that the current from the source to drain is carried by electrons (NMOS), by holes (PMOS) or by both electrons and holes in the case of complementary MOSFET (CMOS). A voltage is applied to the gate that ‘inverts’ the polarity of the carriers and produces electrons near the oxide-semiconductor interface. The gate length is one of the most critical parameters controlling device performance. The body or substrate of a MOSFET can also be contacted and a bias applied to it.

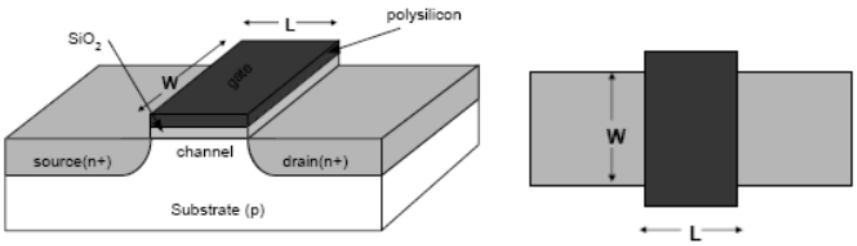


FIGURE 1 The side and top view of n-type MOSFET structure

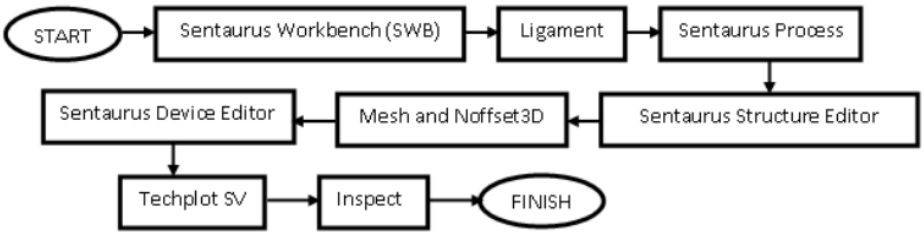
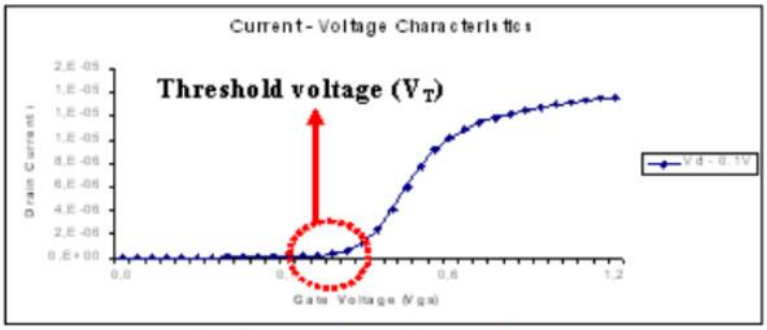


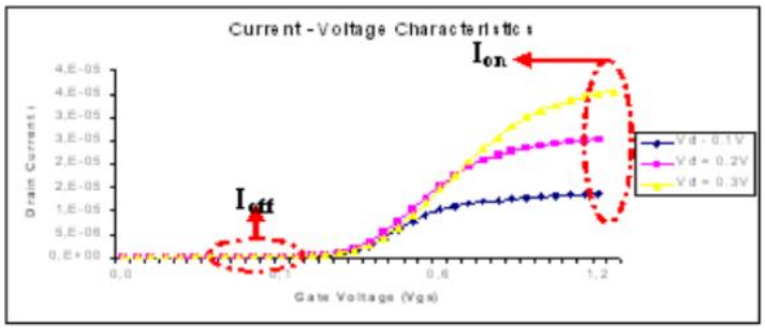
FIGURE 2 Flow chart of n-channel MOSFET simulation process

2.3.4 Result and Analysis

The current-voltage (Id-Vgs) characteristics and subthreshold curves for NMOS device of channel length Lgat30nm, 50nm and 100nm respectively with uniform boron doping concentration of 1012cm-3to 1020cm-3. The measured threshold voltage is shown three curves represent simulated output at Vds= 0.1V, 0.2Vand 0.3V separately for gate length 30nm. In Vgs sweeps from 0V to 1.2V which produced Ion–Ioff current ratio, subthreshold swing and leakage current. All these characteristics are the same for the gate length at 50nm and 100nm respectively.



(a) Threshold voltage at $V_d - 0.1V$



(b) Current-Voltage ($I_d - V_{gs}$) characteristics of 30nm

2.3.5 References

We referred this paper for the understanding of basic structure of MOSFET and also analysing the Sentaurus TCAD software. The flowchart shown describes all the steps of the software.

Chapter-3

REQUIREMENT ANALYSIS

3.1 Problem Statement

Short Channel Effects (SCEs) have become a significant challenge in the design and operation of Field-Effect Transistors (FETs) in modern semiconductor technology. As transistors continue to shrink in size, the impact of SCEs on device performance, power consumption, and reliability has become more pronounced. To address this issue, it is crucial to conduct a comprehensive quantitative analysis of these effects and their implications. The relentless pursuit of smaller and more powerful Field-Effect Transistors (FETs) has driven the semiconductor industry to the cutting edge of technology. As channel lengths in FETs continue to shrink to meet the demands of ever more compact and energy-efficient electronic devices, the emergence of Short Channel Effects (SCEs) has become a paramount concern. These SCEs, encompassing phenomena such as Drain-Induced Barrier Lowering (DIBL), Subthreshold Slope Degradation, and increased leakage currents, pose a substantial challenge to the performance, reliability, and power efficiency of FET-based electronic systems.

Short Channel Effects, as the name implies, are most pronounced in transistors with shorter channel lengths. As semiconductor technology advances, the transition to smaller channel lengths is unavoidable to meet the insatiable appetite for faster and more power-efficient electronics. However, as channel lengths decrease, the adverse impact of SCEs becomes increasingly pronounced.

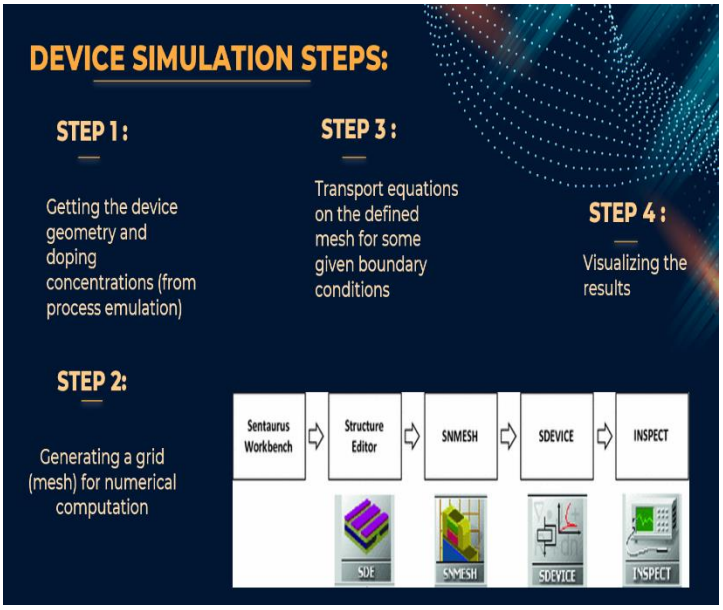
3.2 Methodology

1. A comprehensive review of existing research on Short Channel Effects in FETs to establish a baseline understanding.
2. Creating a quantitative model that describes the behavior of SCEs in FETs based on physical principles.
3. Design and fabricate FET devices of varying channel lengths.
4. Measure and analyze the performance of fabricated devices, focusing on SCEs.
5. Compare experimental results with the theoretical model and derive insights into the magnitude and impact of SCEs.

3.3 Software Used

SENTAURUS TCAD (Technology Computer-Aided Design) is a widely used software tool for simulating and designing semiconductor devices and processes. It is developed by Synopsys and provides a comprehensive suite of tools for device simulation, process simulation, and electrical analysis.

1. **Semiconductor Device Simulation:** Sentaurus TCAD is primarily used for simulating the behavior of semiconductor devices, such as transistors, diodes, and other components. It allows engineers and researchers to study device characteristics and performance under various conditions.
2. **Process Simulation**: It also includes process simulation capabilities, which enable users to model and analyse the fabrication processes used to create semiconductor devices.



CONCLUSION

In conclusion, the quantitative analysis conducted in this project has provided valuable insights into the short channel effects in Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). The fabrication and experimental methodology allowed for a systematic examination of the impact of varying channel lengths on MOSFET performance. The results obtained through data analysis highlight the significance of short channel effects and their influence on device characteristics.

Our findings contribute to the existing body of knowledge on semiconductor devices, specifically in the context of MOSFETs. The observed correlations between short channel effects and device performance underscore the importance of addressing these effects in the design and fabrication of MOSFETs for optimal functionality.

As technology continues to advance, the knowledge gained from this study can inform future research and development efforts aimed at mitigating the challenges posed by short channel effects. The data presented here serve as a foundation for further exploration and innovation in semiconductor technology, paving the way for enhanced MOSFET designs and improved electronic devices.

In closing, this project has provided a comprehensive analysis of short channel effects in MOSFETs, offering a valuable contribution to the field. The insights gained underscore the need for ongoing research and optimization, ensuring the continued progress of semiconductor technology in the ever-evolving landscape of electronic devices.

FUTURE SCOPES

The quantitative analysis of short channel effects in FETs conducted in this project opens avenues for future research and development in several key areas:

1. Advanced Fabrication Techniques:

Explore novel fabrication techniques to further reduce short channel effects, such as advanced lithography methods and innovative materials for gate structures. Investigate the feasibility of emerging technologies, such as nanowire FETs, to overcome limitations associated with conventional approaches.

2. Device Scaling and Miniaturization:

Investigate the impact of continued device scaling on short channel effects as technology advances. Explore the challenges and potential solutions associated with miniaturizing FETs, considering the implications on device performance, power consumption, and reliability.

3. Material Engineering:

Investigate the use of alternative materials for FET components to mitigate short channel effects. Explore the potential of two-dimensional materials or engineered heterostructures to enhance device performance and reduce susceptibility to short channel effects.

4. Process Optimization:

Focus on refining process parameters during fabrication to minimize short channel effects. Investigate the influence of doping profiles, annealing conditions, and other process variables on the occurrence and severity of short channel effects.

5. Simulation and Modeling:

Develop advanced simulation and modeling techniques to predict and understand short channel effects in MOSFETs. Utilize these tools to explore virtual prototypes and optimize device designs before physical fabrication, enabling more efficient development cycles.

6. Power-Efficient Designs:

Investigate strategies for designing MOSFETs with reduced power consumption while maintaining optimal performance. This includes exploring low-power modes, energy-efficient architectures, and innovative circuit designs that mitigate the impact of short channel effects on overall power efficiency.

7. Integration with Emerging Technologies:

Explore the integration of MOSFETs with emerging technologies, such as quantum computing or neuromorphic computing. Investigate how short channel effects may manifest in these novel computing paradigms and develop strategies to address them effectively.

Addressing these future research directions will not only deepen our understanding of short channel effects in FETs but also contribute to the development of more robust and efficient semiconductor technologies for future electronic applications.

OUR CONTRIBUTION

Our collaborative efforts on the Quantitative Analysis of short channel effects in FETs project have been integral to its partial completion. Each team member played a distinct role, contributing expertise and dedication to different aspects of the project. The following outlines our individual contributions:

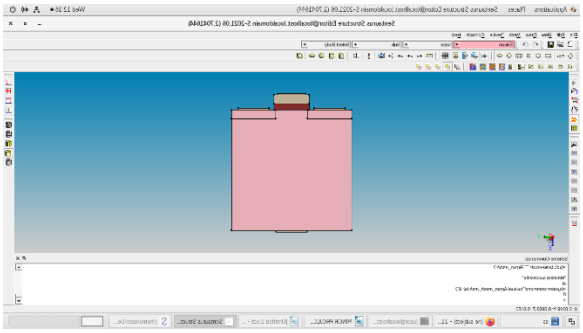
Aakarshita Srivastava (21102168):

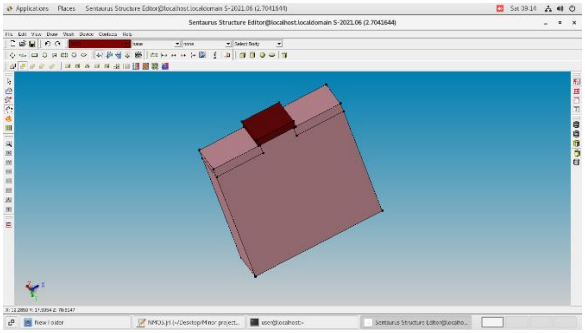
She took the charge of the project's conceptualization and MOSFETs structure phase. She was responsible for deciding the structure of MOSFETs and making the script file for the structure part of the device. She also played a crucial role in the understanding basic ideas of commands generated in TCAD.

```
;#############################################################################
;                                    PARAMETERS
;#############################################################################

;*****************************defined  parameters*******************************

(define Xbox 136)
(define Ybox 136 )
(define Zbox 36)

(define Xs 10)
(define Ys 50)

(define Xd 10)
(define Yd 50)

(define Yg 40)

(define Yl 2)

(define Tox -7)

(set! Xbox (/ Xbox 1e3))
(set! Ybox (/ Ybox 1e3))
(set! Zbox (/ Zbox 1e3))

(set! Xs (/ Xs 1e3))
(set! Ys (/ Ys 1e3))
```

```
(set! Xd (/ Xd 1e3))
(set! Yd (/ Yd 1e3))

(set! Yl (/ Yl 1e3))
(set! Tox(/  Tox 1e3))
(set! Yg(/ Yg 1e3))


; ****************************derived parameters*************************


(define Ygmin(- Yd  Yl))
(define Ygmax(+ Ygmin  Yg))
(define Ydmin(- Ybox Yd))
(define Xg(- Tox Xd))


;*****************************SUBSTRATE*********************************

(sdegeo:set-default-boolean "ABA")
"ABA"

(sdegeo:create-cuboid
        (position 0 0 0)
        (position Xbox Ybox Zbox)

"Silicon"  "region_SUBSTRATE"
)

;***********************************SOURCE*******************************

(sdegeo:set-default-boolean "ABA")
"ABA"

(sdegeo:create-cuboid
        (position 0 0 0)
        (position Xs Ys  Zbox)

 "Silicon"  "source"
)

;*********************************DRAIN**********************************
(sdegeo:set-default-boolean "ABA")
"ABA"

(sdegeo:create-cuboid
        (position 0  Ydmin  0  )
        (position Xd Ybox Zbox)
```

```
 "Silicon"  "drain"
)

;*****************************GATE OXIDE**********************************

(sdegeo:set-default-boolean "ABA")
"ABA"

(sdegeo:create-cuboid

        (position   0       Ygmin        0 )
        (position    Tox     Ygmax       Zbox   )

 "SiO2" "Gate Oxide"
)

;*********************************GATE ***********************************

(sdegeo:set-default-boolean "ABA")
"ABA"
(sdegeo:create-cuboid
        (position Tox  Ygmin  0  )
        (position Xg    Ygmax   Zbox)

 "Metal"  "Gate"
)
```





Aryan Aggarwal (21102151):

He spearheaded the implementation phase of the project. His responsibilities included defining the project scope, identifying key functionalities, and formulating the overall system architecture. He was responsible for making the contacts on the device and do

doping of various materials accordingly. His main responsibility is to generate mesh file of the decided structure.

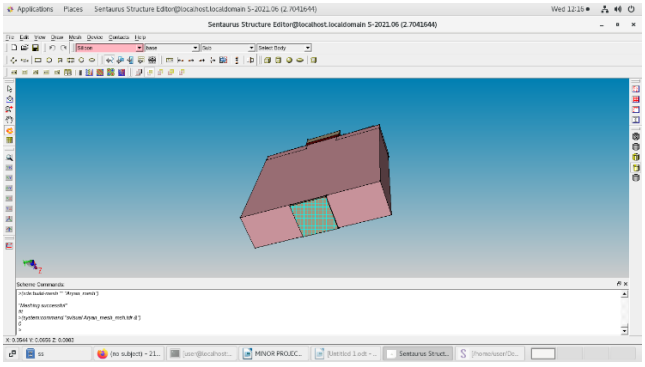
```
;*****************************DOPING*************************************

;*************************Source*************************

(sdedr:define-constant-profile "ConstantProfileDefinition_source" "ArsenicActiveConcentration"
2e+20)

(sdedr:define-constant-profile-region "ConstantProfilePlacement_source"
"ConstantProfileDefinition_source" "source")


;*************************Drain*************************

(sdedr:define-constant-profile "ConstantProfileDefinition_drain" "ArsenicActiveConcentration"
2e+20)

(sdedr:define-constant-profile-region "ConstantProfilePlacement_drain"
"ConstantProfileDefinition_drain" "drain")


;*************************Substrate*************************

(sdedr:define-constant-profile "ConstantProfileDefinition_substrate" "BoronActiveConcentration"
1e+17)

(sdedr:define-constant-profile-region "ConstantProfilePlacement_substrate"
"ConstantProfileDefinition_substrate" "region_SUBSTRATE")


;#########################################################################
;                                        CONTACTS
;#########################################################################


(sdegeo:create-cuboid (position 0 0.0075 0.0005) (position -0.002 0.0425 0.0355) "Metal"
"region_source_contact")
(sdegeo:create-cuboid (position 0 0.0935 0.0005) (position -0.002 0.1285 0.0355) "Metal"
"region_drain_contact")
(sdegeo:create-cuboid (position -0.017 0.0525 0.0025) (position -0.019 0.0835 0.0335) "Metal"
"region_gate_contact")
(sdegeo:create-cuboid (position 0.136 0.0505 0.0005) (position 0.138 0.0855 0.0355) "Metal"
"region_substrate_contact")

(sdegeo:define-contact-set "G" 4 (color:rgb 1 0 0 ) "##")

(sdegeo:define-contact-set "S" 4 (color:rgb 1 1 0 ) "##")

(sdegeo:define-contact-set "D" 4 (color:rgb 1 1 1 ) "##")
```

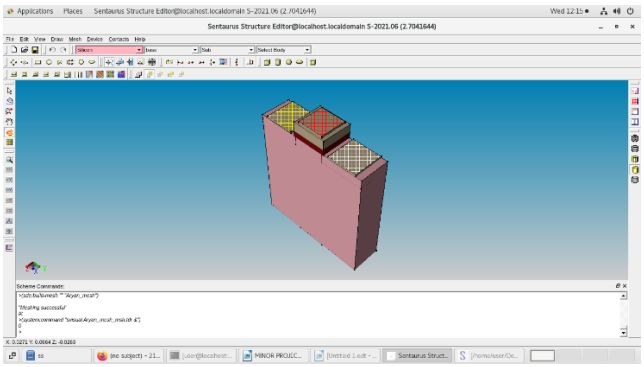
(sdegeo:define-contact-set "Sub" 4 (color:rgb 0 1 1) "##")

(sdegeo:set-current-contact-set "S")
"none"
(sdegeo:define-3d-contact (list (car (find-face-id (position -0.002 0.025 0.018)))) "S")
(render:rebuild)
(sdegeo:set-current-contact-set "D")
"source"
(sdegeo:define-3d-contact (list (car (find-face-id (position -0.002 0.111 0.018)))) "D")
(render:rebuild)

(sdegeo:set-current-contact-set "G")
"drain"
(sdegeo:define-3d-contact (list (car (find-face-id (position -0.019 0.068 0.018)))) "G")
(render:rebuild)

(sdegeo:set-current-contact-set "Sub")
"drain"
(sdegeo:define-3d-contact (list (car (find-face-id (position 0.138 0.068 0.018)))) "Sub")
(render:rebuild)





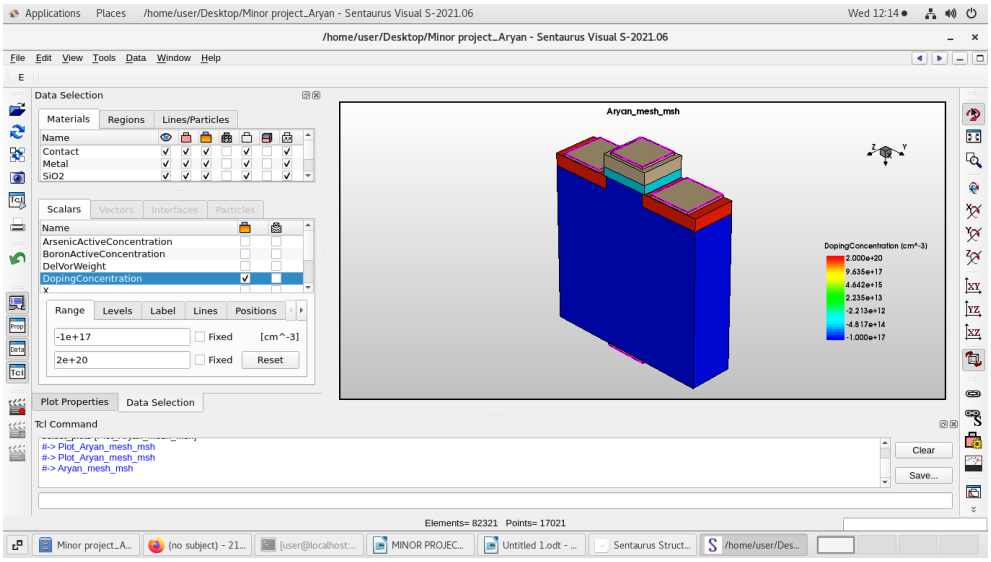
;###
; **MESHING**
;###

(sdedr:define-refinement-size "RefinementDefinition_silicon" 0.004 0.012 0.01 0.002 0.006 0.005)
(sdedr:define-refinement-material "RefinementPlacement_silicon" "RefinementDefinition_silicon"
"Silicon")

(sdedr:define-refinement-size "RefinementDefinition_SiO2" 0.002 0.006 0.01 0.002 0.003 0.005)

(sdedr:define-refinement-material "RefinementPlacement_SiO2" "RefinementDefinition_SiO2" "SiO2")

(sdedr:define-refinement-size "RefinementDefinition_Metal" 0.0004 0.006 0.01 0.0002 0.003 0.005)
(sdedr:define-refinement-material "RefinementPlacement_Metal" "RefinementDefinition_Metal" "Metal")



REFRENCES

Books

"Fundamentals of modern vlsi devices Book" by Tak H. Ning and Yuan Taur

"CMOS Digital Integrated Circuits Analysis and Design" by Suand-Mo Kang and Yusuf Leblebici

Journals

IEEE Transactions on Electronic Devices

IEEE Transactions on Nanotechnology

Research Paper

https://ieeexplore.ieee.org/document/4444639

https://sci-hub.ru/10.1109/tnano.2003.817224