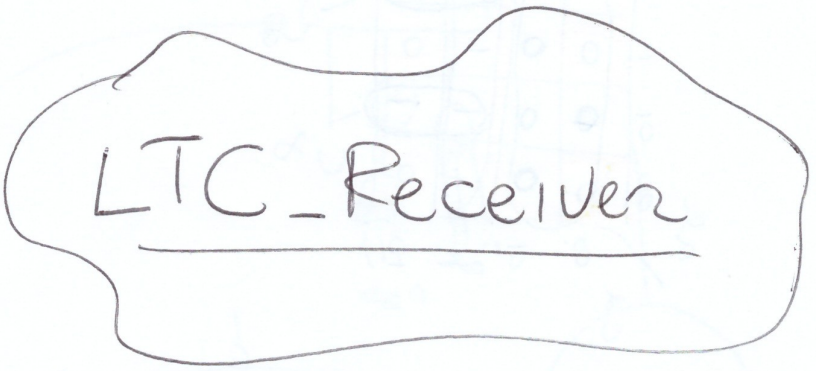
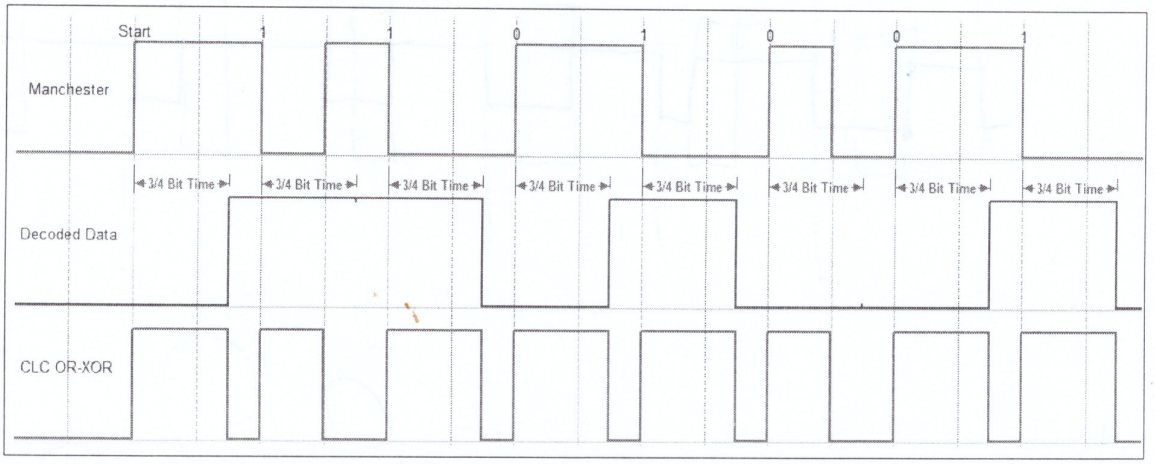

LTC_Receiver

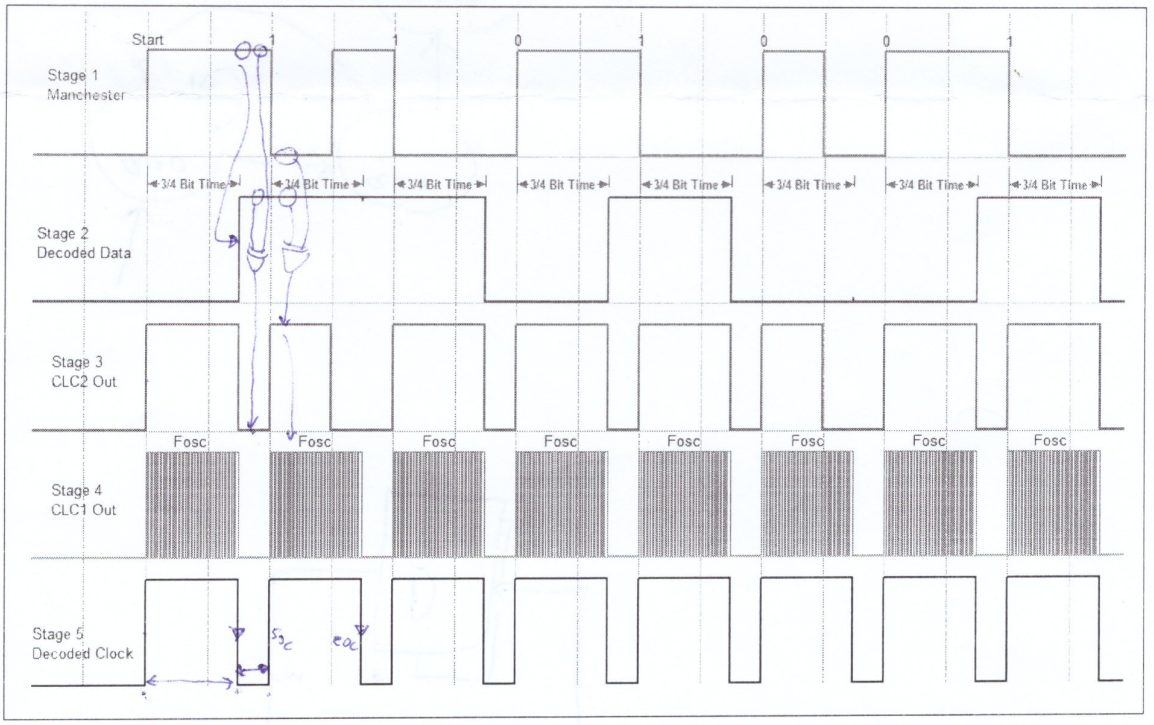
CLC block in OR-XOR configuration is used to extract clock out of this configuration (Figure 8).

FIGURE 8: CLOCK EXTRACTION



This essentially is our Manchester decoder, where CLC OR-XOR is clock and *D* is data. If we use the rising edge of a clock signal to capture data from *D*, we notice that every bit except the first one is decoded. The issue can be resolved in several ways, which will be discussed in the **Section "Synchronization"**.

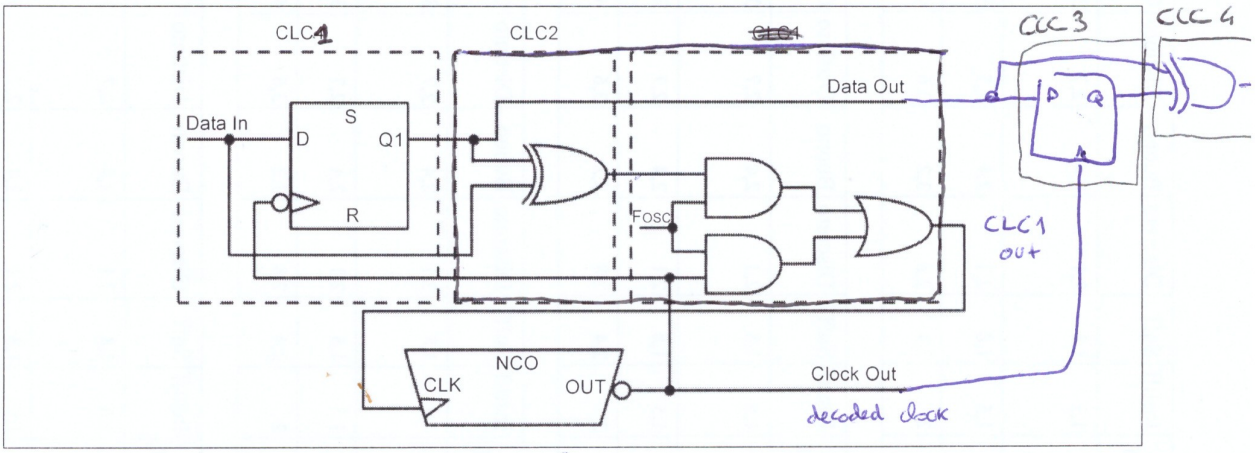
FIGURE 9: MANCHESTER DECODER



The timing diagram above (Figure 9) is decoded into the following block diagram (Figure 10). There are five stages in this diagram:

- Stage 1 – Incoming Manchester Signal
- Stage 2 – D flip-flop that captures input data when NCO is triggered
- Stage 3 – XOR gate to provide start time for NCO
- Stage 4 – AND-OR gate to supply clock to NCO, and to ensure that it clocks for full ¾ bit time
- Stage 5 – NCO to generate ¾ bit time, started in mid-bit transition of previous bit

FIGURE 10: FULL DECODER BLOCK DIAGRAM



PIC16F1509 IMPLEMENTATION

The device chosen for this implementation is PIC16F1509. It has four CLC blocks to implement combinational logic along with NCO to generate specific bit time. The following section covers the implementation of these blocks using the available resources in this device.

Stage 1 – D Flip-Flop (CLC4)

This stage latches in the Manchester data on the falling edge of the clock signal. This output is the recovered data that will be fed into the microcontroller. The data is sampled on the clock falling edge, and is stable to be read on the clock rising edge, because the data line never changes on a rising clock edge.

Stage 2 – XOR Gate (CLC2)

Because a transition is ensured in the middle of every bit in Manchester encoding, we can use an XOR gate to ensure that each mid-bit transition gives us a rising edge for Stage 3. This means that we are synchronizing our decoder in the middle of each bit.

Stage 3 – NCO + AND-OR (CLC1)

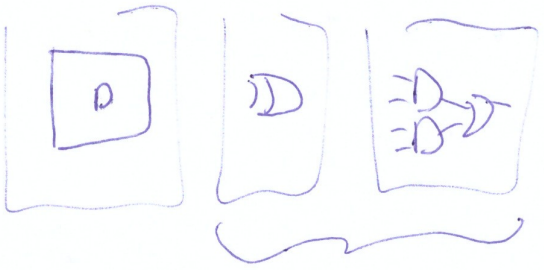
The PIC16F1509 has a NCO module that is used to generate ¾ bit-time to capture data value. The NCO is used in active-low Pulse Frequency mode to output a pulse when ¾ bit time expires. The pulse width can be controlled using a Special Function Register. The module also requires a clock source that allows it to repeatedly add a fixed value to an accumulator at the specified clock rate, which will be supplied by CLC1.

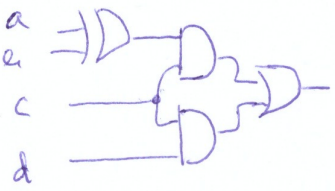
These two blocks together are the most important in the decoder. They create a fixed length pulse for each rising edge coming out of Stage 2. The output of the NCO is fed back into the AND-OR gate, so that when the output of Stage 2 goes to zero, the NCO will continue clocking until it overflows.

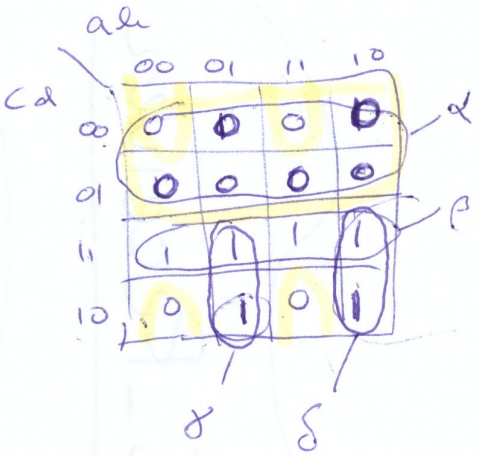
When the part is first configured, it will output a single ¾ bit length pulse. This is needed to put the NCO in its active-low state. When it is active, the NCO is waiting on the output pulse width clocks configured in the NCOCLK register.* Once a clock source is supplied, it will finish its active pulse and start counting again.

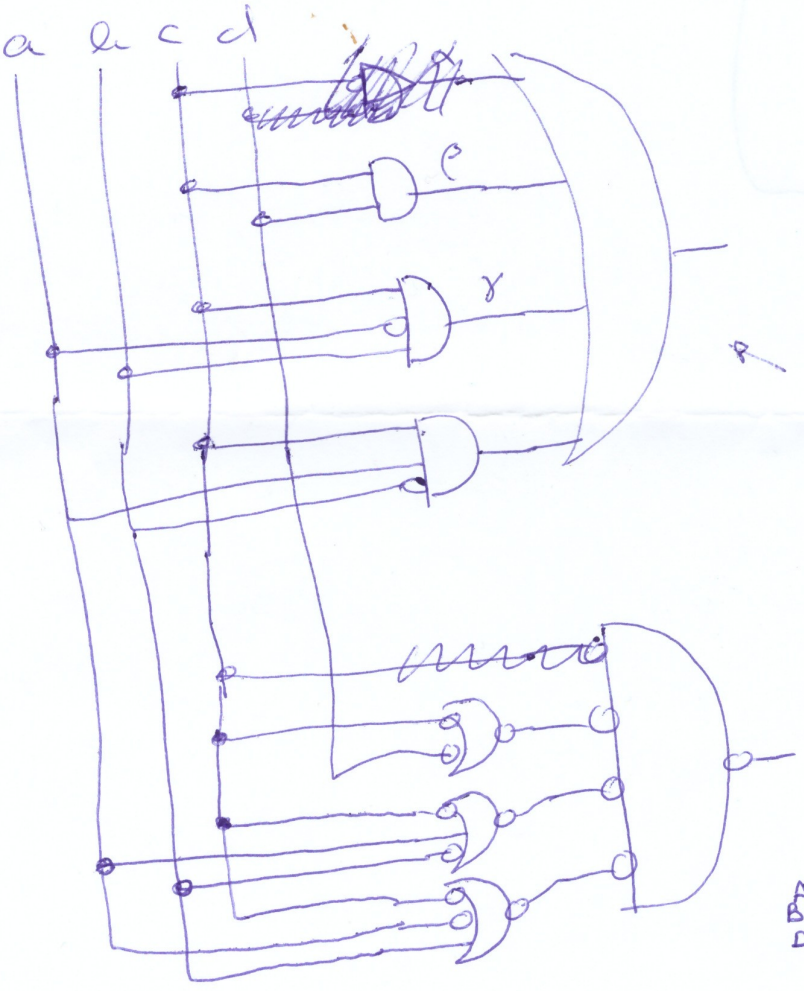
**Design Tip: By removing the clock source from the NCO and holding it in its active state, you have essentially created a way to control the duty cycle of the NCO.*

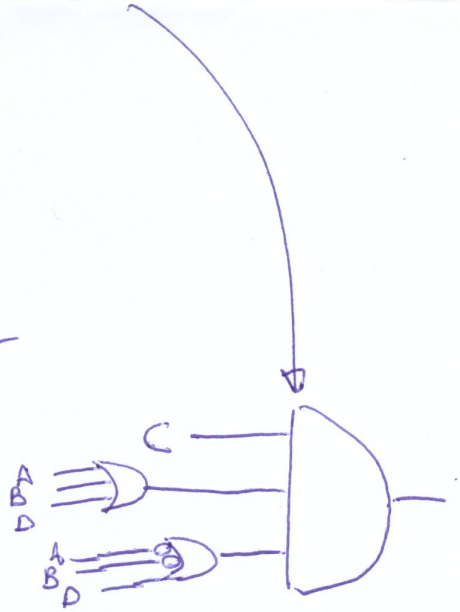
$$\text{Increment} = \frac{1\ \text{KHz} \cdot 2^{20}}{32\ \text{MHz}} = \frac{2^{20}}{32000} \qquad \frac{2{,}4\ \text{KHz} \cdot 2^{20}}{500\ \text{KHz}} =$$

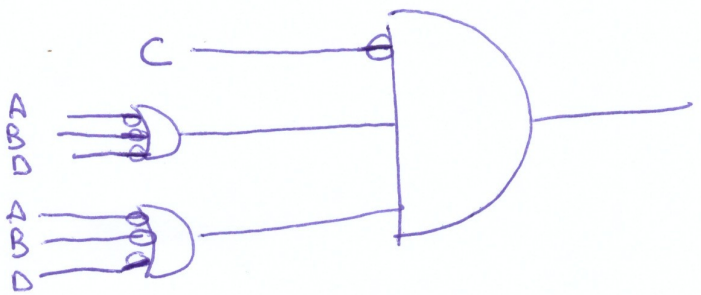












$$C \cdot (A + B + D) \cdot (\bar{A} + \bar{B} + D)$$

$$IMC = \frac{f \cdot 2^{20}}{Fosc}$$

DATE

OBJECT

$10 < f_{sig} < 4{,}8\ KHz$

$26 < f < 6400$

$$Fox_{MAX} = \frac{f_{max} \cdot 2^{20}}{IMC=1} = \frac{26 \cdot 2^{20}}{1} = 27{,}26\ MHz$$

$Fosc = 24\ MHz$;

$$f_{min} = \frac{1 \cdot 24\ MHz}{2^{20}} = 22{,}9\ Hz$$

$f_{max} \cong 24\ MHz$

$$IMC_{60Fps=6400} = \frac{6400 \cdot 2^{20}}{24\ MHz} = 279{,}6$$

$$IMC_{25Fps=2666} = \frac{2666 \cdot 2^{20}}{24\ MHz} = 116{,}5$$

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