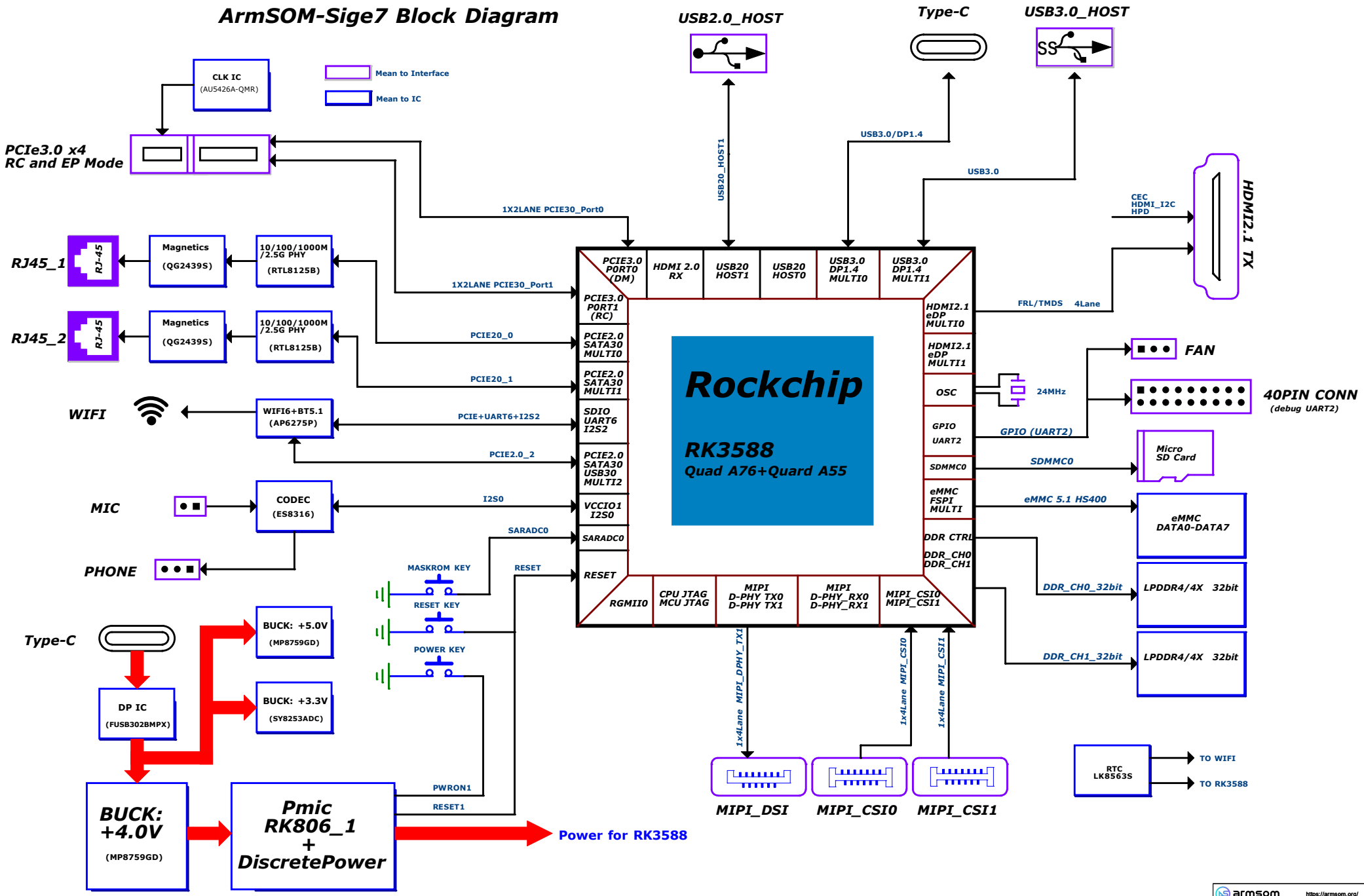
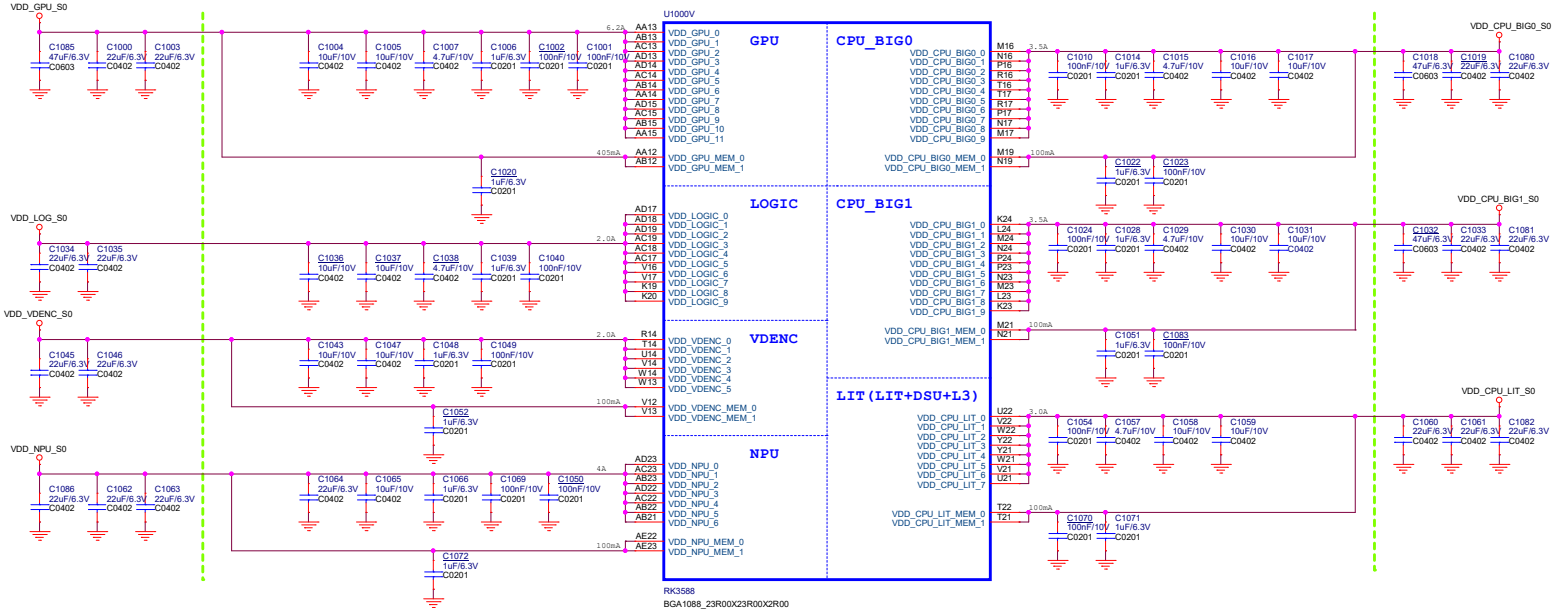
ArmSOM-Sige7 Block Diagram

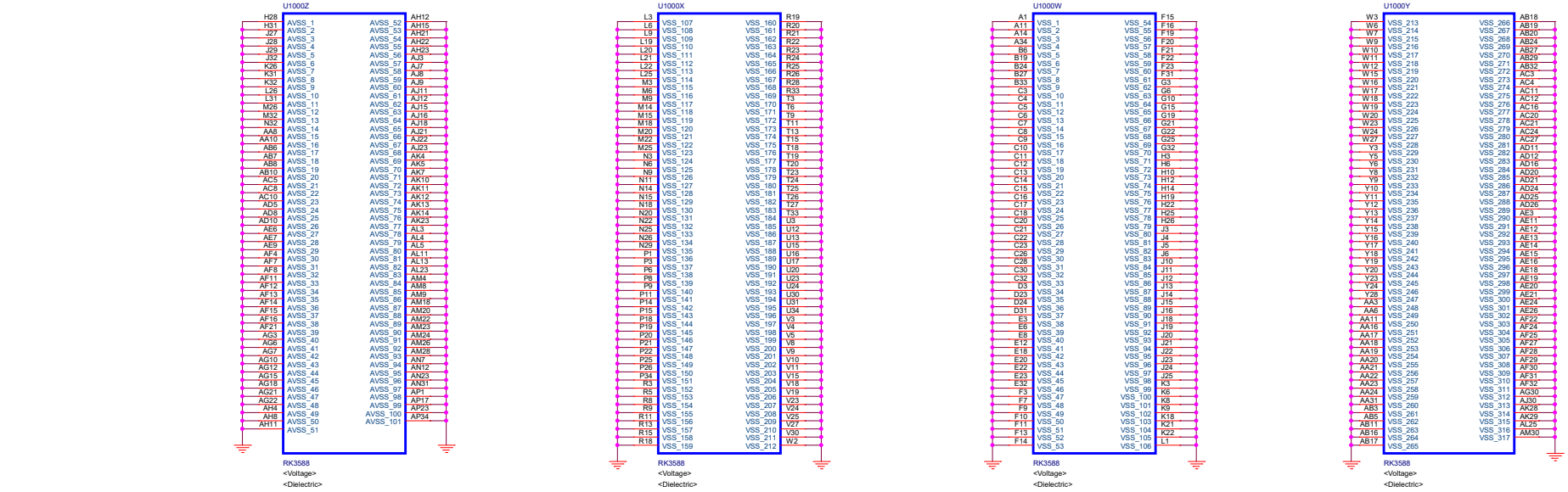


armsom	https://armsom.org/				
Project:	ArmSoM-Sige7				
File:	Block Diagram				
Date:	Monday, December 25, 2023			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	1 of 24

RK3588_V(POWER)



Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package



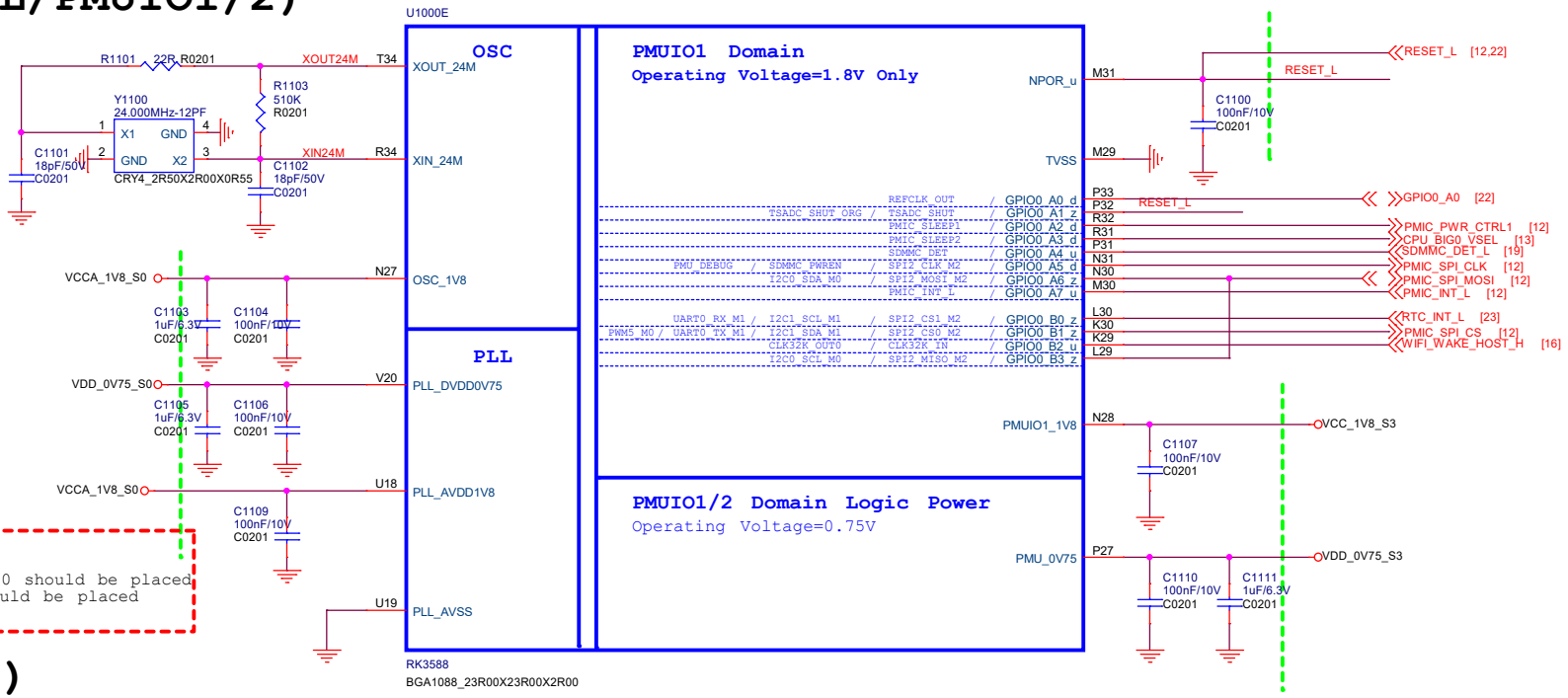
armsom	https://armsom.org/		
Project:	ArmSoM-Sige7		
File:	RK3588_Power/GND		
Date:	Monday, December 18, 2023	Rev:	V1.1
Designed by: Park	Reviewed by: <Checker>	Sheet:	2 of 24

RK3588_E(OSC/PLL/PMUIO1/2)

Note:
Adjusted the load capacitance according to the crystal specification

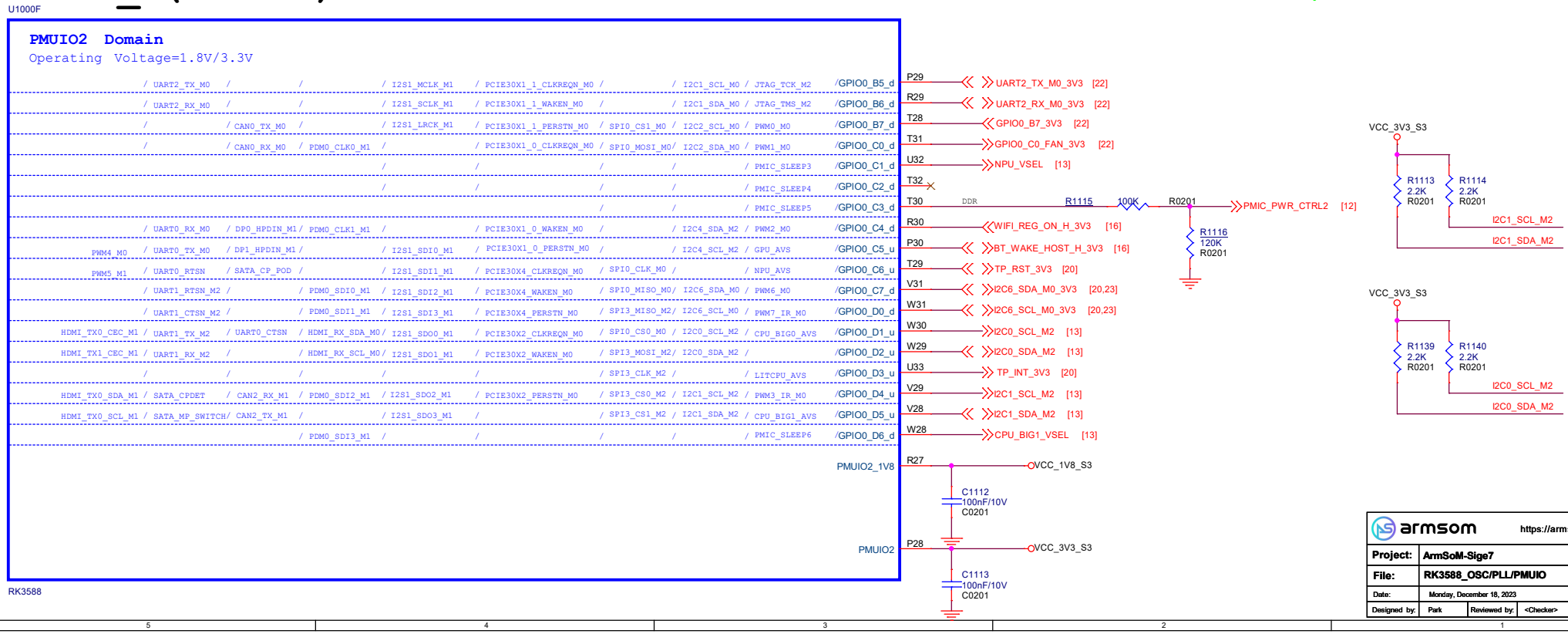
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<=12pF

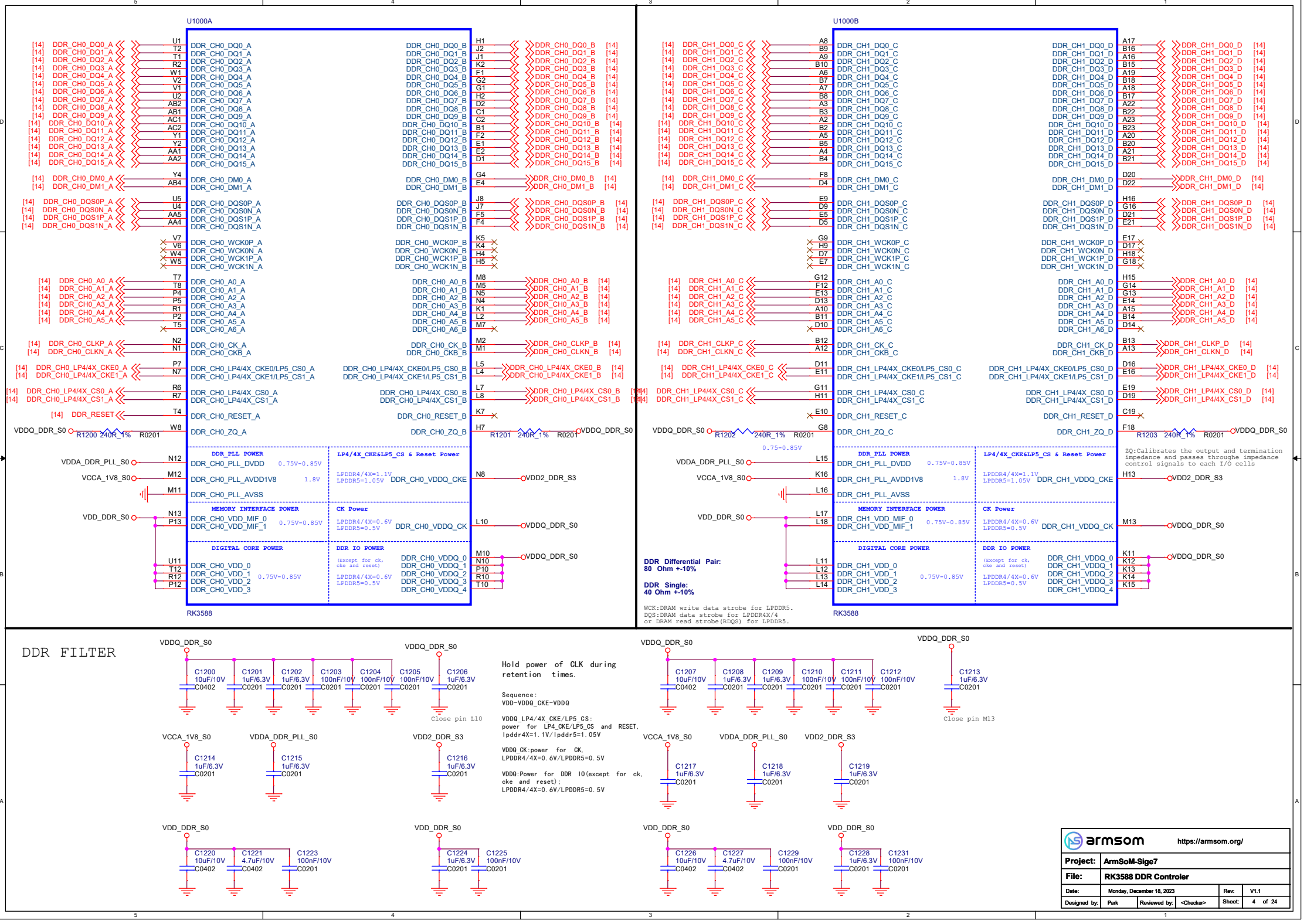


Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package

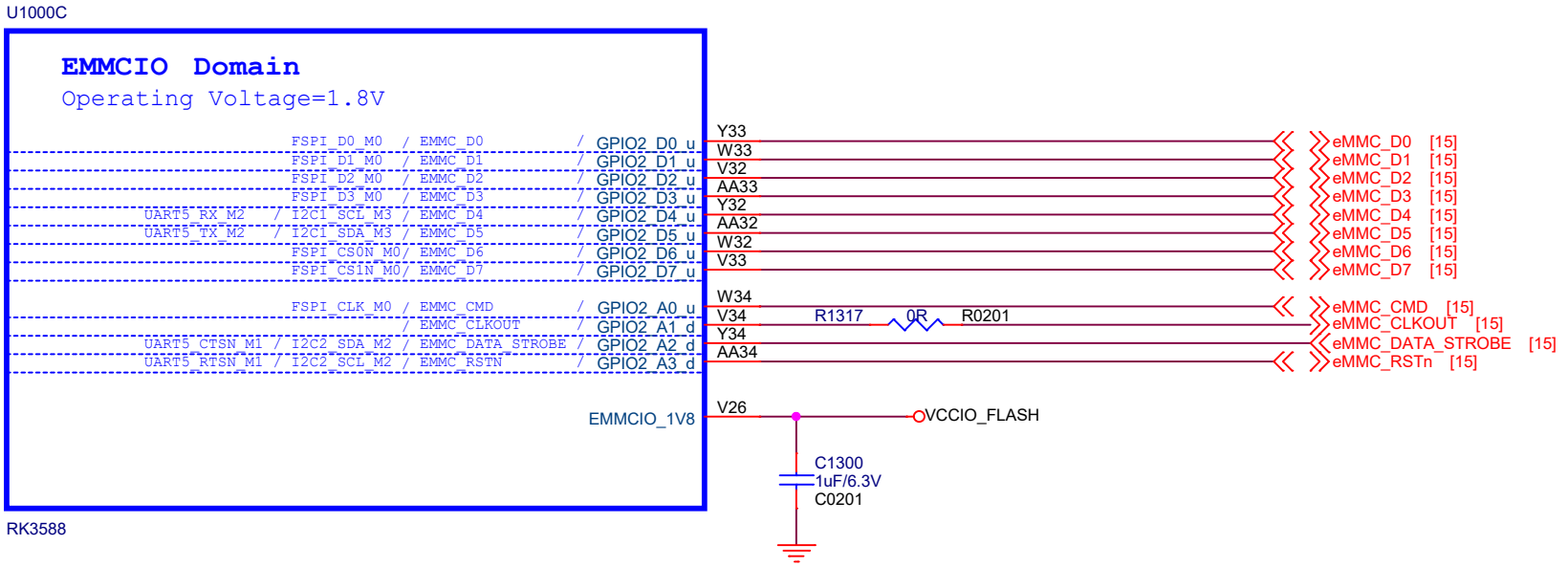
RK3588_F(PMUIO2)



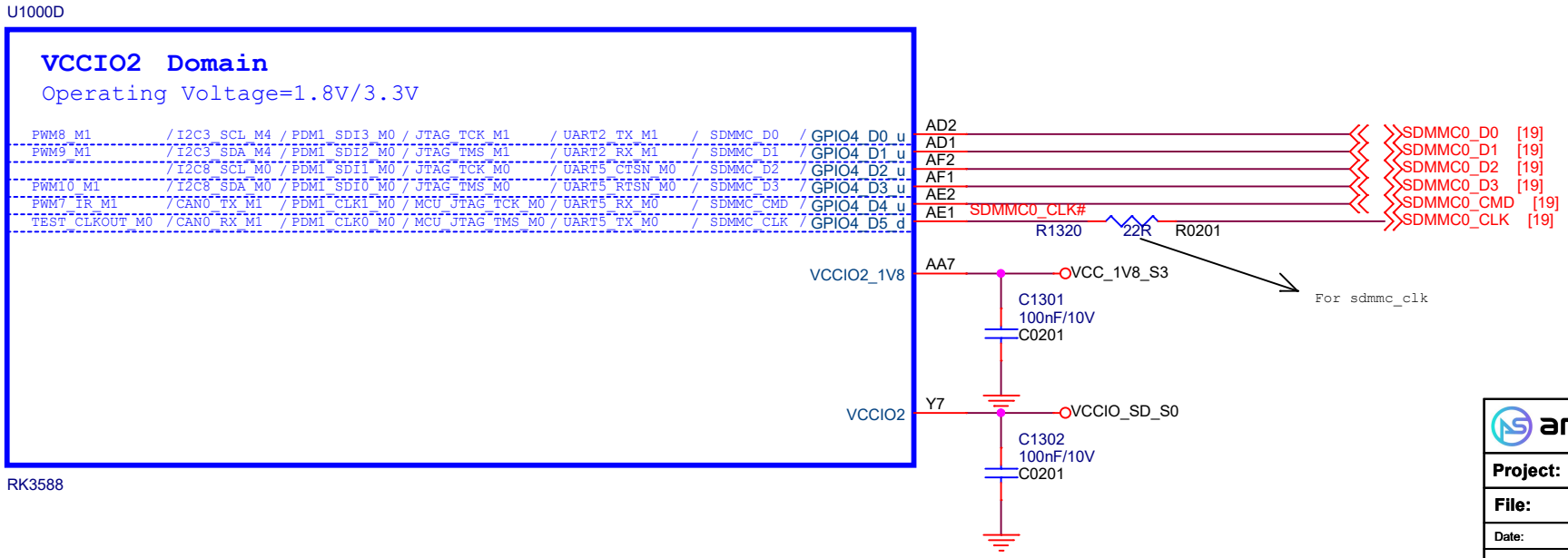
armsom	https://armsom.org/				
Project:	ArmSoM-Sige7				
File:	RK3588_OSC/PLL/PMUIO				
Date:	Monday, December 18, 2023			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	3 of 24


U1000A
U1000B
RK3588
RK3588
DDR_PLL POWER
LP4/4X_CKE&LP5_CS & Reset Power
MEMORY INTERFACE POWER
CK Power
DIGITAL CORE POWER
DDR IO POWER
DDR Differential Pair:
80 Ohm +-10%
DDR Single:
40 Ohm +-10%
WCK:DRAM write data strobe for LPDDR5.
DQS:DRAM data strobe for LPDDR4X/4
or DRAM read strobe(RDQS) for LPDDR5.
ZQ:Calibrates the output and termination impedance and passes throughe impedance control signals to each I/O cells
DDR FILTER
Hold power of CLK during retention times.
Sequence:
VDD-VDDQ_CKE-VDDQ
VDDQ_LP4/4X_CKE/LP5_CS:
power for LP4_CKE/LP5_CS and RESET, lpddr4X=1.1V/lpddr5=1.05V
VDDQ_CK:power for CK, LPDDR4/4X=0.6V/LPDDR5=0.5V
VDDQ:Power for DDR IO(except for ck, cke and reset); LPDDR4/4X=0.6V/LPDDR5=0.5V
Close pin L10
Close pin M13
armsom
https://armsom.org/
Project: ArmSoM-Sige7
File: RK3588 DDR Controler
Date: Monday, December 18, 2023
Rev: V1.1
Designed by: Park
Reviewed by: <Checker>
Sheet: 4 of 24

RK3588_C(EMMCIO Domain)



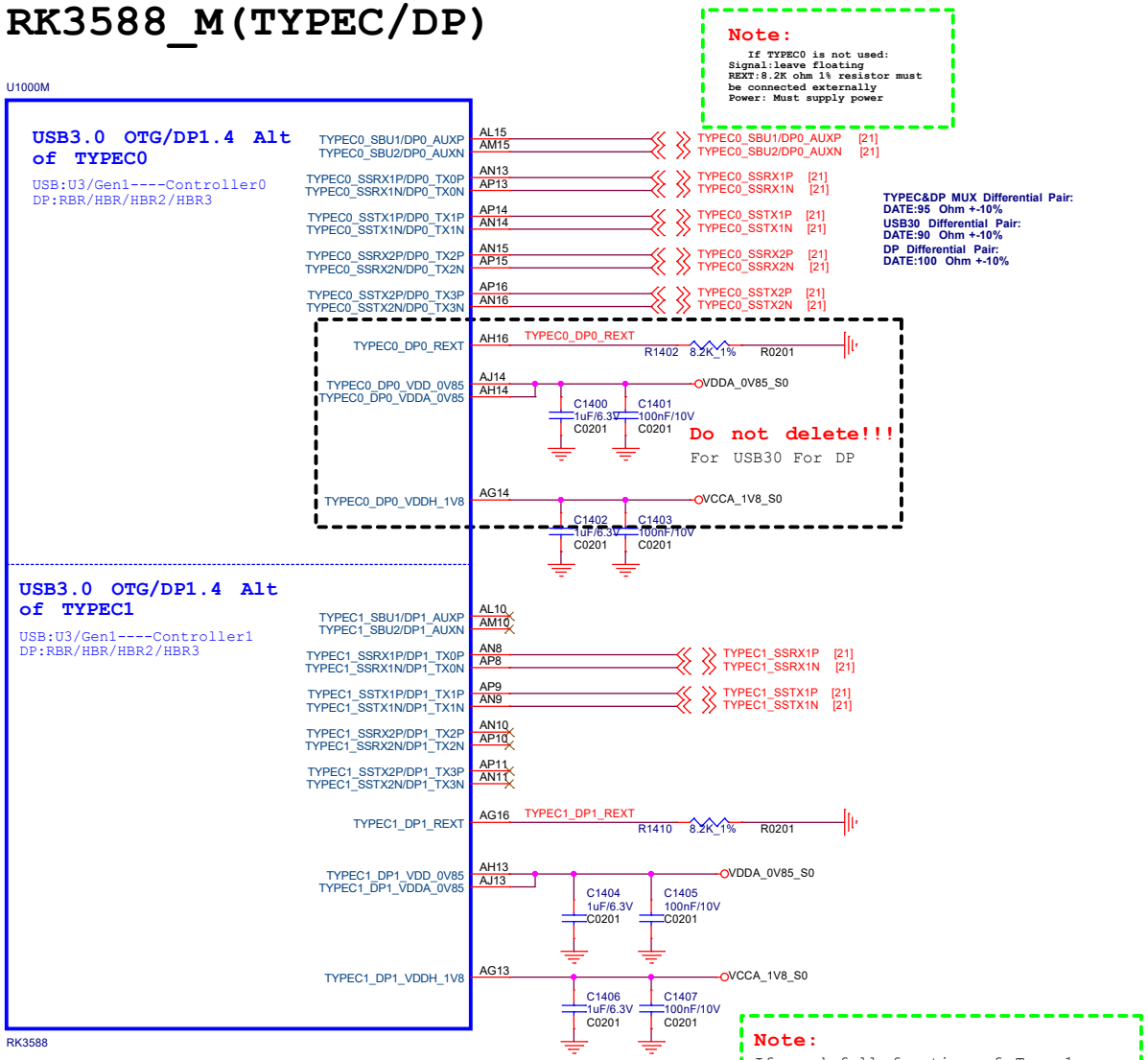
RK3588_D(VCCIO2 Domain)



armsom https://armsom.org/

Project:	ArmSoM-Sige7				
File:	RK3588_Flash/SD Controller				
Date:	Monday, December 18, 2023			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	5 of 24

RK3588_M(TYPEC/DP)



Note:
If TYPEC0 is not used:
Signal:leave floating
REXT:8.2K ohm 1% resistor must be connected externally
Power: Must supply power

TYPEC&DP MUX Differential Pair: DATE:95 Ohm +-10%
USB30 Differential Pair: DATE:90 Ohm +-10%
DP Differential Pair: DATE:100 Ohm +-10%

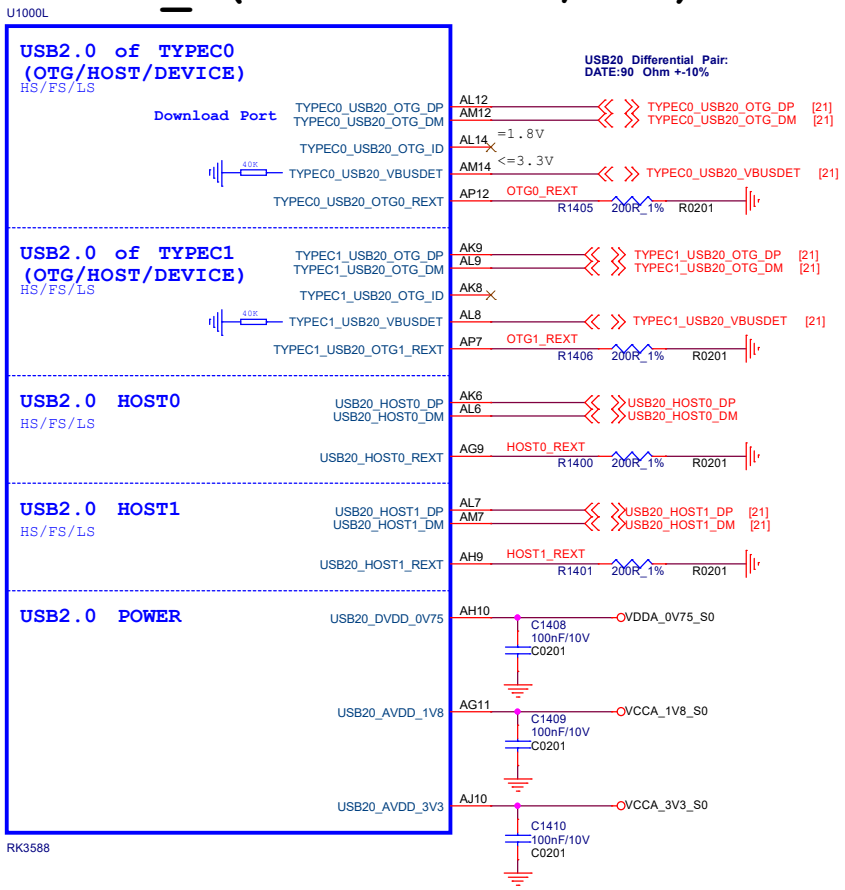
Note:
If need full function of Typec1 (With DP funtion) please Refer to the circuit of Typec0

If TYPEC1 is not used,
Signal: Leave floating
REXT: Leave floating
Power: Leave floating

USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*USB30 x4Lane*	*TYPEC_SSTX1P/1N&TYPEC_SSRX1P/1N or TYPEC_SSTX2P/2N&TYPEC_SSRX2P/2N*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:Lane0 Lane1 DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:Lane2 Lane3 DP:Lane0 Lane1*

RK3588_L(USB2.0 HOST/OTG)



USB20 Differential Pair: DATE:90 Ohm +-10%

Note:
TYPEC0_USB20_OTG:
DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

TYPEC1_USB20_OTG:
If not used:
DP/DM:Leave floating
ID:Leave floating
VBUSDET:Leave floating
REXT:Leave floating
Power:Leave floating

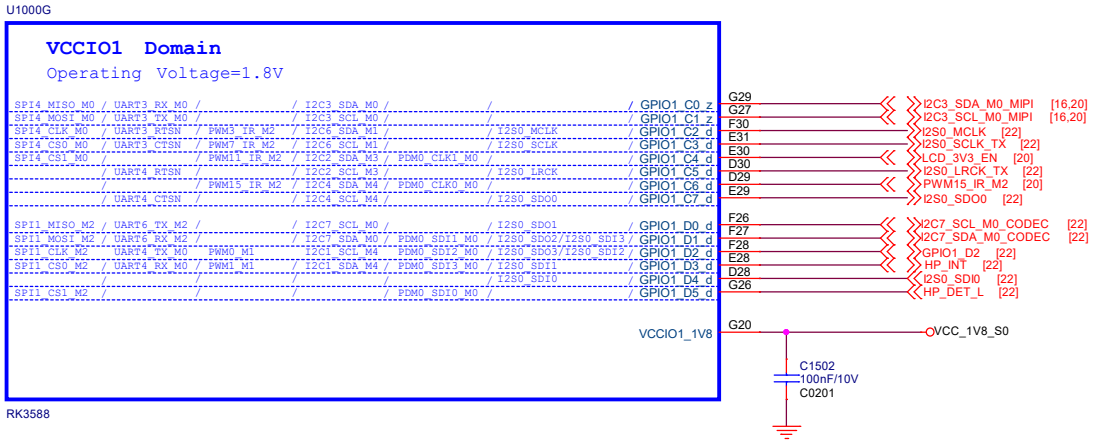
USB20_HOST0/USB20_HOST1:
If not used:
DP/DM:Leave floating
REXT:Leave floating
Power:Leave floating

Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 30K ohm resistor.The VBUSDETpin voltage range <=3.3V.

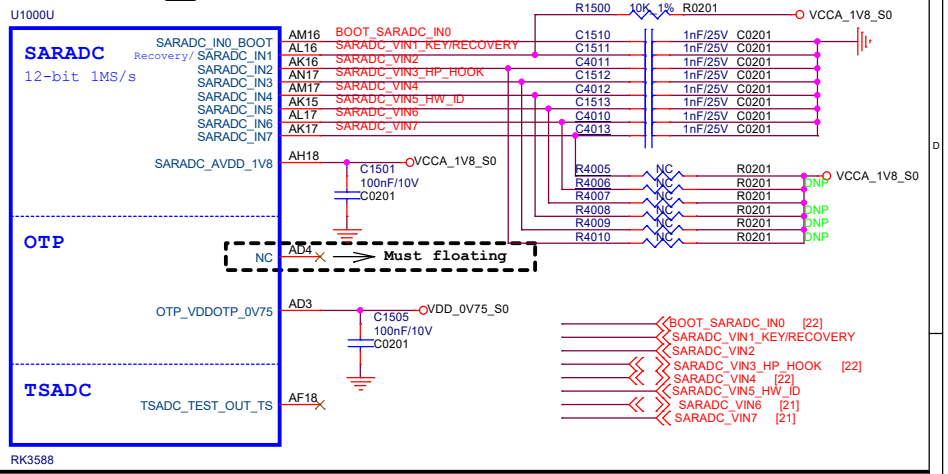
armsom https://armsom.org/

Project:	ArmSoM-Sige7				
File:	RK3588_USB30/USB20_Ctrl				
Date:	Monday, December 18, 2023			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	6 of 24

RK3588_G(VCCIO1 Domain)



RK3588_U(SARADC/OTP)



BOOT MODE CONFIG

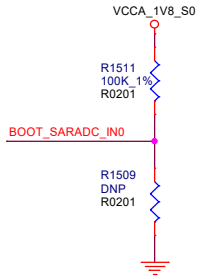


TABLE 1

Item	Rup	Rdown	ADC	VOL	BOOT MODE
LEVEL1	100K	0ohm	0	0V	USB (Maskrom mode)
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	100K	51K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	100K	200K	2730	1.2V	FSPI M1-USB
LEVEL6	100K	499K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0 -EMMC-SD Card-USB

BOARD ID CONFIG

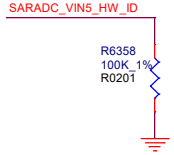
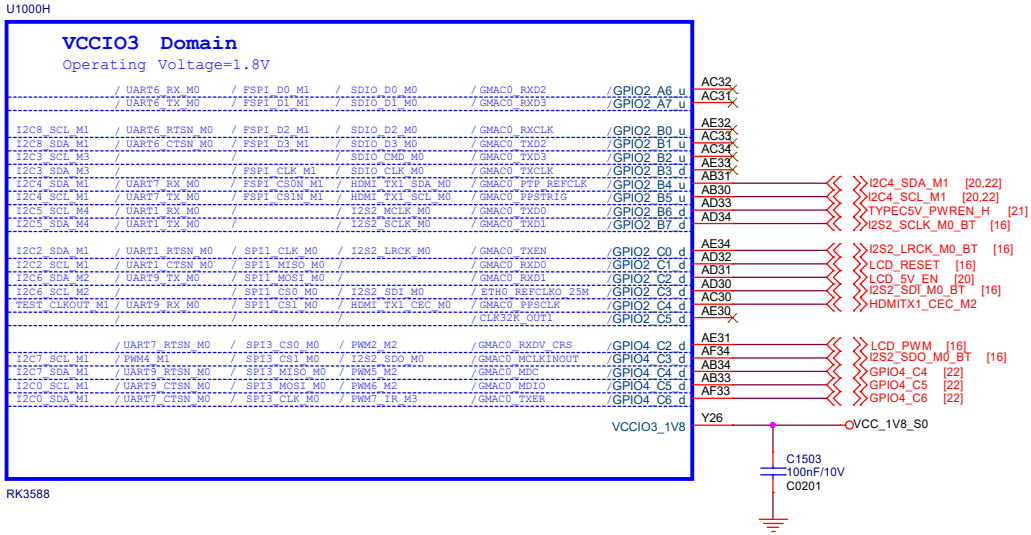
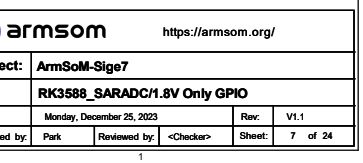


TABLE 2

Item	Rup	Rdown	ADC	VOL	VERSION
LEVEL1	DNP	100K	0	0V	V1.0
LEVEL2	100K	20K	682	0.3V	V2.0
LEVEL3	100K	51K	1365	0.6V	V3.0
LEVEL4	100K	100K	2047	0.9V	V4.0
LEVEL5	100K	200K	2730	1.2V	V5.0
LEVEL6	100K	499K	3412	1.5V	V6.0
LEVEL7	100K	DNP	4095	1.8V	V7.0

RK3588_H(VCCIO3 Domain)





RK3588_Q/R(MIPI_D/C_PHY0/1)

U1000Q

MIPI D/C-PHY DSI_TX Port0

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY0_TX_CLKP/MIPI_CPHY0_TX_TRIO1_C — AN26
MIPI_DPHY0_TX_CLKN/MIPI_CPHY0_TX_TRIO1_B — AP26
MIPI_DPHY0_TX_D0P/MIPI_CPHY0_TX_TRIO0_B — AN24
MIPI_DPHY0_TX_D0N/MIPI_CPHY0_TX_TRIO0_A — AP24
MIPI_DPHY0_TX_D1P/MIPI_CPHY0_TX_TRIO1_A — AN25
MIPI_DPHY0_TX_D1N/MIPI_CPHY0_TX_TRIO0_C — AP25
MIPI_DPHY0_TX_D2P/MIPI_CPHY0_TX_TRIO2_B — AN27
MIPI_DPHY0_TX_D2N/MIPI_CPHY0_TX_TRIO2_A — AP27
MIPI_DPHY0_TX_D3P /NO_USE_AN28 — AN28
MIPI_DPHY0_TX_D3N/MIPI_CPHY0_TX_TRIO2_C — AP28

MIPI DPHY Differential Pair:
100 Ohm +-10%

MIPI CPHY Single:
50 Ohm +-10%

TX and RX port must work in the same mode, DPHY or CPHY

MIPI D/C-PHY CSI_RX Port0

D-PHY:V1.2 2.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

Note:
此D-PHY不支持接收！！
详细情况请参阅硬件设计指南。
This D-PHY is limited!!!
Please refer to the hardware design guide for details.

MIPI_DPHY0_RX_CLKP/MIPI_CPHY0_RX_TRIO1_C — AN32
MIPI_DPHY0_RX_CLKN/MIPI_CPHY0_RX_TRIO1_B — AP32
MIPI_DPHY0_RX_D0P/MIPI_CPHY0_RX_TRIO0_B — AN29
MIPI_DPHY0_RX_D0N/MIPI_CPHY0_RX_TRIO0_A — AP29
MIPI_DPHY0_RX_D1P/MIPI_CPHY0_RX_TRIO1_A — AN30
MIPI_DPHY0_RX_D1N/MIPI_CPHY0_RX_TRIO0_C — AP30
MIPI_DPHY0_RX_D2P/MIPI_CPHY0_RX_TRIO2_B — AN33
MIPI_DPHY0_RX_D2N/MIPI_CPHY0_RX_TRIO2_A — AP33
MIPI_DPHY0_RX_D3P /NO_USE_AN34 — AN34
MIPI_DPHY0_RX_D3N/MIPI_CPHY0_RX_TRIO2_C — AP34

Note:
Suggest Using 1/2 lane mode.
Using 4Lane is limited,
Please refer to the hardware design guide for details.

MIPI D/C-PHY POWER

MIPI_D/C_PHY0_VREG — AF20 — C1600 1uF/6.3V — C0201
MIPI_D/C_PHY0_VDD — AG20 — VDD_0V75_S0
C1602 100nF/10V C0201
C1601 1uF/6.3V C0201
C-PHY 5.7Gbps 0.85V
D-PHY 2.5Gbps & C-PHY 5.7Gbps 0.75V
MIPI_D/C_PHY0_VDD_1V2 — AH20 — VDDA_1V2_S0
C1603 1uF/6.3V C0201
MIPI_D/C_PHY0_VDD_1V8 — AJ20 — VCC_1V8_S0
C1605 1uF/6.3V C0201

RK3588

U1000R

MIPI D/C-PHY DSI_TX Port1

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY1_TX_CLKP/MIPI_CPHY1_TX_TRIO1_C — AN20 — MIPI_DPHY1_TX_CLKP [20]
MIPI_DPHY1_TX_CLKN/MIPI_CPHY1_TX_TRIO1_B — AP20 — MIPI_DPHY1_TX_CLKN [20]
MIPI_DPHY1_TX_D0P/MIPI_CPHY1_TX_TRIO0_B — AN18 — MIPI_DPHY1_TX_D0P [20]
MIPI_DPHY1_TX_D0N/MIPI_CPHY1_TX_TRIO0_A — AP18 — MIPI_DPHY1_TX_D0N [20]
MIPI_DPHY1_TX_D1P/MIPI_CPHY1_TX_TRIO1_A — AN19 — MIPI_DPHY1_TX_D1P [20]
MIPI_DPHY1_TX_D1N/MIPI_CPHY1_TX_TRIO0_C — AP19 — MIPI_DPHY1_TX_D1N [20]
MIPI_DPHY1_TX_D2P/MIPI_CPHY1_TX_TRIO2_B — AN21 — MIPI_DPHY1_TX_D2P [20]
MIPI_DPHY1_TX_D2N/MIPI_CPHY1_TX_TRIO2_A — AP21 — MIPI_DPHY1_TX_D2N [20]
MIPI_DPHY1_TX_D3P /NO_USE_AN22 — AN22 — MIPI_DPHY1_TX_D3P [20]
MIPI_DPHY1_TX_D3N/MIPI_CPHY1_TX_TRIO2_C — AP22 — MIPI_DPHY1_TX_D3N [20]

TX and RX port must work in the same mode, DPHY or CPHY

MIPI D/C-PHY CSI_RX Port1

D-PHY:V1.2 2.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

Note:
此D-PHY不支持接收！！
详细情况请参阅硬件设计指南。
This D-PHY is limited!!!
Please refer to the hardware design guide for details.

MIPI_DPHY1_RX_CLKP/MIPI_CPHY1_RX_TRIO1_C — AK20
MIPI_DPHY1_RX_CLKN/MIPI_CPHY1_RX_TRIO1_B — AL20
MIPI_DPHY1_RX_D0P/MIPI_CPHY1_RX_TRIO0_B — AK18
MIPI_DPHY1_RX_D0N/MIPI_CPHY1_RX_TRIO0_A — AL18
MIPI_DPHY1_RX_D1P/MIPI_CPHY1_RX_TRIO1_A — AK19
MIPI_DPHY1_RX_D1N/MIPI_CPHY1_RX_TRIO0_C — AL19
MIPI_DPHY1_RX_D2P/MIPI_CPHY1_RX_TRIO2_B — AK21
MIPI_DPHY1_RX_D2N/MIPI_CPHY1_RX_TRIO2_A — AL21
MIPI_DPHY1_RX_D3P /NO_USE_AK22 — AK22
MIPI_DPHY1_RX_D3N/MIPI_CPHY1_RX_TRIO2_C — AL22

Note:
Suggest Using 1/2 lane mode.
Using 4Lane is limited,
Please refer to the hardware design guide for details.

MIPI D/C-PHY POWER

MIPI_D/C_PHY1_VREG — AF19 — C1608 1uF/6.3V — C0201
MIPI_D/C_PHY1_VDD — AG19 — VDD_0V75_S0
C1609 1uF/6.3V C0201
MIPI_D/C_PHY1_VDD_1V2 — AH19 — VDDA_1V2_S0
C1611 100nF/10V C0201
MIPI_D/C_PHY1_VDD_1V8 — AJ19 — VCC_1V8_S0
C1613 1uF/6.3V C0201

Note:
If not used:
Signal:leave floating
Power: Floating

RK3588

RK3588_P(MIPI_DPHY_CSI_RX_PHY)

U1000P

MIPI DPHY CSI_RX Port0

MIPI V1.2/2.5Gbps

MIPI_CSI0_CLK0P/MIPI_CSI0_CLK0N — AJ33/AJ34 — MIPI_CSI0_RX_CLK0P/MIPI_CSI0_RX_CLK0N [20]
MIPI_CSI0_D0P/MIPI_CSI0_D0N — AG33/AG34 — MIPI_CSI0_RX_D0P/MIPI_CSI0_RX_D0N [20]
MIPI_CSI0_D1P/MIPI_CSI0_D1N — AH33/AH34 — MIPI_CSI0_RX_D1P/MIPI_CSI0_RX_D1N [20]
MIPI_CSI0_CLK1P/MIPI_CSI0_CLK1N — AM33/AM34 — MIPI_CSI0_RX_CLK1P/MIPI_CSI0_RX_CLK1N [20]
MIPI_CSI0_D2P/MIPI_CSI0_D2N — AK33/AK34 — MIPI_CSI0_RX_D2P/MIPI_CSI0_RX_D2N [20]
MIPI_CSI0_D3P/MIPI_CSI0_D3N — AL33/AL34 — MIPI_CSI0_RX_D3P/MIPI_CSI0_RX_D3N [20]

MIPI CSI Differential Pair:
100 Ohm +-10%

MIPI_CSI0_AVCC0V75 — AB25 — VDD_0V75_S0
C1616 100nF/10V C0201
C1615 1uF/6.3V C0201
MIPI_CSI0_AVCC1V8 — AB26 — VCC_1V8_S0
C1617 1uF/6.3V C0201

MIPI DPHY CSI_RX Port1

MIPI V1.2/2.5Gbps

MIPI_CSI1_CLK0P/MIPI_CSI1_CLK0N — AJ31/AJ32 — MIPI_CSI1_RX_CLK0P/MIPI_CSI1_RX_CLK0N [20]
MIPI_CSI1_D0P/MIPI_CSI1_D0N — AG31/AG32 — MIPI_CSI1_RX_D0P/MIPI_CSI1_RX_D0N [20]
MIPI_CSI1_D1P/MIPI_CSI1_D1N — AH31/AH32 — MIPI_CSI1_RX_D1P/MIPI_CSI1_RX_D1N [20]
MIPI_CSI1_CLK1P/MIPI_CSI1_CLK1N — AM31/AM32 — MIPI_CSI1_RX_CLK1P/MIPI_CSI1_RX_CLK1N [20]
MIPI_CSI1_D2P/MIPI_CSI1_D2N — AK31/AK32 — MIPI_CSI1_RX_D2P/MIPI_CSI1_RX_D2N [20]
MIPI_CSI1_D3P/MIPI_CSI1_D3N — AL31/AL32 — MIPI_CSI1_RX_D3P/MIPI_CSI1_RX_D3N [20]

MIPI_CSI1_AVCC0V75 — AA25 — VDD_0V75_S0
C1619 1uF/6.3V C0201
MIPI_CSI1_AVCC1V8 — AA26 — VCC_1V8_S0
C1621 100nF/10V C0201

Note:
建议优先使用U1000P这个模块的DPHY CSI_RX。
First use the DPHY_CSI_RX controller of U1000P.

MIPI_CSI_RX Configuration

Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* + *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0*
		MIPI_CSI_RX_D2-3 *MIPI_CSI_RX_CLK1*

Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

Note:
If not used:
Signal:leave floating
Power: Floating

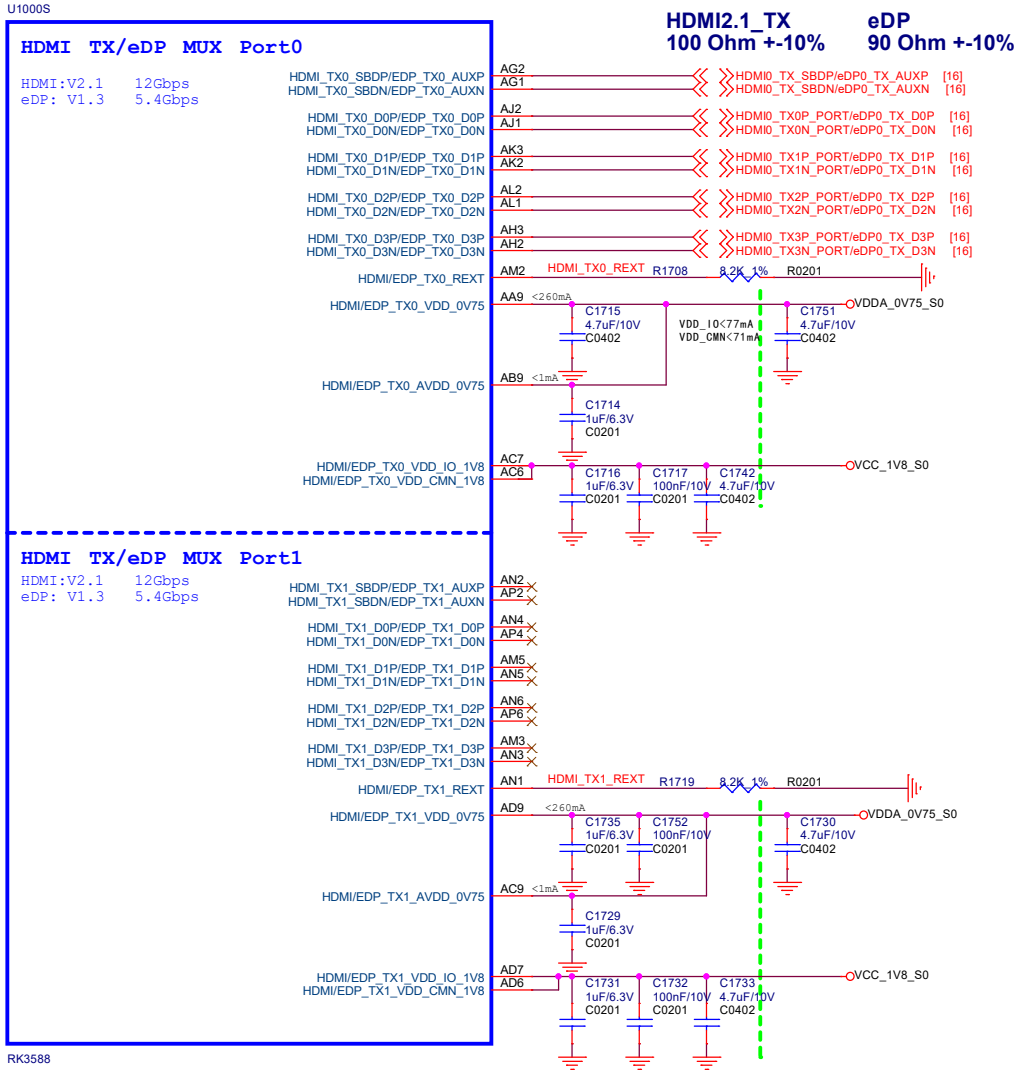
RK3588

armsom https://armsom.org/

Project:	ArmSoM-Sige7				
File:	RK3588_MIPI Interface				
Date:	Monday, December 25, 2023			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	8 of 24

RK3588_S(HDMI2.1 TX)

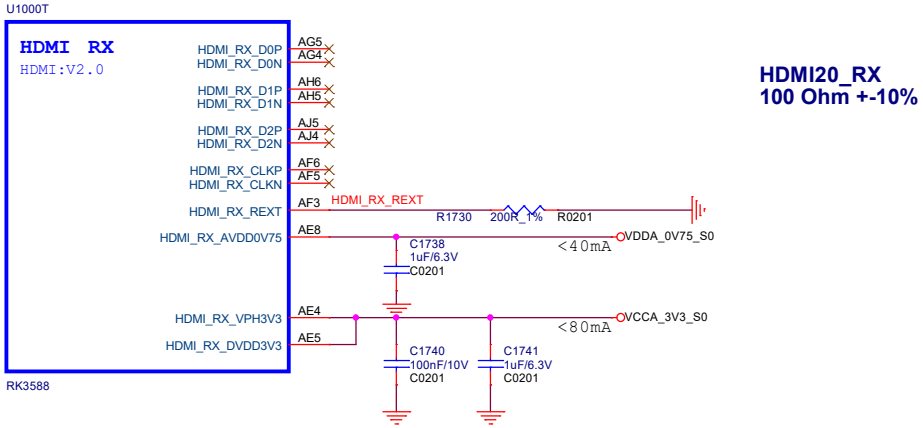
Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.



Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

Note:
If not used:
Signal:leave floating
Power: Floating or tie to VSS

RK3588_T(HDMI20 RX)



Note:
If not used:
Signal:leave floating
Power: Floating

armsom https://armsom.org/					
Project:	ArmSoM-Sige7				
File:	RK3588_HDMI/eDP Interface				
Date:	Monday, December 18, 2023			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	9 of 24

RK3588_N(PCIE20)

U1000N

Note:
If not used:
Signal:leave floating
Power: Floating

PCIE20/SATA30 Mux0

PCIe20x1_2
1Lane(RC)--4(1L2)

SATA30 HOST
Controller0

MUX

input or output

PCIE20_0_REFCLKP / PCIE20_0_REFCLKN — L32 / L33 — PCIE20_0_REFCLKP [17] / PCIE20_0_REFCLKN [17]
PCIE20_0_TXP/SATA30_0_TXP / PCIE20_0_TXN/SATA30_0_TXN — M34 / M33 — PCIE20_0_TXP [17] / PCIE20_0_TXN [17]
PCIE20_0_RXP/SATA30_0_RXP / PCIE20_0_RXN/SATA30_0_RXN — N33 / N34 — PCIE20_0_RXP [17] / PCIE20_0_RXN [17]

PCIE20_SATA30_0_AVDD_0V85 — M28 — C1810 10uF/10V C0402 — VDDA_0V85_S0
PCIE20_SATA30_0_AVDD_1V8 — M27 — C1808 1uF/6.3V C0201 — VCCA_1V8_S0

CLK Differential Pair:
100 Ohm± 10 %
DATA Differential Pair:
PCIE20: 85 Ohm ± 10 %
SATA30: 100 Ohm ± 10 %
USB30: 90ohm ± 10 %

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30 Mux1

PCIe30x1_0
1Lane(RC)--2(1L0)

SATA30 HOST
Controller1

MUX

input or output

PCIE20_1_REFCLKP / PCIE20_1_REFCLKN — H32 / H33 — PCIE20_1_REFCLKP [18] / PCIE20_1_REFCLKN [18]
PCIE20_1_TXP/SATA30_1_TXP / PCIE20_1_TXN/SATA30_1_TXN — K33 / K34 — PCIE20_1_TXP [18] / PCIE20_1_TXN [18]
PCIE20_1_RXP/SATA30_1_RXP / PCIE20_1_RXN/SATA30_1_RXN — J33 / J34 — PCIE20_1_RXP [18] / PCIE20_1_RXN [18]

PCIE20_SATA30_1_AVDD_0V85 — L28 — C1818 100nF/10V C0201 — VDDA_0V85_S0
PCIE20_SATA30_1_AVDD_1V8 — L27 — C1816 100nF/10V C0201 — VCCA_1V8_S0

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30/USB30 HOST Mux2

PCIe30x1_1
1Lane(RC)--3(1L1)

SATA30 HOST
Controller2

USB30 HOST
Controller2

MUX

input or output

PCIE20_2_REFCLKP / PCIE20_2_REFCLKN — G31 / G30 — PCIE20_2_REFCLKP [16] / PCIE20_2_REFCLKN [16]
PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP / PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN — H30 / H29 — PCIE20_2_TXP [16] / PCIE20_2_TXN [16]
PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP / PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN — J31 / J30 — PCIE20_2_RXP [16] / PCIE20_2_RXN [16]

PCIE20_SATA30_USB30_2_AVDD_0V85 — K28 — C1806 1uF/6.3V C0201 — VDDA_0V85_S0
PCIE20_SATA30_USB30_2_AVDD_1V8 — K27 — C1804 1uF/6.3V C0201 — VCCA_1V8_S0

PCIE20:Gen1/Gen2
USB 30:Gen1
SATA30:Gen1/Gen2/Gen3

RK3588

Note:
The SATA differential trace impedance is 100 OHM
The SATA trace length is less than 5 inch

RK3588_O(PCIE30)

Note:
Only PCIE3.0 Controller 0 support RC and EP,Other controller only support RC Mode.

U1000O

PCIE30X4

PCIe30X4
4Lane(DM)--0(4L)

PCIe30x1_0
1Lane(RC)--2(1L0)

PCIE20/SATA30 MUX1

PCIe30x2
2Lane(RC)--1(2L)

PCIe30x1_1
1Lane(RC)--3(1L1)

PCIE20/SATA30/USB30 MUX2

PCIE30:
PCIe1.1(2.5Gbps)
PCIe2.1(5Gbps)
PCIe3.0(8Gbps)

PCIE30 PORT0

input PCIE30_PORT0_REF_CLKP / PCIE30_PORT0_REF_CLKN — E33 / E34 — PCIE30_PORT0_REFCLKP_IN [19] / PCIE30_PORT0_REFCLKN_IN [19]

Lane0
PCIE30_PORT0_TX0P / PCIE30_PORT0_TX0N — D32 / D33 — PCIE30_PORT0_TX0P [19] / PCIE30_PORT0_TX0N [19]
PCIE30_PORT0_RX0P / PCIE30_PORT0_RX0N — G33 / G34 — PCIE30_PORT0_RX0P [19] / PCIE30_PORT0_RX0N [19]

Lane1
PCIE30_PORT0_TX1P / PCIE30_PORT0_TX1N — C33 / C34 — PCIE30_PORT0_TX1P [19] / PCIE30_PORT0_TX1N [19]
PCIE30_PORT0_RX1P / PCIE30_PORT0_RX1N — F32 / F33 — PCIE30_PORT0_RX1P [19] / PCIE30_PORT0_RX1N [19]

PCIE30_PORT0_RESREF — B34 — PCIE30_0_REF — R1801 200R 1% R0201
PCIE30_PORT0_AVDD0V75 — G24 — VDD_0V75_S0
C1802 1uF/6.3V C0201 / C1803 4.7uF/10V C0402
PCIE30_PORT0_AVDD1V8 — G23 — VCCA_1V8_S0
C1800 1uF/6.3V C0201 / C1801 4.7uF/10V C0402

PCIE30 PORT1

input PCIE30_PORT1_REF_CLKP / PCIE30_PORT1_REF_CLKN — A28 / B28 — PCIE30_PORT1_REFCLKP_IN [19] / PCIE30_PORT1_REFCLKN_IN [19]

Lane0
PCIE30_PORT1_TX0P / PCIE30_PORT1_TX0N — B30 / A30 — PCIE30_PORT1_TX2P [19] / PCIE30_PORT1_TX2N [19]
PCIE30_PORT1_RX0P / PCIE30_PORT1_RX0N — B32 / A32 — PCIE30_PORT1_RX2P [19] / PCIE30_PORT1_RX2N [19]

Lane1
PCIE30_PORT1_TX1P / PCIE30_PORT1_TX1N — C29 / B29 — PCIE30_PORT1_TX3P [19] / PCIE30_PORT1_TX3N [19]
PCIE30_PORT1_RX1P / PCIE30_PORT1_RX1N — C31 / B31 — PCIE30_PORT1_RX3P [19] / PCIE30_PORT1_RX3N [19]

PCIE30_PORT1_RESREF — A33 — PCIE30_1_REF — R1807 200R 1% R0201
PCIE30_PORT1_AVDD0V75 — H24 — VDD_0V75_S0
C1814 1uF/6.3V C0201 / C1815 4.7uF/10V C0402
PCIE30_PORT1_AVDD1V8 — H23 — VCCA_1V8_S0
C1812 100nF/10V C0201 / C1813 4.7uF/10V C0402

CLK Differential Pair:
100 Ohm ± 10 %
DATA Differential Pair:
PCIE30: 85 Ohm ± 10 %

RK3588

Note:

If Port0 and Port1 are not used,
Port0 and Port1 REF_CLKP/N: Leave floating or tie to VSS
Port0 and Port1 Other Signal: Leave floating
Port0 and Port1 Power: Leave floating or tie to VSS

If Port0 is used ,Port1 is not used,
Port1 REF_CLKP/N: Leave floating or tie to VSS
Port1 Other Signal: Leave floating
Port1 Power: Must supply power

If Port1 is used ,Port0 is not used,
Port0 REF_CLKP/N: Leave floating or tie to VSS
Port0 Other Signal: Leave floating
Port0 Power: Must supply power

armsom https://armsom.org/					
Project:	ArmSoM-Sige7				
File:	RK3588_PCIE30/PCIE20/SATA30				
Date:	Monday, December 25, 2023			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	10 of 24

RK3588_J(VCCIO5 Domain)

U1000J

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM10_M0	SPI4_MISO_M1		I2C6_SDA_M4	PSPI_D0_M2	I2S3_MCLK	SDIO_D0_M1	GMAC1_TXD2	GPIO3_A0_u
AUDDSM_LN	SPI4_MOSI_M1	PWM11_IR_M0	I2C6_SCL_M4	PSPI_D1_M2	I2S3_SCLK	SDIO_D1_M1	GMAC1_TXD3	GPIO3_A1_u
AUDDSM_LP	SPI4_CLK_M1	UART8_TX_M1		PSPI_D2_M2	I2S3_LRCK	SDIO_D2_M1	GMAC1_RXD2	GPIO3_A2_u
AUDDSM_RN	SPI4_CS0_M1	UART8_RX_M1		PSPI_D3_M2	I2S3_SDO	SDIO_D3_M1	GMAC1_RXD3	GPIO3_A3_u
AUDDSM_RP	SPI4_CS1_M1	UART8_RTSN_M1			I2S3_SDI	SDIO_CMD_M1	GMAC1_TXCLK	GPIO3_A4_d
	MIPI_CAMERA0_CLK_M1	UART8_CTSN_M1	I2C4_SDA_M0	PSPI_CLK_M2		SDIO_CLK_M1	GMAC1_RXCLK	GPIO3_A5_d
	MIPI_CAMERA1_CLK_M1		I2C4_SCL_M0				ETH1_REFCLKO_25M	GPIO3_A6_d
PWM8_M0	MIPI_CAMERA2_CLK_M1						GMAC1_RXD0	GPIO3_A7_u
PWM9_M0	MIPI_CAMERA3_CLK_M1						GMAC1_RXD1	GPIO3_B0_u
PWM2_M1	MIPI_CAMERA4_CLK_M1	UART2_TX_M2					GMAC1_RXDV_CRS	GPIO3_B1_d
PWM3_IR_M1		UART2_RX_M2			I2S2_SDI_M1		GMAC1_TXER	GPIO3_B2_d
		UART2_RTSN			I2S2_SDO_M1		GMAC1_TXD0	GPIO3_B3_u
		UART2_CTSN			I2S2_MCLK_M1		GMAC1_TXD1	GPIO3_B4_u
PWM12_M0	CAN1_RX_M0	UART3_TX_M1			I2S2_SCLK_M1		GMAC1_TXEN	GPIO3_B5_u
PWM13_M0	CAN1_TX_M0	UART3_RX_M1			I2S2_LRCK_M1		GMAC1_MCLKINOUT	GPIO3_B6_d
			I2C3_SCL_M1	SPI1_MOSI_M1	HDMI_TX1_HPD_M1		GMAC1_PTP_REF_CLK	GPIO3_B7_d
		UART7_TX_M1	I2C3_SDA_M1	SPI1_MISO_M1			GMAC1_PPSTRIG	GPIO3_C0_d
	PCIE30X2_BUTTON_RSTN	UART7_RX_M1		SPI1_CLK_M1			GMAC1_PPSCLK	GPIO3_C1_d
PWM14_M0		UART7_RTSN_M1	I2C8_SCL_M4	SPI1_CS0_M1		MIPI_TE0	GMAC1_MDC	GPIO3_C2_d
PWM15_IR_M0		UART7_CTSN_M1	I2C8_SDA_M4	SPI1_CS1_M1		MIPI_TE1	GMAC1_MDIO	GPIO3_C3_d
CAN2_RX_M0	PCIE30X4_CLKREQN_M2	UART5_TX_M1	FSPI_CS0N_M2	SPI3_CS0_M3	HDMI_TX1_CEC_M2		CIF_D8	GPIO3_C4_u
CAN2_TX_M0	PCIE30X4_WAKEN_M2	UART5_RX_M1	FSPI_CS1N_M2	SPI3_CS1_M3	HDMI_TX1_SDA_M1		CIF_D9	GPIO3_C5_u
	PCIE30X4_PERSTN_M2			SPI3_MISO_M3	HDMI_TX1_SCL_M1		CIF_D10	GPIO3_C6_u
	PCIE20X1_2_CLKREQN_M0		I2C5_SCL_M0	SPI3_MOSI_M3	HDMI_TX0_SCL_M2		CIF_D11	GPIO3_C7_u
PWM8_M2	PCIE20X1_2_WAKEN_M0	UART4_RX_M1	I2C5_SDA_M0	SPI3_CLK_M3	HDMI_TX0_SDA_M2		CIF_D12	GPIO3_D0_u
PWM9_M2	PCIE20X1_2_PERSTN_M0	UART4_TX_M1		SPI0_MISO_M3	HDMI_RX_CEC_M1		CIF_D13	GPIO3_D1_d
	PCIE30X2_CLKREQN_M2	UART9_RTSN_M2	I2C7_SCL_M2	SPI0_MOSI_M3	HDMI_RX_SCL_M1		CIF_D14	GPIO3_D2_d
PWM10_M2	PCIE30X2_WAKEN_M2	UART9_CTSN_M2	I2C7_SDA_M2	SPI0_CLK_M3	HDMI_RX_SDA_M1		CIF_D15	GPIO3_D3_d
	PCIE30X2_PERSTN_M2	UART9_RX_M2		SPI0_CS0_M3	HDMI_RX_HPDOUT_M1/	HDMI_TX0_HPD_M1/	MCU_JTAG_TCK_M1	GPIO3_D4_d
PWM11_IR_M3	PCIE30X4_BUTTON_RSTN	UART9_TX_M2		SPI0_CS1_M3	DP1_HPDIN_M0		MCU_JTAG_TMS_M1	GPIO3_D5_d

AA29	CM2_RST_L_3V3 [16]	GPIO3_A0_u
AA30	LCD_BL_EN_3V3 [20]	GPIO3_A1_u
AD27	MIPI_CSI1_PDN0_H_3V3 [22]	GPIO3_A2_u
AE27	MIPI_CSI1_PDN1_H_3V3 [22]	GPIO3_A3_u
AD28	UART8_RTSn_M1_BT_3V3 [22]	GPIO3_A4_d
AH30	MIPI_CAM0_CLKOUT_M1_3V3 [22]	GPIO3_A5_d
AH27	BT_REG_ON_H_3V3 [16]	GPIO3_A6_d
AG29	PWM8_M0_3V3 [22]	GPIO3_A7_u
AG28	PCIE_PERST_L_3V3 [17]	GPIO3_B0_u
AH29	I2S2_LRCK_RX_M1_3V3 [22]	GPIO3_B1_d
AE28	I2S2_SDI_M1_3V3 [22]	GPIO3_B2_d
AC28	I2S2_SDO_M1_3V3 [22]	GPIO3_B3_u
AC29	CC_INT_L_3V3 [21]	GPIO3_B4_u
AD29	I2S2_SCLK_TX_M1_3V3 [22]	GPIO3_B5_u
AE29	I2S2_LRCK_TX_M1_3V3 [22]	GPIO3_B6_d
AA28	SPI1_MISO_M1_3V3 [22]	GPIO3_B7_d
Y29	SPI1_MOSI_M1_3V3 [22]	GPIO3_C0_d
Y27	SPI1_CLK_M1_3V3 [22]	GPIO3_C1_d
Y31	SPI1_CS0_M1_3V3 [22]	GPIO3_C2_d
Y30	SPI1_CS1_M1_3V3 [22]	GPIO3_C3_d
AH26	CC2_INT_L_3V3 [21]	GPIO3_C4_u
AH25	HDMITX1_SDA_M1	GPIO3_C5_u
AG26	HDMITX1_SCL_M1	GPIO3_C6_u
AJ24	PCIE20_1_2_CLKREQn_M1_L_3V3 [17]	GPIO3_C7_u
AH24	PCIE20_1_2_WAKEn_M1_L_3V3 [17]	GPIO3_D0_u
AG23	HDMI_RX_CEC	GPIO3_D1_d
AG25	PCIE30X2_CLKREQN_M2 [16]	GPIO3_D2_d
AG24	PCIE30X2_WAKEN_M2 [16]	GPIO3_D3_d
AA27	PCIE30X2_PERSTN_M2 [16]	GPIO3_D4_d
AB28	HOST_WAKE_BT_H_3V3 [16]	GPIO3_D5_d

VCCIO5_1V8 — W25 — C1903 100nF/10V C0201 — VCC_1V8_S0

VCCIO5 — W26 — C1902 100nF/10V C0201 — VCC_3V3_S0

RK3588

RK3588_K(VCCIO6 Domain)

U1000K

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

	SPI0_MISO_M1	UART9_RTSN_M1			I2S1_MCLK_M0	PCIE30X1_1_CLKREQN_M1	BT1120_D0	CIF_D0	GPIO4_A0_d
	SPI0_MOSI_M1	UART9_CTSN_M1			I2S1_SCLK_M0	PCIE30X1_1_WAKEN_M1	BT1120_D1	CIF_D1	GPIO4_A1_d
	SPI0_CLK_M1				I2S1_LRCK_M0	PCIE30X1_1_PERSTN_M1	BT1120_D2	CIF_D2	GPIO4_A2_d
		UART0_TX_M2				PCIE30X1_0_CLKREQN_M1	BT1120_D3	CIF_D3	GPIO4_A3_d
	SPI2_MISO_M1	UART0_RX_M2	I2C3_SCL_M2			PCIE30X1_0_WAKEN_M1	BT1120_D4	CIF_D4	GPIO4_A4_d
	SPI2_MOSI_M1	UART3_TX_M2	I2C3_SDA_M2		I2S1_SDI0_M0	PCIE30X1_0_PERSTN_M1	BT1120_D5	CIF_D5	GPIO4_A5_d
	SPI2_CLK_M1	UART3_RX_M2	I2C5_SCL_M2		I2S1_SDI1_M0	PCIE30X2_CLKREQN_M1	BT1120_D6	CIF_D6	GPIO4_A6_d
	SPI2_CS0_M1		I2C5_SDA_M2		I2S1_SDI2_M0	PCIE30X2_WAKEN_M1	BT1120_D7	CIF_D7	GPIO4_A7_d
	SPI2_CS1_M1	UART8_TX_M0	I2C6_SDA_M3		I2S1_SDI3_M0	PCIE30X2_PERSTN_M1	BT1120_CLKOUT	CIF_CLKIN	GPIO4_B0_d
SATA2_ACT_LED_M0	SPDIF1_TX_M1	SPI0_CS1_M1	UART8_RX_M0	I2C6_SCL_M3		I2S1_SDO0_M0	PCIE30X1_0_BUTTON_RSTN		MIPI_CAMERA0_CLK_M0	GPIO4_B1_u
CAN1_RX_M1	PWM14_M1	SPI0_CS0_M1	UART8_RTSN_M0	I2C7_SCL_M3		I2S1_SDO1_M0	PCIE30X1_1_BUTTON_RSTN	BT1120_D8	CIF_HREF	GPIO4_B2_u
CAN1_TX_M1	PWM15_IR_M1		UART8_CTSN_M0	I2C7_SDA_M3		I2S1_SDO2_M0	PCIE20X1_2_BUTTON_RSTN	BT1120_D9	CIF_VSYNC	GPIO4_B3_u
SPDIF0_TX_M1	PWM1_IR_M1	DP0_HPDIN_M0	UART9_TX_M1			I2S1_SDO3_M0	PCIE30X4_CLKREQN_M1	BT1120_D10	CIF_CLKOUT	GPIO4_B4_u
SATA1_ACT_LED_M0	PWM12_M1	SPI1_MISO_M1	UART9_RX_M1			HDMI_RX_CEC_M0	PCIE30X4_WAKEN_M1	BT1120_D11		GPIO4_B5_d
SATA0_ACT_LED_M0	PWM13_M1	SPI1_MOSI_M1		I2C5_SCL_M1		HDMI_RX_HPDOUT_M0	PCIE30X4_PERSTN_M1	BT1120_D12		GPIO4_B6_d
		SPI1_CLK_M1		I2C5_SDA_M1		HDMI_TX0_SCL_M0	PCIE20X1_2_CLKREQN_M1	BT1120_D13		GPIO4_B7_u
		SPI3_CS0_M1		I2C8_SCL_M3		HDMI_TX0_SDA_M0	PCIE20X1_2_WAKEN_M1	BT1120_D14		GPIO4_C0_u
SPDIF1_TX_M2	PWM6_M1	SPI3_CS1_M1		I2C8_SDA_M3		HDMI_TX0_CEC_M0	PCIE20X1_2_PERSTN_M1	BT1120_D15		GPIO4_C1_d

AK30	CM1_RST_L_3V3 [16]	GPIO4_A0_d
AL30	HDMI1_TX_ON_H	GPIO4_A1_d
AM29		GPIO4_A2_d
AL29	PCIE30x1_0_CLKREQn_M1_L_3V3 [18]	GPIO4_A3_d
AL28	PCIE30x1_0_WAKEn_M1_L_3V3 [18]	GPIO4_A4_d
AK27	PCIE30x1_0_PERSTn_M1_L_3V3 [18]	GPIO4_A5_d
AL27	TYPEC0_SBU1_DC [21]	GPIO4_A6_d
AM27	TYPEC0_SBU2_DC [21]	GPIO4_A7_d
AK26	USB_HOST_PWREN_H_3V3 [21]	GPIO4_B0_d
AL24	HDMI0_TX_ON_H_3V3 [16]	GPIO4_B1_u
AK25	I2C7_SCL_M3_3V3 [22]	GPIO4_B2_u
AM25	I2C7_SDA_M3_3V3 [22]	GPIO4_B3_u
AL26	PCIE30X4_CLKREQn_M1_L_3V3 [19]	GPIO4_B4_u
AJ26	PCIE30X4_WAKEn_M1_L_3V3 [19]	GPIO4_B5_d
AJ27	PCIE30X4_PERSTn_M1_L_3V3 [19]	GPIO4_B6_d
AJ28	HDMITX0_SCL_M0_3V3 [16]	GPIO4_B7_u
AJ25	HDMITX0_SDA_M0_3V3 [16]	GPIO4_C0_u
AK24	HDMITX0_CEC_M0_3V3 [16]	GPIO4_C1_d

VCCIO6_1V8 — AC25 — C1909 100nF/10V C0201 — VCC_1V8_S0

VCCIO6 — AC26 — C1908 100nF/10V C0201 — VCC_3V3_S0

RK3588

RK3588_I(VCCIO4 Domain)

U1000I

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

		SPI4_MISO_M2	PCIE30X1_1_CLKREQN_M2/	DP0_HPDIN_M2		I2C2_SDA_M4	UART6_RX_M1	GPIO1_A0_d
SATA1_ACT_LED_M1		SPI4_MOSI_M2	PCIE30X1_1_WAKEN_M2	DP1_HPDIN_M2		I2C2_SCL_M4	UART6_TX_M1	GPIO1_A1_d
	PWM0_M2	SPI4_CLK_M2			VOP_POST_EMPTY	I2C4_SDA_M3	UART6_RTSN_M1	GPIO1_A2_d
	PWM1_M2	SPI4_CS0_M2		HDMI_TX1_SDA_M2		I2C4_SCL_M3	UART6_CTSN_M1	GPIO1_A3_d
		SPI2_MISO_M0		HDMI_TX1_SCL_M2				GPIO1_A4_d
		SPI2_MOSI_M0		HDMI_TX0_HPD_M0				GPIO1_A5_d
		SPI2_CLK_M0		HDMI_TX1_HPD_M0				GPIO1_A6_d
	PWM3_IR_M3	SPI2_CS0_M0	PCIE30X1_1_PERSTN_M2			PDM1_SDI0_M1		GPIO1_A7_u
		SPI2_CS1_M0	PCIE30X4_CLKREQN_M3			PDM1_SDI1_M1		GPIO1_B0_u
		SPI0_MISO_M2	PCIE30X4_WAKEN_M3			PDM1_SDI2_M1		GPIO1_B1_d
		SPI0_MOSI_M2	PCIE30X4_PERSTN_M3			PDM1_SDI3_M1	UART4_RX_M2	GPIO1_B2_d
SATA0_ACT_LED_M1		SPI0_CLK_M2	PCIE30X1_0_WAKEN_M2			PDM1_CLK1_M1	UART4_TX_M2	GPIO1_B3_d
		SPI0_CS0_M2	PCIE30X1_0_PERSTN_M2			PDM1_CLK0_M1	UART7_RX_M2	GPIO1_B4_u
		SPI0_CS1_M2	PCIE30X1_0_CLKREQN_M2/				UART7_TX_M2	GPIO1_B5_u
	HDMI_RX_HPDOUT_M2/	SPDIF0_TX_M0	PCIE30X2_WAKEN_M3	MIPI_CAMERA1_CLK_M0 /		I2C5_SCL_M3	UART1_TX_M1	GPIO1_B6_u
SATA2_ACT_LED_M1	HDMI_RX_CEC_M2	PWM13_M2	SPDIF1_TX_M0	PCIE30X2_PERSTN_M3	MIPI_CAMERA2_CLK_M0 /	I2C5_SDA_M3	UART1_RX_M1	GPIO1_B7_u
	HDMI_RX_SCL_M2	PWM14_M2			MIPI_CAMERA3_CLK_M0 /	I2C8_SCL_M2	UART1_RTSN_M1	GPIO1_D6_u
	HDMI_RX_SDA_M2	PWM15_IR_M3		PCIE30X2_CLKREQN_M3	MIPI_CAMERA4_CLK_M0 /	I2C8_SDA_M2	UART1_CTSN_M1	GPIO1_D7_u

A24	UART6-RX [16]	GPIO1_A0_d
A25	UART6-TX [16]	GPIO1_A1_d
A26	UART6-RTSN [16]	GPIO1_A2_d
A27	UART6-CTSN [16]	GPIO1_A3_d
B25	PCIE30x4_PWREN_H [19]	GPIO1_A4_d
B26	HDMITX0_HPDIN_M1 [16]	GPIO1_A5_d
C24	HDMITX1_HPDIN_M1	GPIO1_A6_d
C25	MIPI_CSI0_PDN1_H [20]	GPIO1_A7_u
C27	MIPI_CSI0_PDN0_H [20]	GPIO1_B0_u
D25	SPI0-MISO [22]	GPIO1_B1_d
D26	SPI0-MOSI [22]	GPIO1_B2_d
D27	SPI0-CLK [22]	GPIO1_B3_d
E24	SPI0-CS0 [22]	GPIO1_B4_u
E25	SPI0-CS1 [22]	GPIO1_B5_u
E26	MIPI_CAM1_CLKOUT [20]	GPIO1_B6_u
E27	GPIO1_B7 [20,22]	GPIO1_B7_u
F24	MIPI_CAM3_CLKOUT [20]	GPIO1_D6_u
F25	GPIO1_D7 [22]	GPIO1_D7_u

VCCIO4_1V8 — H20 — C1907 100nF/10V C0201 — VCC_1V8_S0

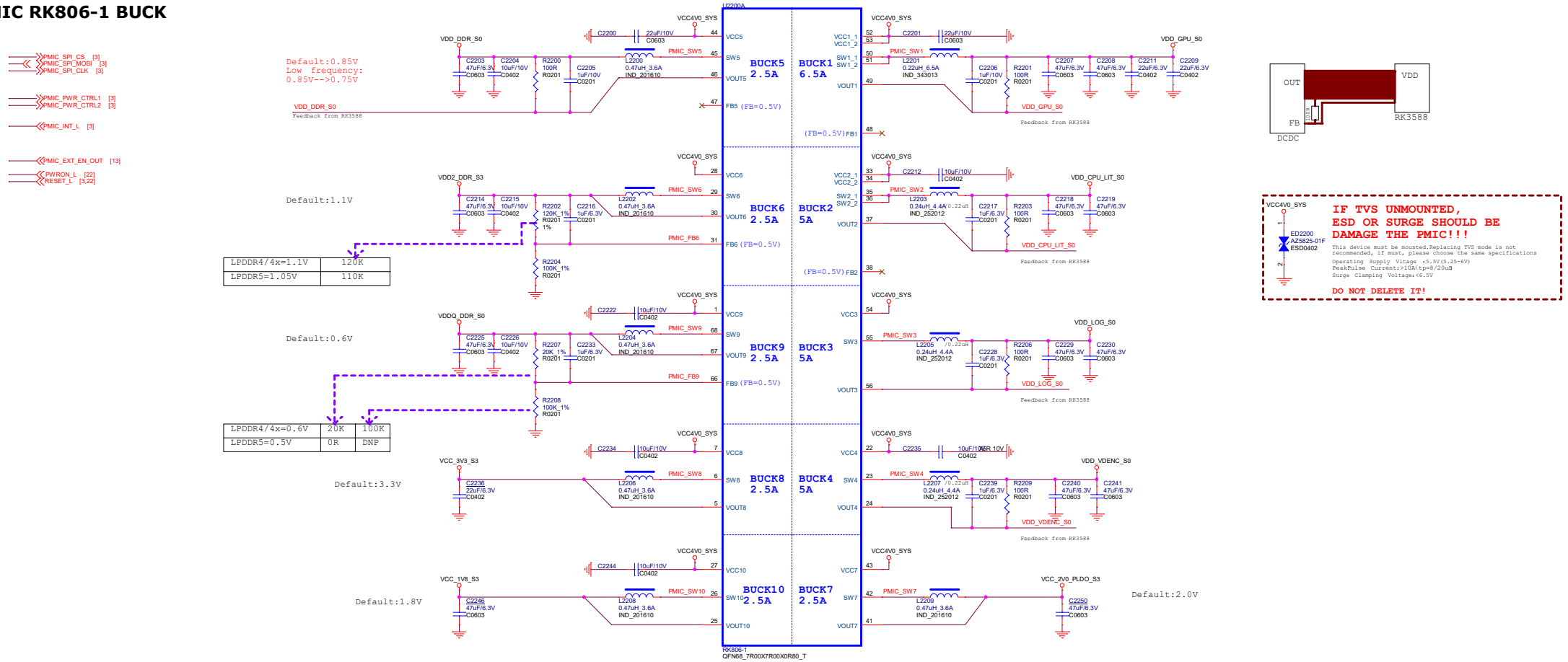
VCCIO4 — H21 — C1906 100nF/10V C0201 — VCC_1V8_S0

RK3588

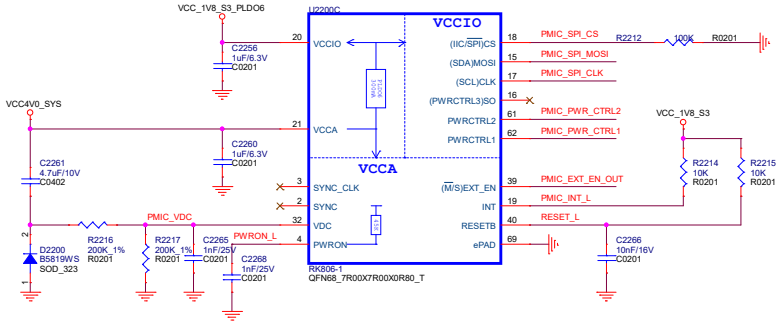
armsom https://armsom.org/

Project:	ArmSoM-Sige7		
File:	RK3588_1.8V/ 3.3V GPIO		
Date:	Monday, December 25, 2023	Rev:	V1.1
Designed by:	Park	Reviewed by: <Checker>	Sheet: 11 of 24

PMIC RK806-1 BUCK



PMIC RK806-1 Managerment

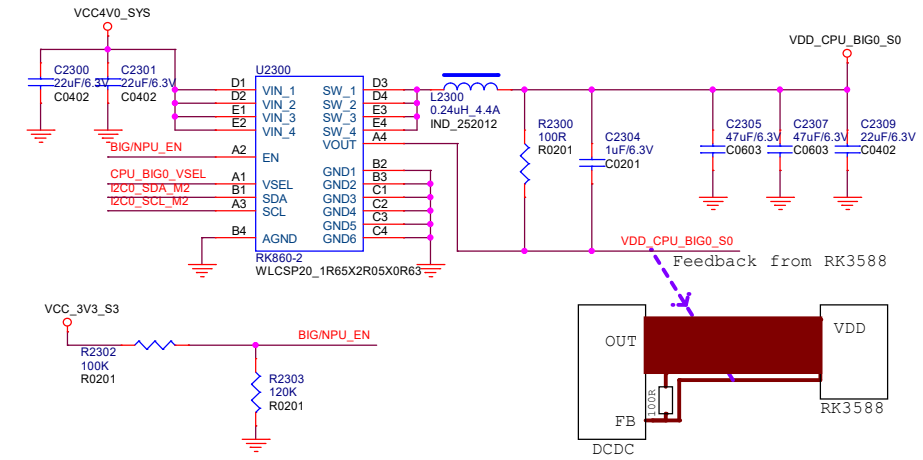


PMIC RK806-1 LDO

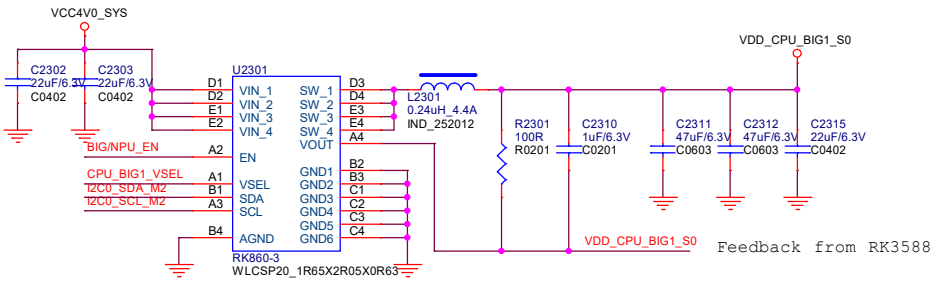
armsom https://armsom.org/

Project:	ArmSoM-Sige7		
File:	Power-PMIC_RK806-1		
Date:	Monday, December 25, 2023	Rev:	V1.1
Designed by:	Park	Reviewed by: <Checker>	Sheet: 12 of 24

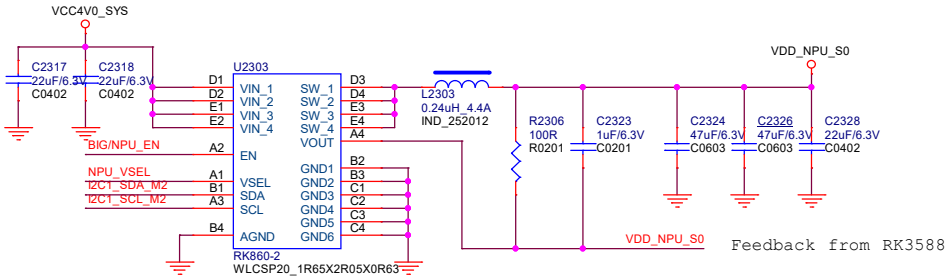
VDD_CPU_BIG0



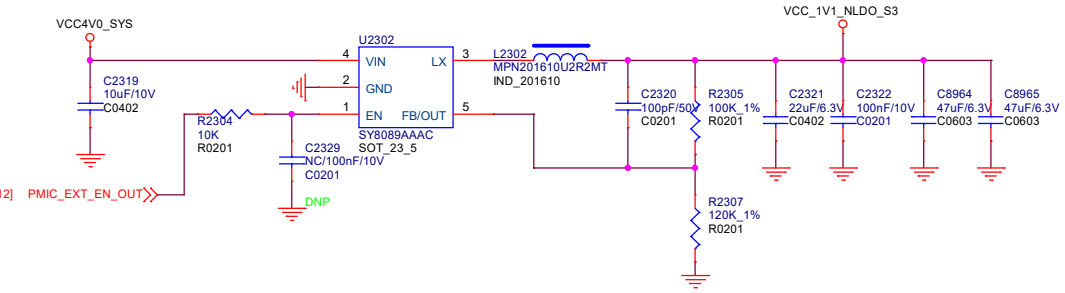
VDD_CPU_BIG1

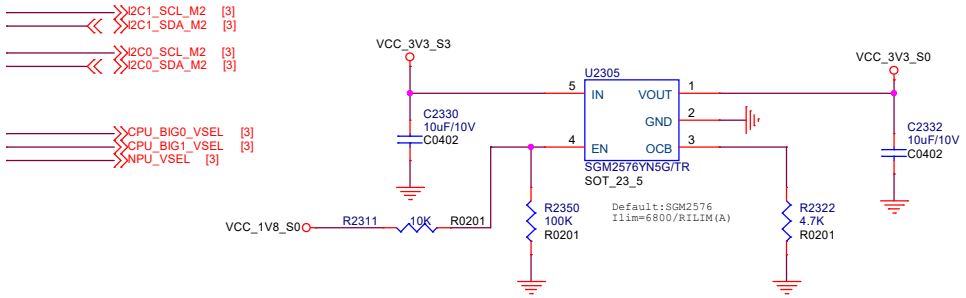


VDD_NPU



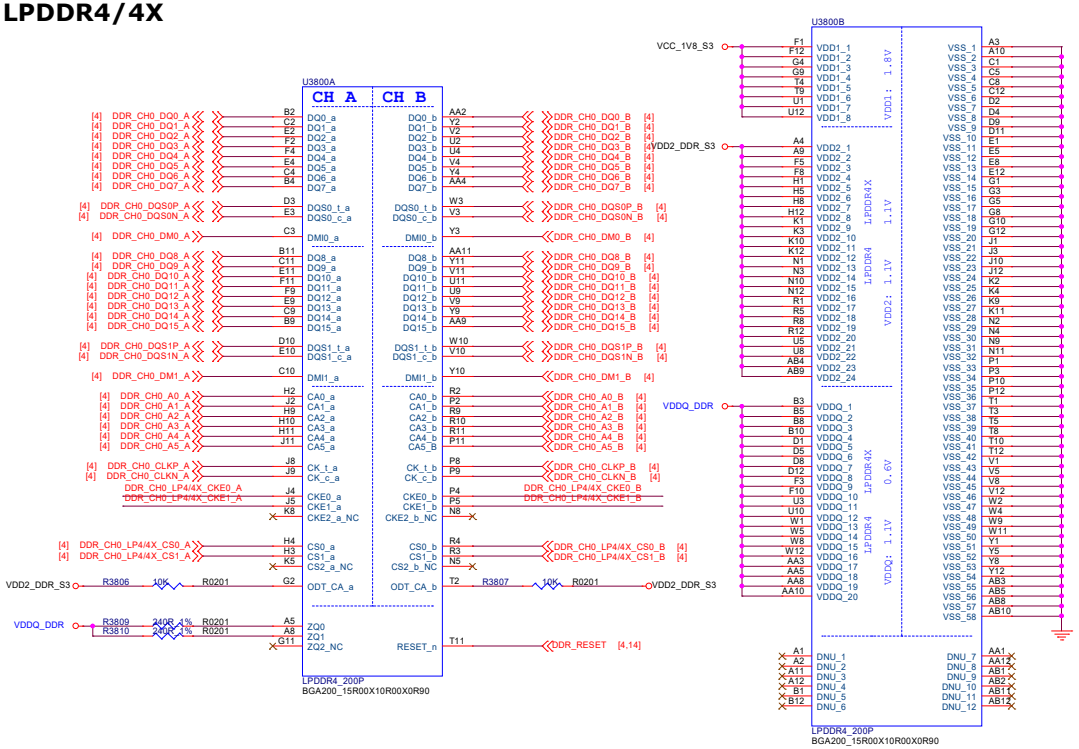
VCC_1V1_NLDO_S3

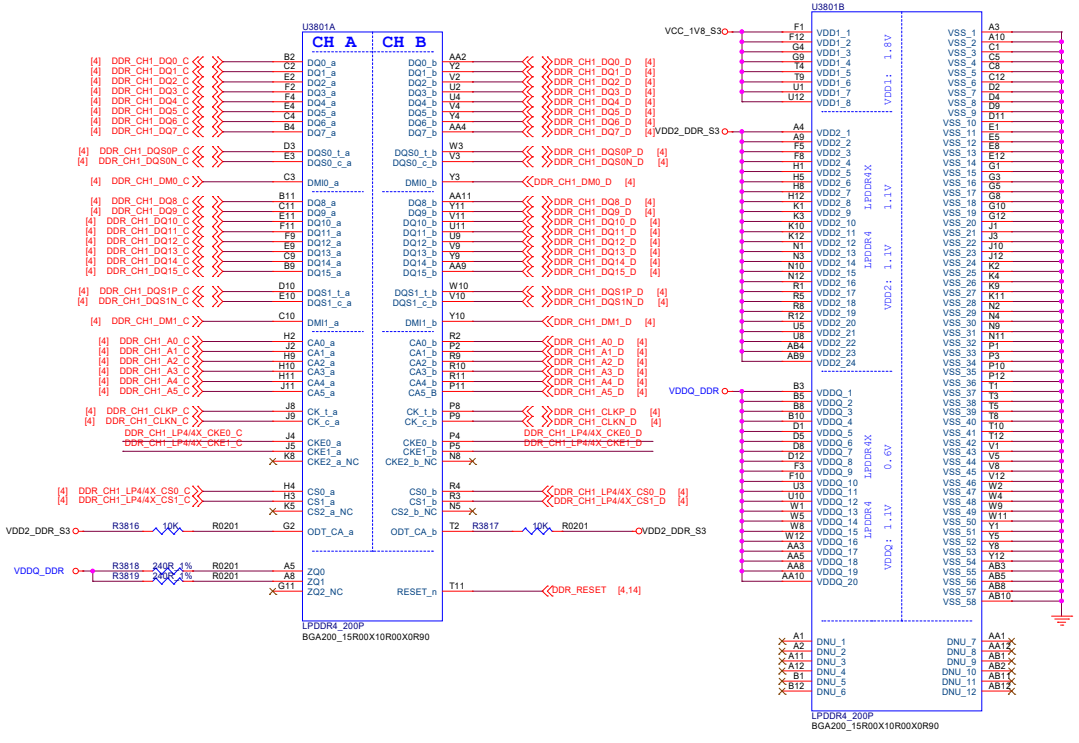




armsom https://armsom.org/					
Project:	ArmSoM-Sige7				
File:	Power_Ext Discrete				
Date:	Monday, December 25, 2023			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	13 of 24

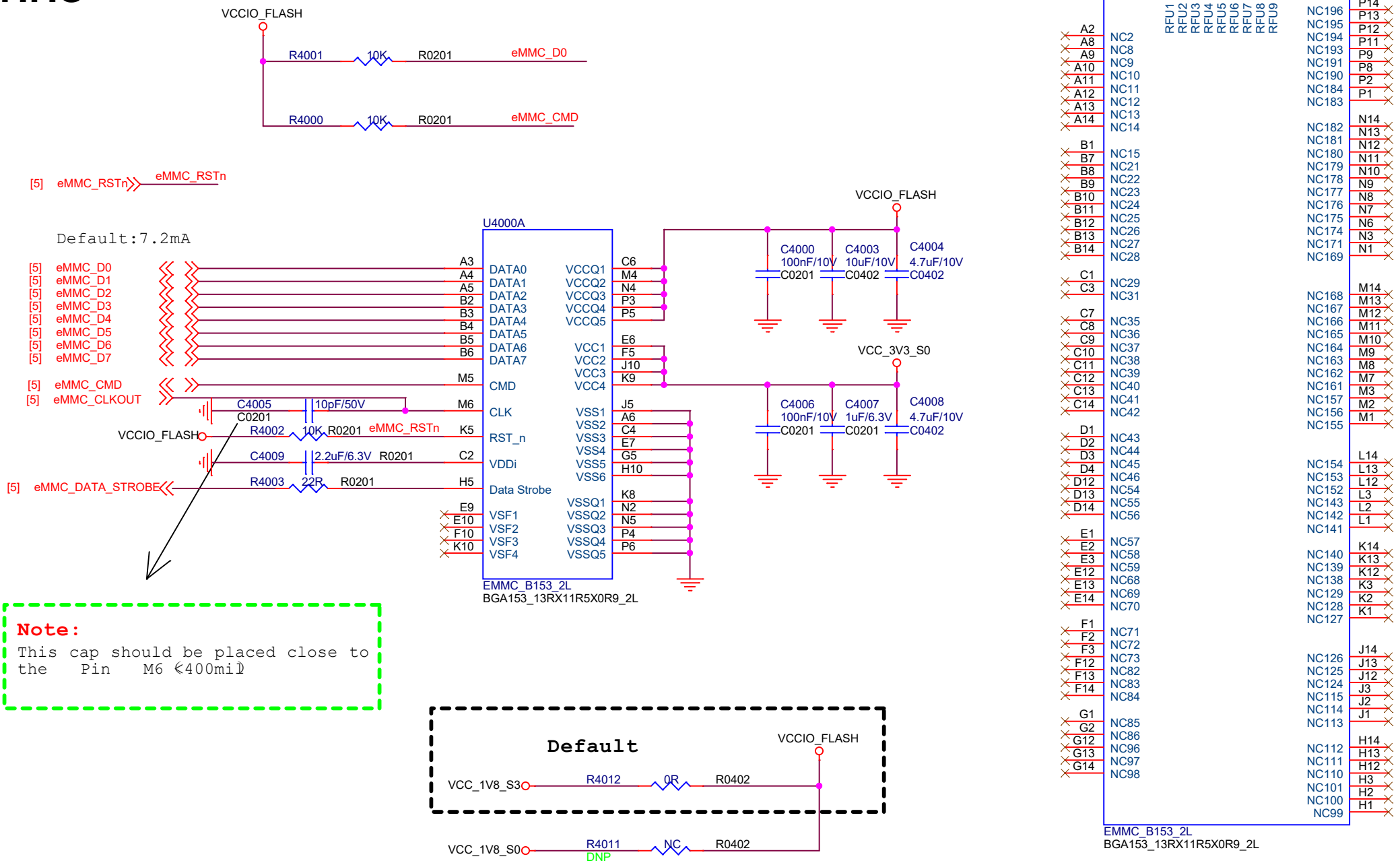
LPDDR4/4X





armsom	https://armsom.org/		
Project:	ArmSoM-Sige7		
File:	DRAM-LPDDR4X_200P_2X32bit		
Date:	Monday, December 25, 2023	Rev:	V1.1
Designed by: Park	Reviewed by: <Checker>	Sheet:	14 of 24

eMMC

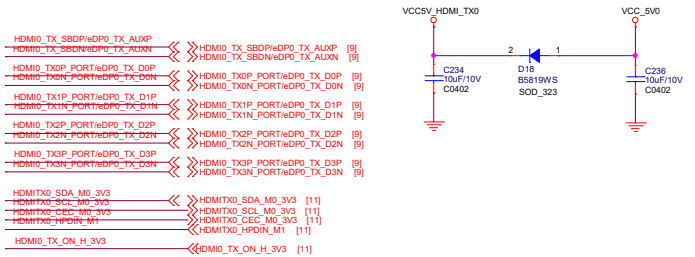


Note:
This cap should be placed close to the Pin M6 (400mil)

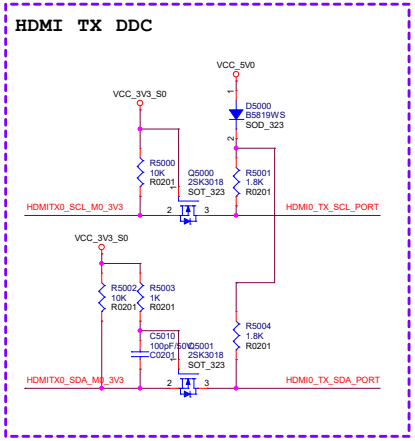
armsom https://armsom.org/

Project:	ArmSoM-Sige7				
File:	Flash-eMMC Flash				
Date:	Monday, December 25, 2023			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	15 of 24

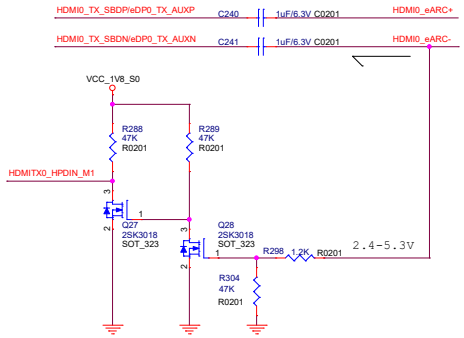
HDMI TX0



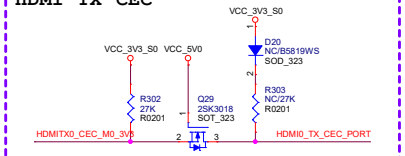
HDMI TX DDC



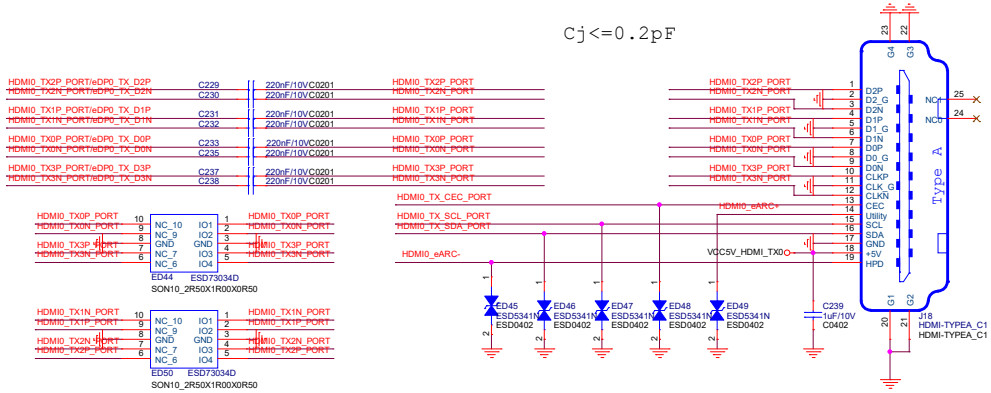
HDMI TX eARC



HDMI TX CEC



Cj<=0.2pF



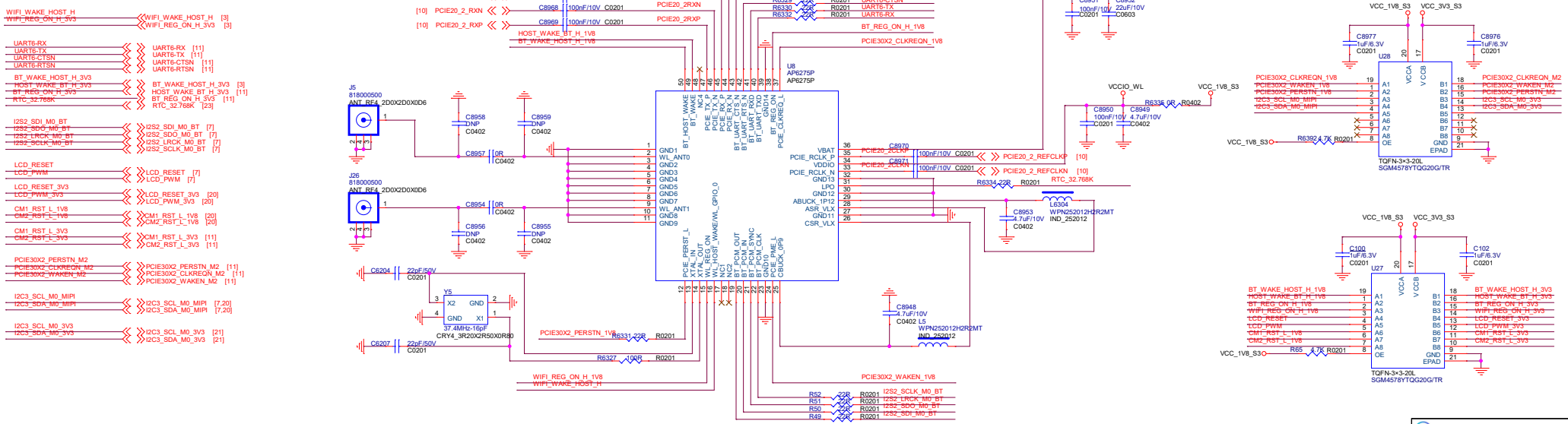
Note:

The controller only support AC coupled link In order to backward compatibility or to meet HDMI2.0 (1.4b) DC common mode spec and Voff, need do R based level-shift.

Switch on in HDMI2.0(TMDS) mode
Switch off in HDMI2.1(FRL) mode.

PCIE WIFI6/BT Module-2T2R

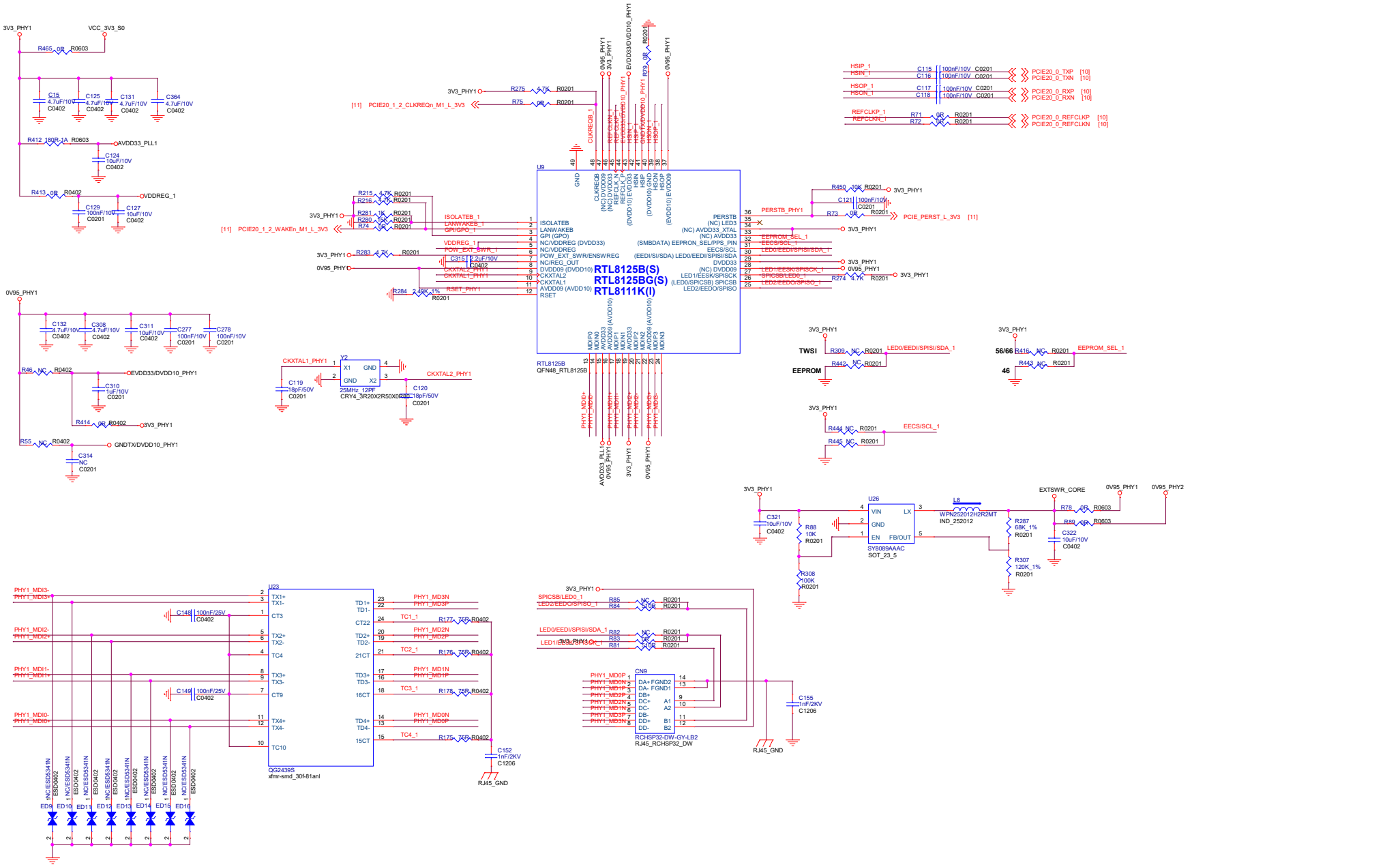
VBAT:(3.1-3.8V)/1.2A
VDDIO:(1.68-1.98V)/300mA.



armsom https://armsom.org/

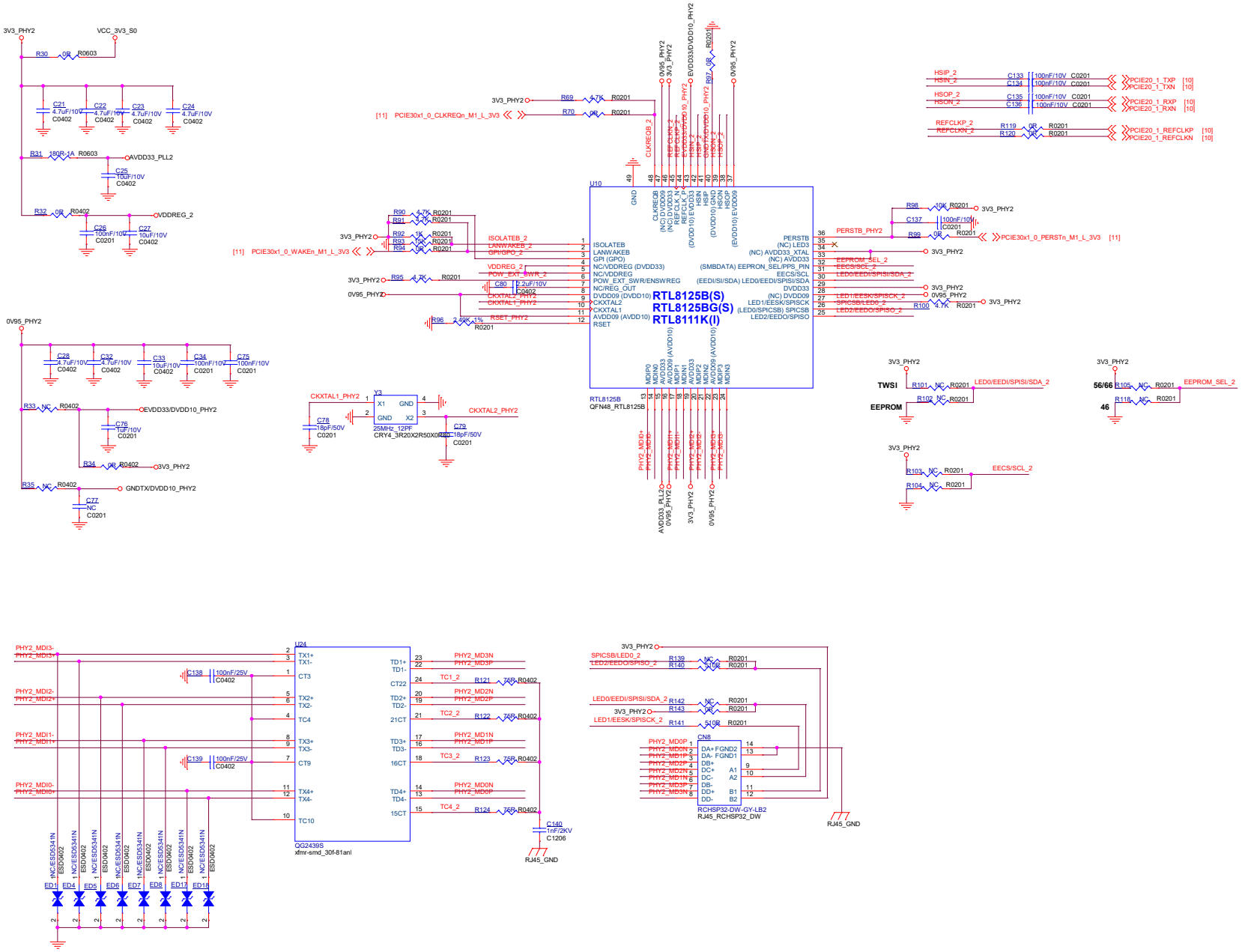
Project:	ArmSoM-Sige7
File:	HDMI_TX0_WIFI
Date:	Monday, December 25, 2023
Rev:	V1.1
Designed by:	Pink
Reviewed by:	<Checker>
Sheet:	16 of 24

PCIE TO RJ45



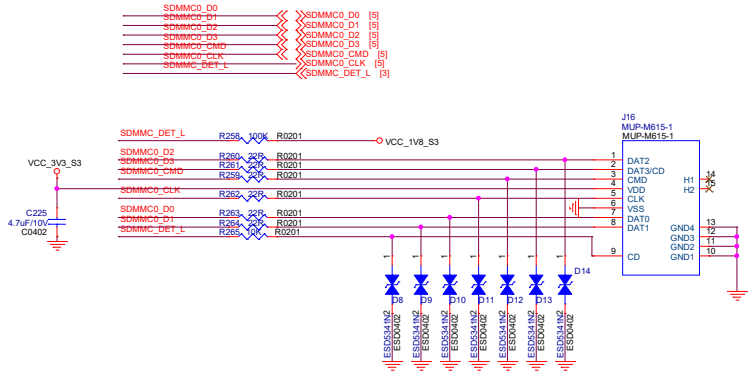
armsom	https://armsom.org/		
Project:	ArmSoM-Sige7		
File:	Ethernet_PCIE1		
Date:	Monday, December 25, 2023	Rev:	V1.1
Designed by:	Park	Reviewed by: <Checker>	Sheet: 17 of 24

PCIE TO RJ45

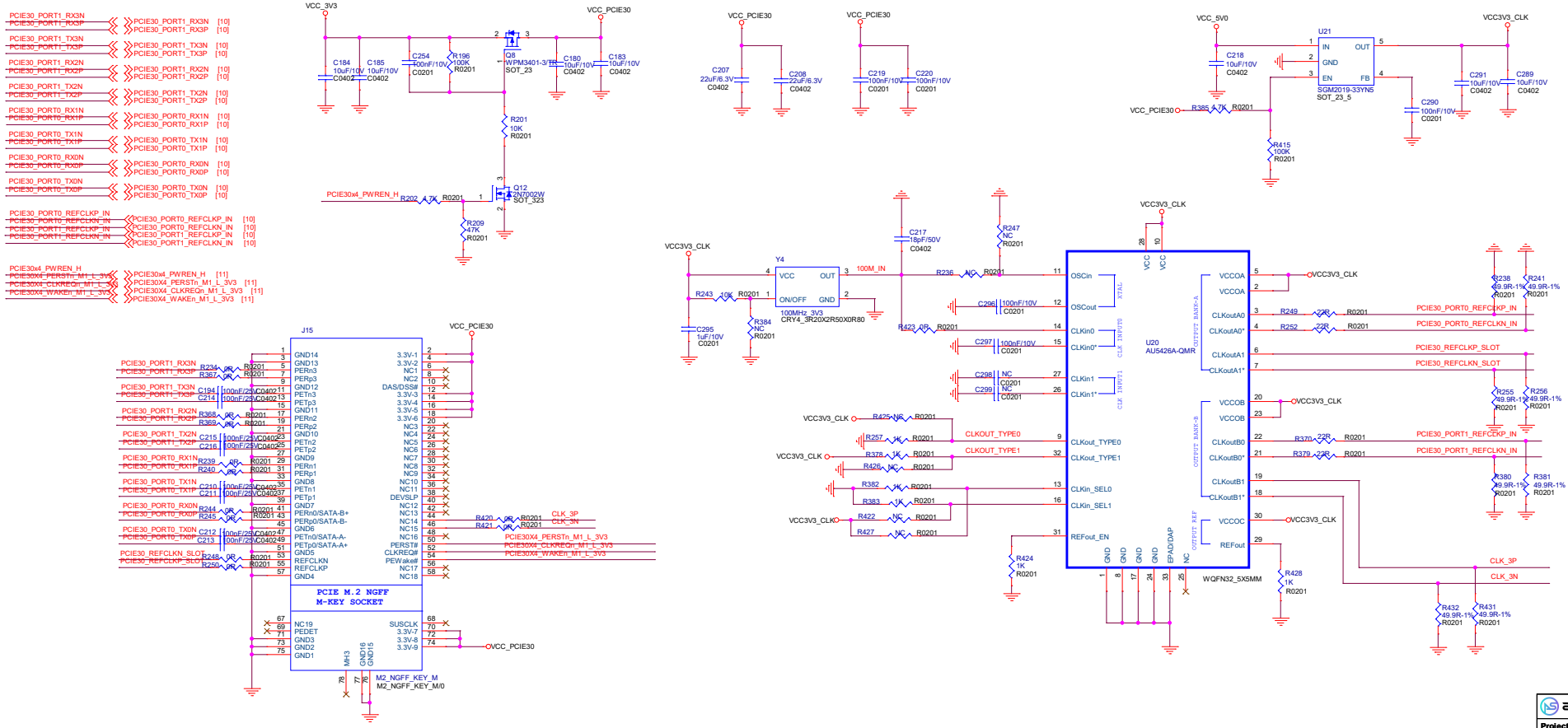


armsom	https://armsom.org/		
Project:	ArmSoM-Sige7		
File:	Ethernet_PCIE2		
Date:	Monday, December 25, 2023	Rev:	V1.1
Designed by:	Park	Reviewed by: <Checker>	Sheet: 18 of 24

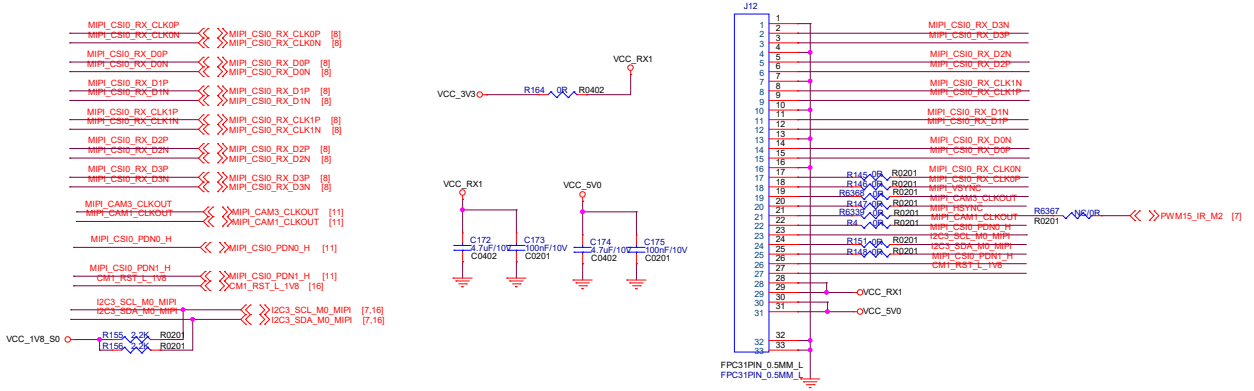
TF CARD



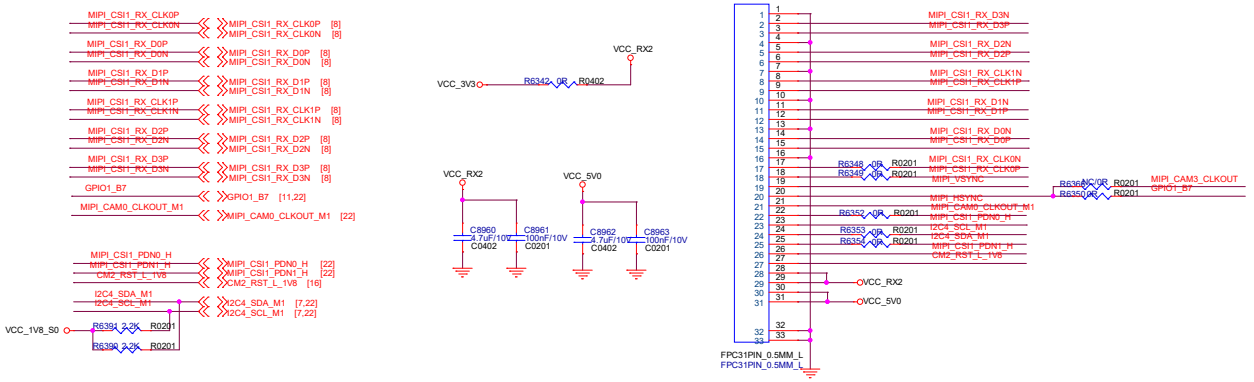
M.2_PCIE3.0



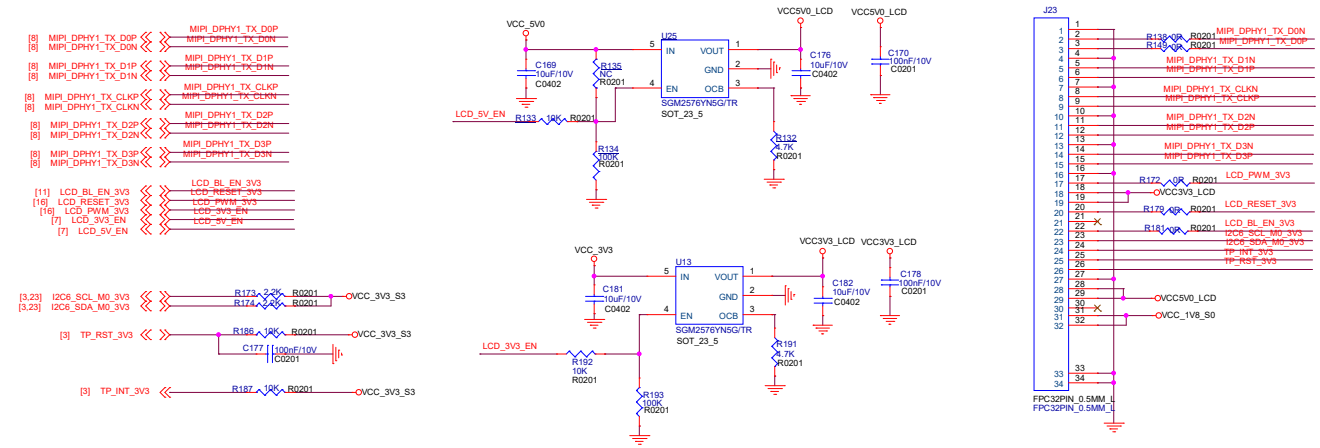
CSI0_MIPI



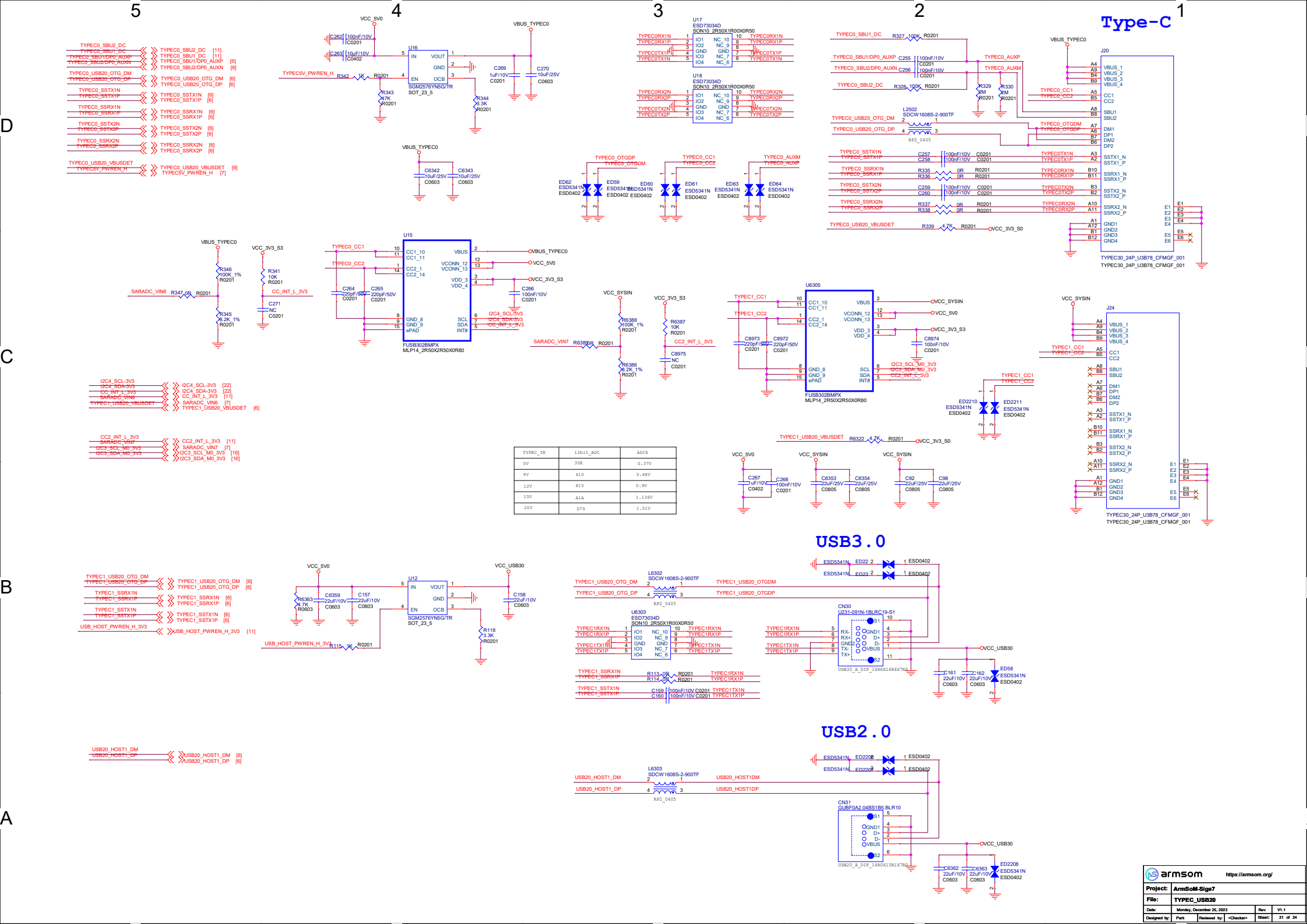
CS1_MIPI



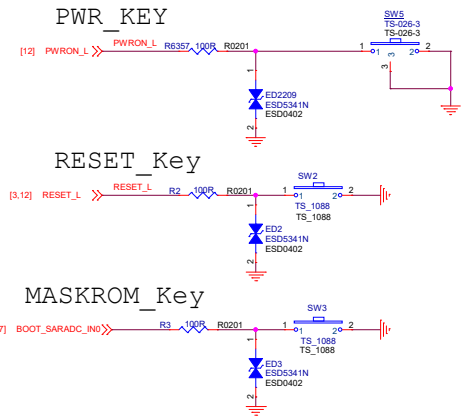
DSI_MIPI



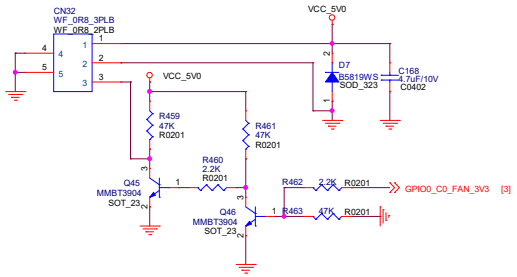
armsom	https://armsom.org/		
Project:	ArmSoM-Sige7		
File:	MIPI_RX_CSI/MIPI_DSI		
Date:	Monday, December 25, 2023	Rev:	V1.1
Designed by:	Patk	Reviewed by: <Checker>	Sheet: 20 of 24

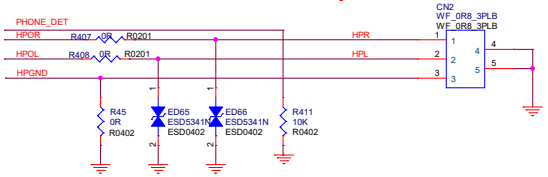

Type-C
USB3.0
USB2.0
TYPEC0_SBU2_DC
TYPEC0_SBU1_DC
TYPEC0_SBU1/DP0_AUXP
TYPEC0_SBU2/DP0_AUXN
TYPEC0_USB20_OTG_DM
TYPEC0_USB20_OTG_DP
TYPEC0_SSTX1N
TYPEC0_SSTX1P
TYPEC0_SSRX1N
TYPEC0_SSRX1P
TYPEC0_SSTX2N
TYPEC0_SSTX2P
TYPEC0_SSRX2N
TYPEC0_SSRX2P
TYPEC0_USB20_VBUSDET
TYPEC5V_PWREN_H
VCC_5V0
VBUS_TYPEC0
VCC_3V3_S3
VCC_SYSIN
VCC_USB30
TYPEC1_USB20_OTG_DM
TYPEC1_USB20_OTG_DP
TYPEC1_SSRX1N
TYPEC1_SSRX1P
TYPEC1_SSTX1N
TYPEC1_SSTX1P
TYPEC1_USB20_VBUSDET
USB_HOST_PWREN_H_3V3
USB20_HOST1_DM
USB20_HOST1_DP
SARADC_VIN6
SARADC_VIN7
I2C4_SCL-3V3
I2C4_SDA-3V3
CC_INT_L_3V3
I2C3_SCL_M0_3V3
I2C3_SDA_M0_3V3
U16
SGM2576YN5G/TR
SOT_23_5
U17
U18
ESD73034D
SON10_2R50X1R00X0R50
U15
FUSB302BMPX
MLP14_2R50X2R50X0R80
U6305
J20
J24
TYPEC30_24P_U3B78_CFMGF_001
L2502
SDCW1608S-2-900TF
L6302
L6303
RP2_0405
CN30
CN31
U231-091N-1BLRC19-S1
GUBF0A2.04BS1B5.BLR10
USB30_A_DIP_16R6X14R6X7R0
USB20_A_DIP_14R0X13R1X7R0
ESD5341N
ESD0402
TYPEC_IN
12bit_ADC
ADC6
5V
9V
12V
15V
20V
armsom
https://armsom.org/
Project: ArmSoM-Sige7
File: TYPEC_USB20
Date: Monday, December 25, 2023
Rev: V1.1
Designed by: Park
Reviewed by: <Checker>
Sheet: 21 of 24

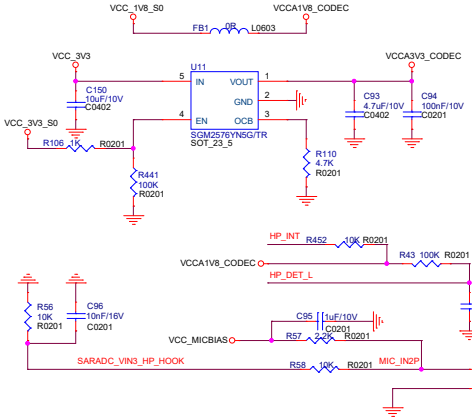
KEY

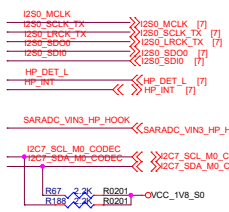


FAN

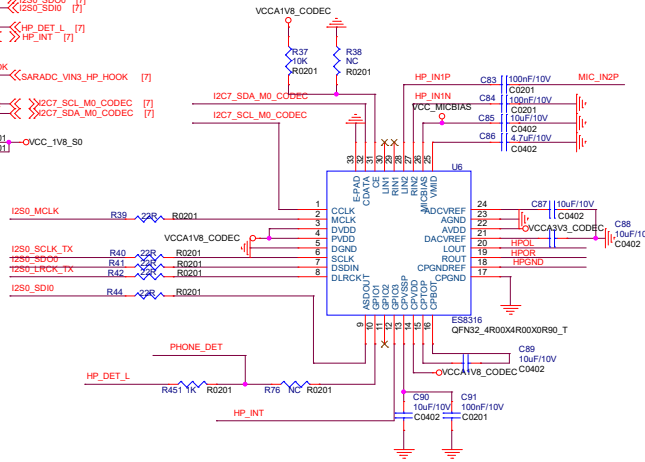


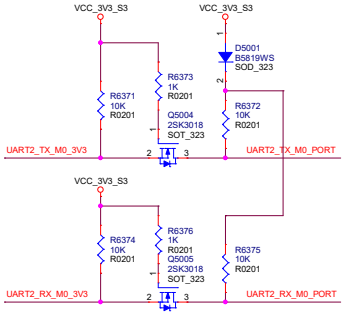




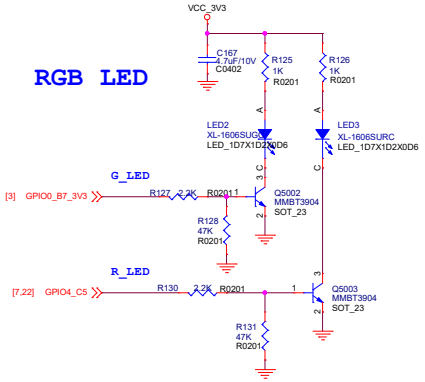


CODEC ES8316

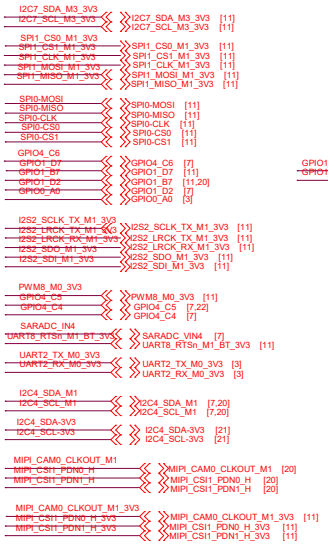


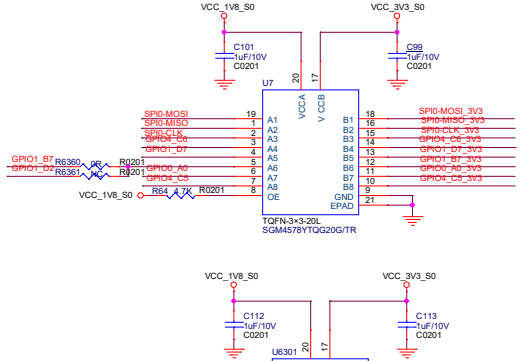


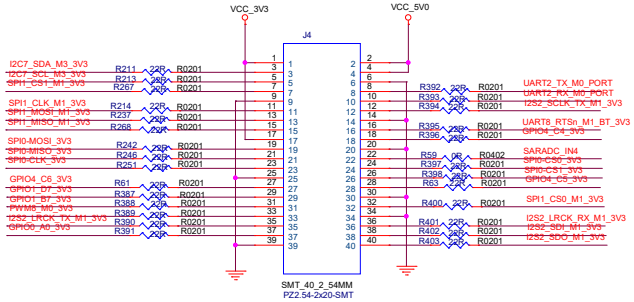
RGB LED

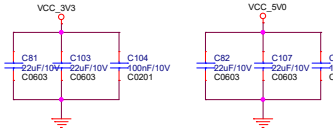


40PIN_GPIO



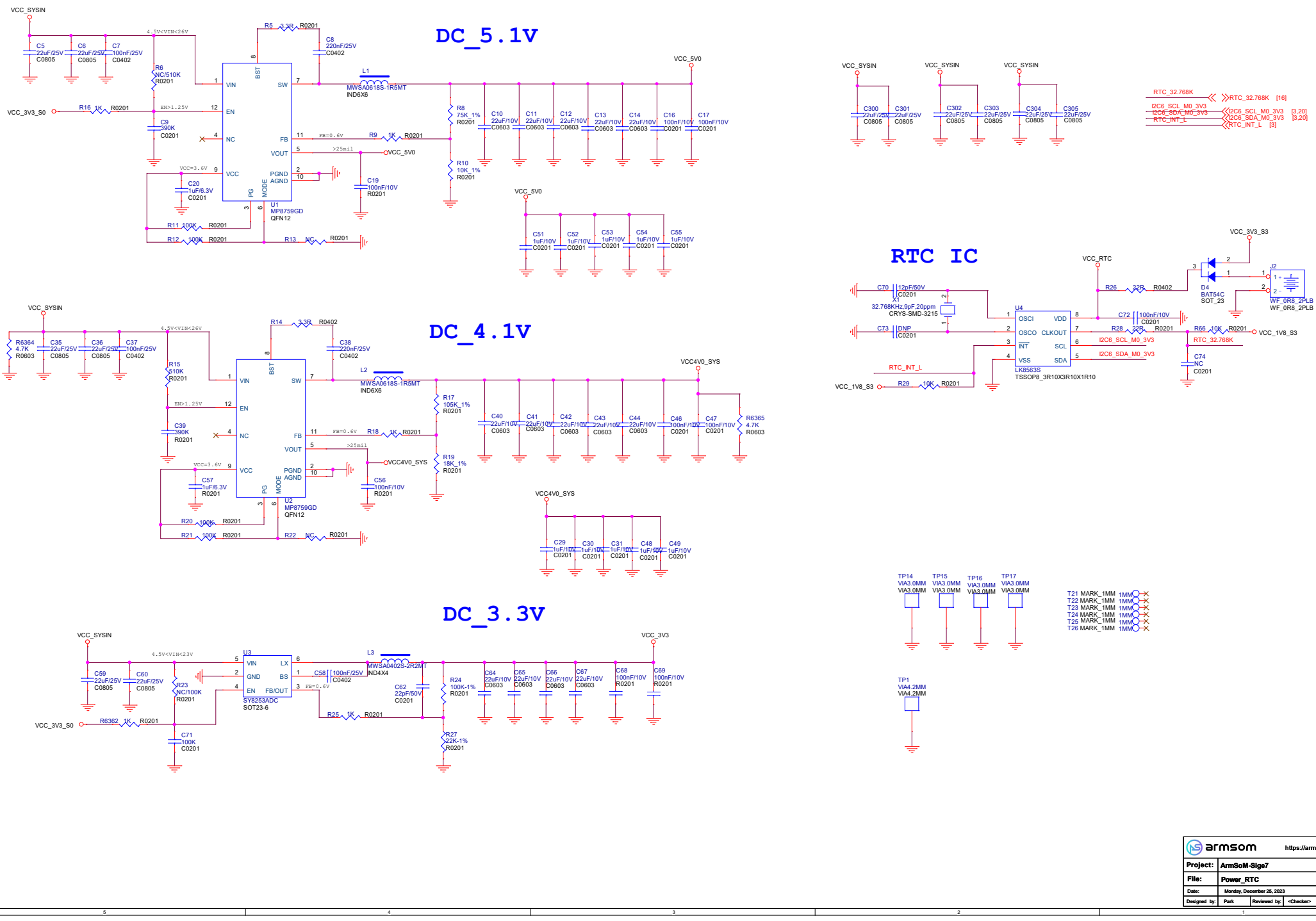






armsom https://armsom.org/

Project:	ArmSoM-Sige7
File:	Audio_GPIO
Date:	Monday, December 25, 2023
Rev:	V1.1
Designed by:	Park
Reviewed by:	<Checker>
Sheet:	22 of 24


DC_5.1V
VCC_SYSIN
4.5V<VIN<26V
C5 22uF/25V C0805
C6 22uF/25V C0805
C7 100nF/25V C0402
R5 3.3R R0201
C8 220nF/25V C0402
R6 NC/510K R0201
L1 MWSA0618S-1R5MT IND6X6
VCC_5V0
VCC_3V3_S0
R16 1K R0201
EN>1.25V
C9 390K C0201
BST
VIN
SW
EN
NC
FB
VOUT
PGND
AGND
PG
MODE
VCC
FB=0.6V
R9 1K R0201
>25mil
VCC=3.6V
C20 1uF/6.3V C0201
C19 100nF/10V R0201
U1 MP8759GD QFN12
R11 100K R0201
R12 100K R0201
R13 NC R0201
R8 75K_1% R0201
R10 10K_1% R0201
C10 22uF/10V C0603
C11 22uF/10V C0603
C12 22uF/10V C0603
C13 22uF/10V C0603
C14 22uF/10V C0603
C16 100nF/10V C0201
C17 100nF/10V C0201
C51 1uF/10V C0201
C52 1uF/10V C0201
C53 1uF/10V C0201
C54 1uF/10V C0201
C55 1uF/10V C0201
DC_4.1V
VCC_SYSIN
R6364 4.7K R0603
C35 22uF/25V C0805
C36 22uF/25V C0805
C37 100nF/25V C0402
4.5V<VIN<26V
R14 3.3R R0402
C38 220nF/25V C0402
R15 510K R0201
L2 MWSA0618S-1R5MT IND6X6
VCC4V0_SYS
EN>1.25V
C39 390K R0201
FB=0.6V
R18 1K R0201
>25mil
VCC=3.6V
C57 1uF/6.3V R0201
C56 100nF/10V R0201
U2 MP8759GD QFN12
R20 100K R0201
R21 100K R0201
R22 NC R0201
R17 105K_1% R0201
R19 18K_1% R0201
C40 22uF/10V C0603
C41 22uF/10V C0603
C42 22uF/10V C0603
C43 22uF/10V C0603
C44 22uF/10V C0603
C46 100nF/10V C0201
C47 100nF/10V C0201
R6365 4.7K R0603
C29 1uF/10V C0201
C30 1uF/10V C0201
C31 1uF/10V C0201
C48 1uF/10V C0201
C49 1uF/10V C0201
DC_3.3V
VCC_SYSIN
4.5V<VIN<23V
C59 22uF/25V C0805
C60 22uF/25V C0805
U3
VIN
LX
GND
BS
EN
FB/OUT
SY8253ADC SOT23-6
L3 MWSA0402S-2R2MT IND4X4
C58 100nF/25V C0402
FB=0.6V
R23 NC/100K R0201
R6362 1K R0201
VCC_3V3_S0
C71 100K C0201
C62 22pF/50V C0201
R25 1K R0201
R24 100K-1% R0201
R27 22K-1% R0201
C64 22uF/10V C0603
C65 22uF/10V C0603
C66 22uF/10V C0603
C67 22uF/10V C0603
C68 100nF/10V R0201
C69 100nF/10V R0201
VCC_3V3
C300 22uF/25V C0805
C301 22uF/25V C0805
C302 22uF/25V C0805
C303 22uF/25V C0805
C304 22uF/25V C0805
C305 22uF/25V C0805
RTC_32.768K
RTC_32.768K [16]
I2C6_SCL_M0_3V3
I2C6_SDA_M0_3V3
RTC_INT_L
I2C6_SCL_M0_3V3 [3,20]
I2C6_SDA_M0_3V3 [3,20]
RTC_INT_L [3]
RTC IC
VCC_3V3_S3
VCC_RTC
C70 12pF/50V C0201
X1 32.768KHz,9pF,20ppm CRYS-SMD-3215
C73 DNP C0201
U4
OSCI
VDD
OSCO
CLKOUT
INT
SCL
VSS
SDA
LK8563S TSSOP8_3R10X3R10X1R10
R26 22R R0402
D4 BAT54C SOT_23
J2
WF_0R8_2PLB
C72 100nF/10V C0201
R28 22R R0201
R66 10K R0201
VCC_1V8_S3
RTC_32.768K
C74 NC C0201
RTC_INT_L
VCC_1V8_S3
R29 10K R0201
I2C6_SCL_M0_3V3
I2C6_SDA_M0_3V3
TP14 VIA3.0MM VIA3.0MM
TP15 VIA3.0MM VIA3.0MM
TP16 VIA3.0MM VIA3.0MM
TP17 VIA3.0MM VIA3.0MM
T21 MARK_1MM 1MM
T22 MARK_1MM 1MM
T23 MARK_1MM 1MM
T24 MARK_1MM 1MM
T25 MARK_1MM 1MM
T26 MARK_1MM 1MM
TP1 VIA4.2MM VIA4.2MM
armsom
https://armsom.org/
Project: ArmSoM-Sige7
File: Power_RTC
Date: Monday, December 25, 2023
Rev: V1.1
Designed by: Park
Reviewed by: <Checker>
Sheet: 23 of 24

Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2023-08-07	SL Chen	First release;	
V1.0	2023-09-19	SL Chen	1.phone jack change to connector; change U23&U24 singal for layout,del poe cn1; 2.PWR: add C8964&C8965,R6364&R6365; 3.CAM: add R6366&R6367&R6368;	
V1.1	2023-12-13	SL Chen	1.VOL_IC: U27/U7/U6301change part pin; 2.USB: U15 from TypeC1 change to TypeC0; CN31 from USB3.0 change to USB2.0; 3.40PIN:add UART Protect; J2&CN2&CN32 change to WF0.8; 4.CAM: DEL R6352, CSI_1 I2C3 change to I2C4 5.WIFI Module: AP6275S change to AP6275P;	

armsom	https://armsom.org/				
Project:	ArmSoM-Sige7				
File:	Revision History				
Date:	Monday, December 25, 2023			Rev:	V1.1
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	24 of 24