Table of Content

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes
For more informations about the second source,please refer to our AVL.

Description ***Note*** ***Option***

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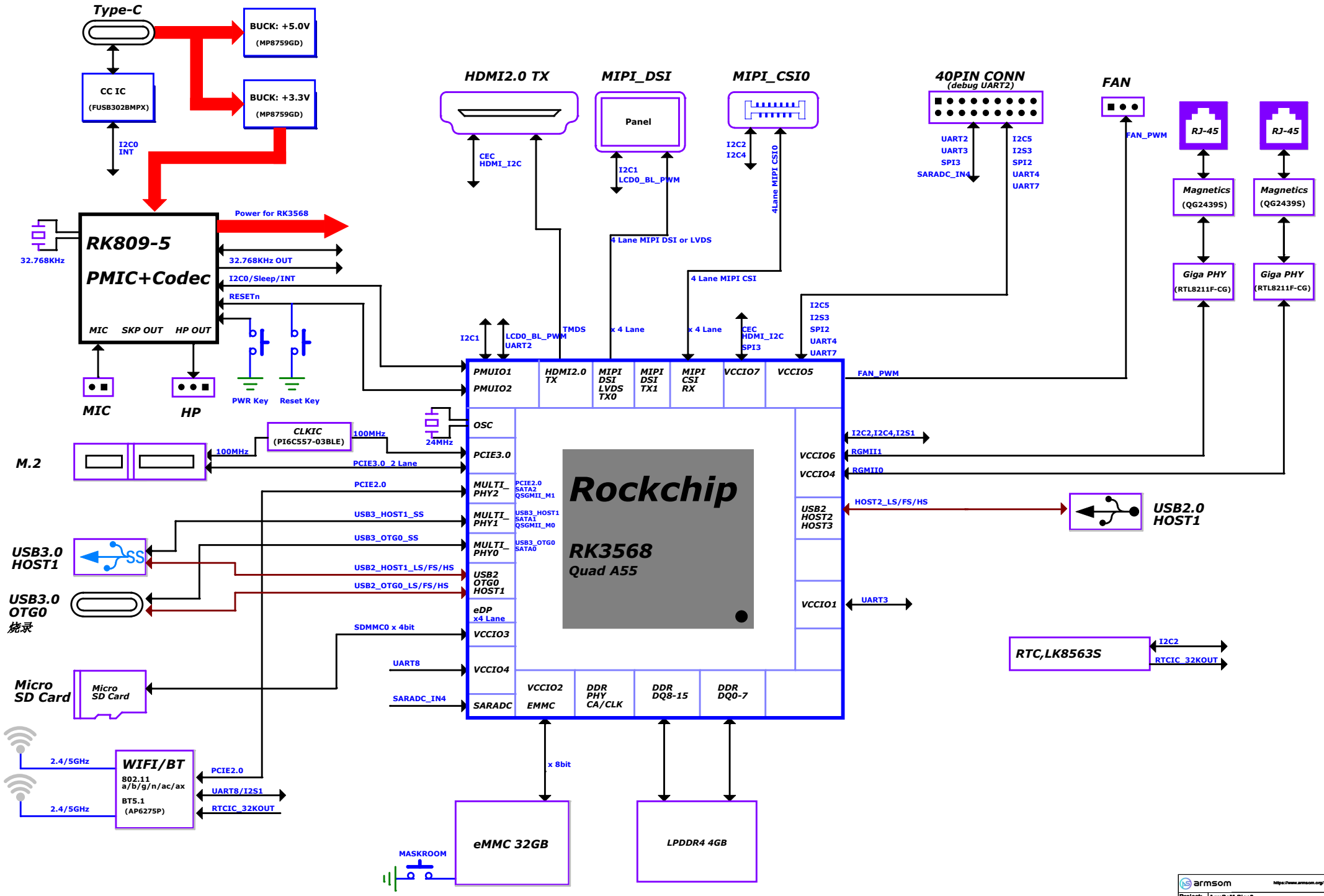
Project:	ArmSoM-Sige3				
File:	01.Index and Notes				
Date:	Tuesday, July 30, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	1 of 35

Revision History

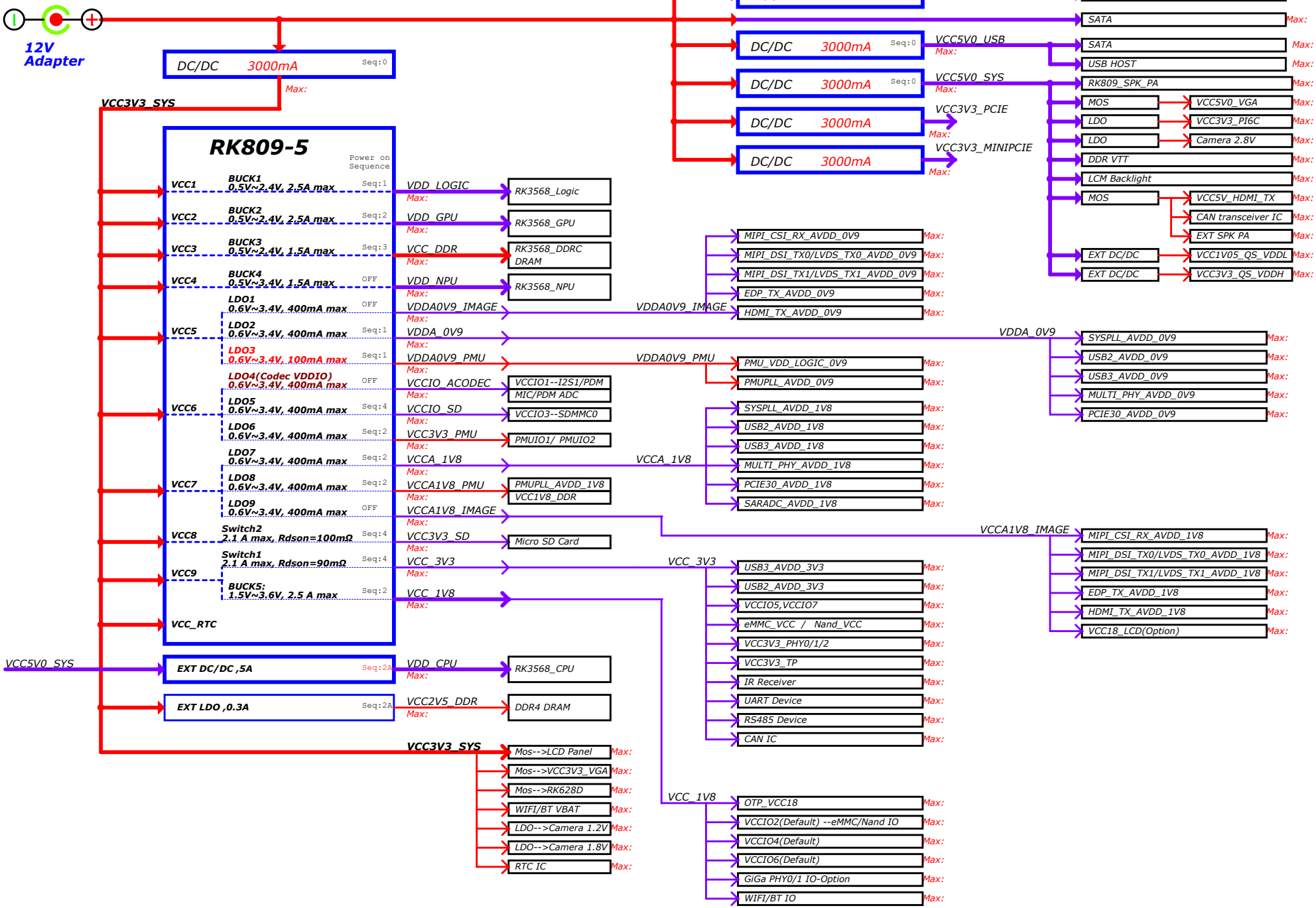
Version	Date	By	Change Dsecription	Approved
V1.0	2024-07-09	Liu Xinglin	1:Revision preliminary version	

armsom	https://www.armsom.org/				
Project:	ArmSoM-Sige3				
File:	02.Revision History				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	2 of 35

ArmSoM-Sige3 Block Diagram



Default Power Diagram



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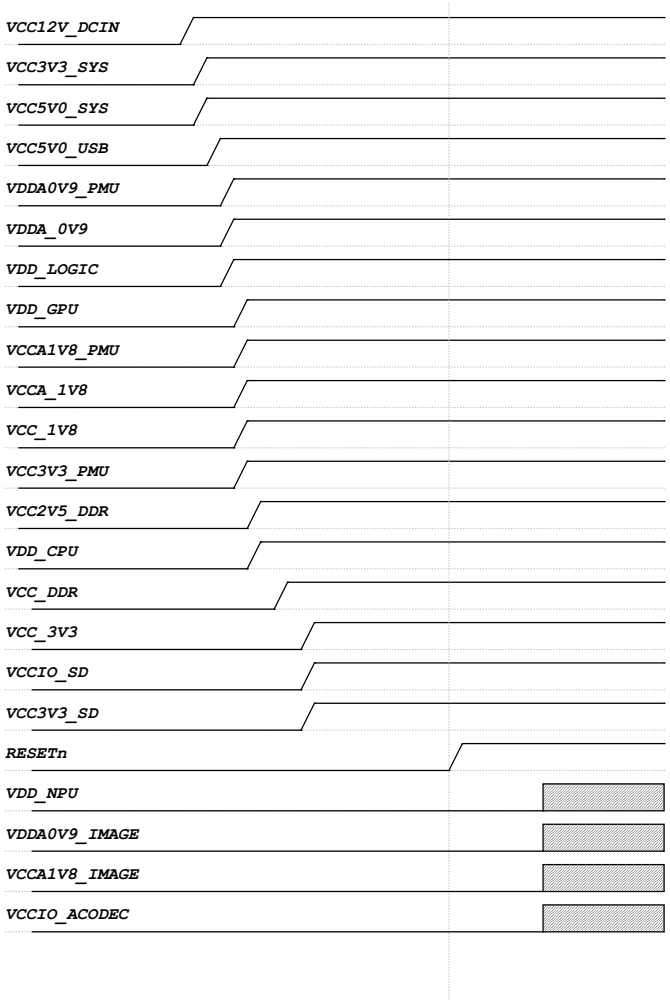
Project:	ArmSoM-Sige3				
File:	04.Power Diagram				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	4 of 35

Power Sequence



Power description

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC3V3_SYS	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	0.9V	TBD	TBD
VCC3V3_SYS	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	DVFS	TBD	TBD
VCC3V3_SYS	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	1.2V (DDR4)	TBD	TBD
VCC3V3_SYS	RK809_BUCK4	1.5A	VDD_NPU	N/A	0V	OFF	DVFS	TBD	TBD
VCC3V3_SYS	RK809_LDO1	0.4A	VDDA0V9_IMAGE	N/A	0V	OFF	0.9V	TBD	TBD
	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	0.9V	TBD	TBD
	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	0.9V	TBD	TBD
VCC3V3_SYS	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	0V	OFF	3.3V	TBD	TBD
	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	3.3V or 1.8V (SD2.0=3.3V,SD3.0=1.8V)	TBD	TBD
	RK809_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	3.3V	TBD	TBD
VCC3V3_SYS	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_LDO8	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_LDO9	0.4A	VCCA1V8_IMAGE	N/A	0V	OFF	1.8V	TBD	TBD
VCC3V3_SYS	RK809_SW2 100mohm	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	3.3V	TBD	TBD
VCC3V3_SYS	RK809_SW1 90mohm	2.1A	VCC_3V3	Slot:4	3.3V	ON	3.3V	TBD	TBD
	RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_RESETn			Slot:4+5					
VCC12V_DCIN	EXT BUCK	3.0A	VCC3V3_SYS	Slot:0	3.3V	ON	3.3V	TBD	TBD
VCC12V_DCIN	EXT BUCK	3.0A	VCC5V0_SYS	Slot:0	5.0V	ON	5.0V	TBD	TBD
VCC5V0_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.0V	ON	DVFS	TBD	TBD
VCC3V3_SYS	EXT LDO	0.3A	VCC2V5_DDR	Slot:2A	2.5V	ON	2.5V	TBD	TBD

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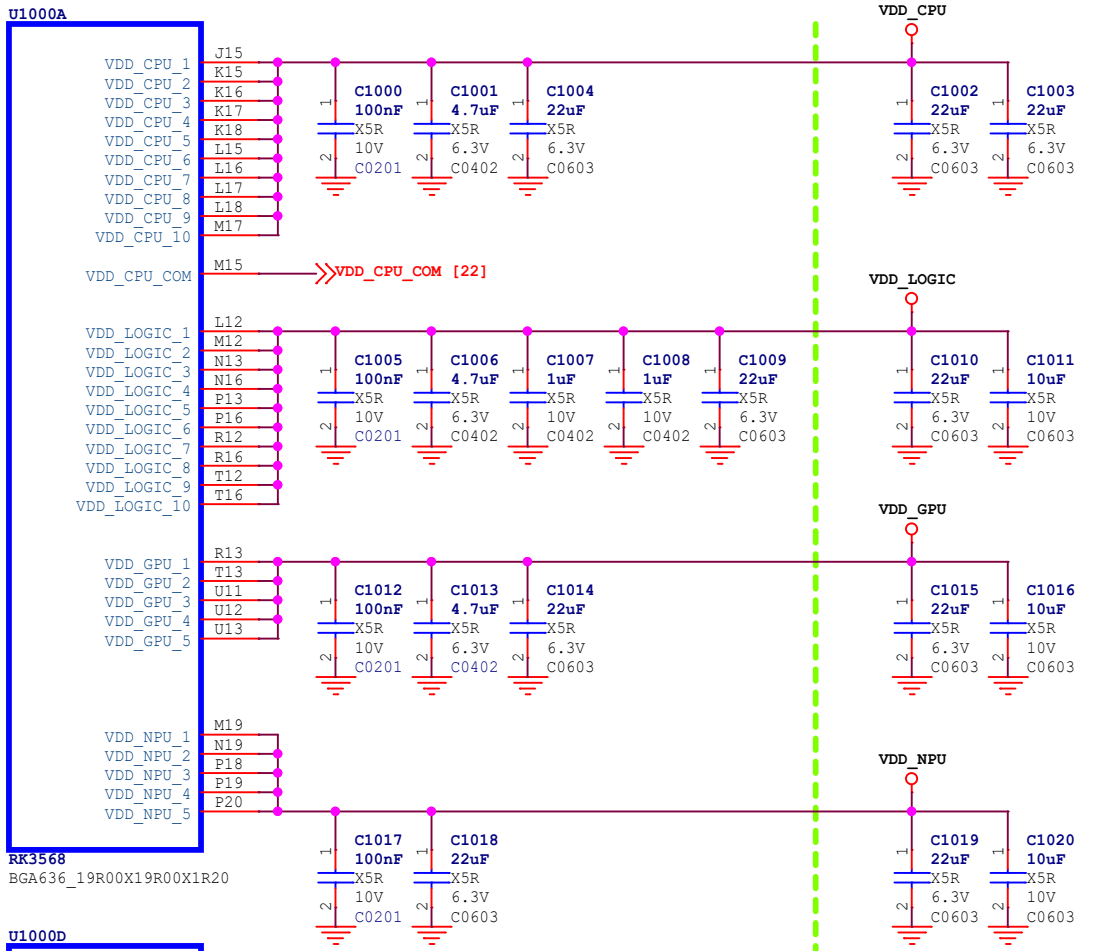
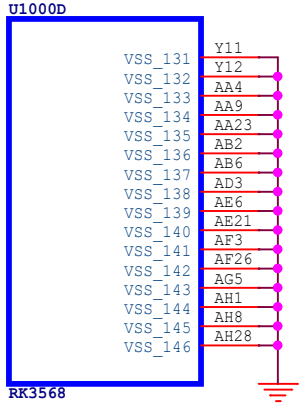
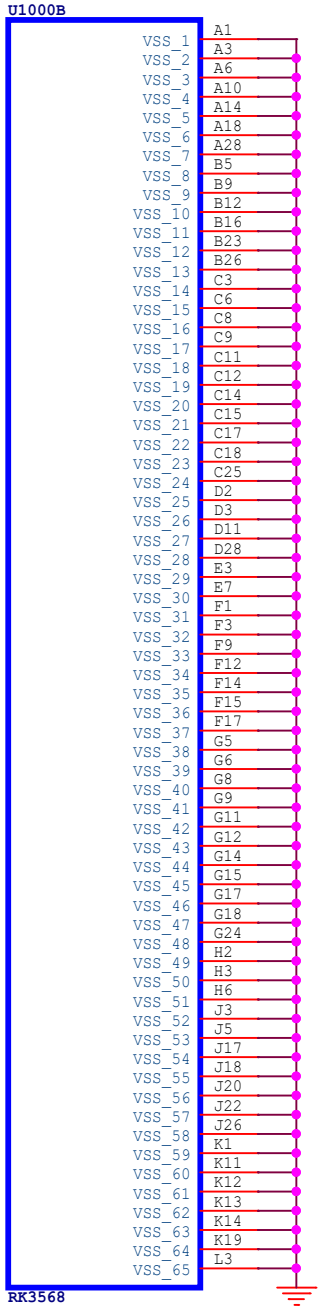
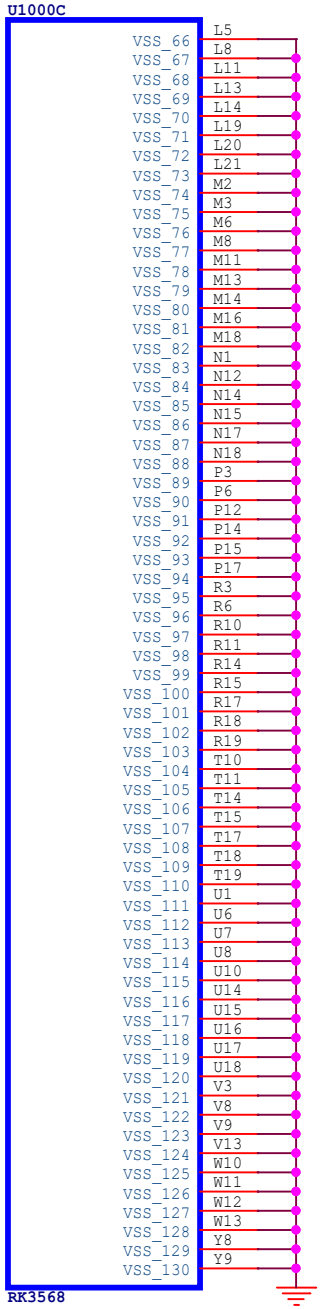
Project:	ArmSoM-Sige3				
File:	05.Power Sequence				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	5 of 35

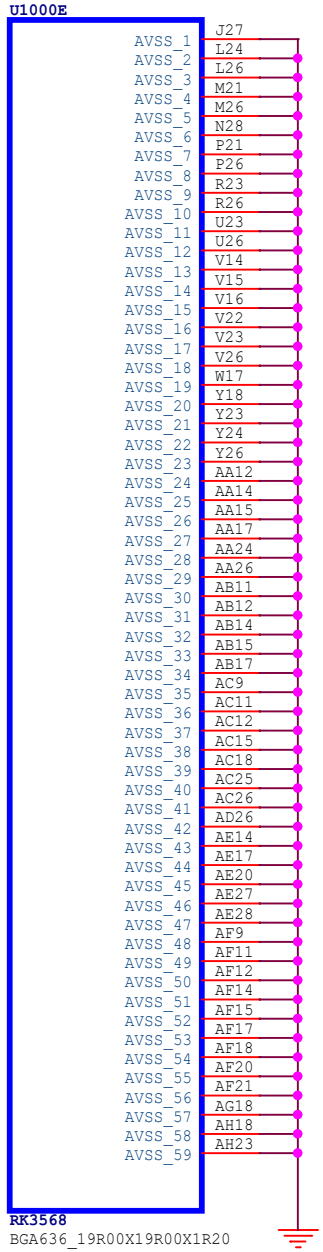
RK3568_ABCDE (Power&Gnd)











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Project:	ArmSoM-Sige3				
File:	06.RK3568_Power/GND				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	6 of 35

RK3568_F (DDR PHY)

U1000F

	DDR4	LPDDR4	DDR3	LPDDR3
F2	DDR_DQ0_A	DDR4_DQL0_A	LPDDR4_DQ0_A	DDR3_DQ0	LPDDR3_DQ15
E1	DDR_DQ1_A	DDR4_DQL2_A	LPDDR4_DQ1_A	DDR3_DQ1	LPDDR3_DQ14
E2	DDR_DQ2_A	DDR4_DQL4_A	LPDDR4_DQ2_A	DDR3_DQ2	LPDDR3_DQ10
D1	DDR_DQ3_A	DDR4_DQL6_A	LPDDR4_DQ3_A	DDR3_DQ3	LPDDR3_DQ9
J1	DDR_DQ4_A	DDR4_DQL7_A	LPDDR4_DQ4_A	DDR3_DQ4	LPDDR3_DQ13
J2	DDR_DQ5_A	DDR4_DQL5_A	LPDDR4_DQ5_A	DDR3_DQ5	LPDDR3_DQ12
H1	DDR_DQ6_A	DDR4_DQL3_A	LPDDR4_DQ6_A	DDR3_DQ6	LPDDR3_DQ8
H4	DDR_DQ7_A	DDR4_DQL1_A	LPDDR4_DQ7_A	DDR3_DQ7	LPDDR3_DQ11
H5	DDR_DM0_A	DDR4_DML_A	LPDDR4_DM0_A	DDR3_DM0	LPDDR3_DM1
G1	DDR_DQS0P_A	DDR4_DQSL_P_A	LPDDR4_DQS0P_A	DDR3_DQS0P	LPDDR3_DQS1P
G2	DDR_DQS0N_A	DDR4_DQSL_N_A	LPDDR4_DQS0N_A	DDR3_DQS0N	LPDDR3_DQS1N
M1	DDR_DQ8_A	DDR4_DQU3_A	LPDDR4_DQ8_A	DDR3_DQ8	LPDDR3_DQ25
N2	DDR_DQ9_A	DDR4_DQU1_A	LPDDR4_DQ9_A	DDR3_DQ9	LPDDR3_DQ24
L7	DDR_DQ10_A	DDR4_DQU7_A	LPDDR4_DQ10_A	DDR3_DQ10	LPDDR3_DQ28
L6	DDR_DQ11_A	DDR4_DQU5_A	LPDDR4_DQ11_A	DDR3_DQ11	LPDDR3_DQ29
K2	DDR_DQ12_A	DDR4_DQU2_A	LPDDR4_DQ12_A	DDR3_DQ12	LPDDR3_DQ26
J6	DDR_DQ13_A	DDR4_DQU4_A	LPDDR4_DQ13_A	DDR3_DQ13	LPDDR3_DQ31
J7	DDR_DQ14_A	DDR4_DQU6_A	LPDDR4_DQ14_A	DDR3_DQ14	LPDDR3_DQ30
L4	DDR_DQ15_A	DDR4_DQU0_A	LPDDR4_DQ15_A	DDR3_DQ15	LPDDR3_DQ27
J4	DDR_DM1_A	DDR4_DMU_A	LPDDR4_DM1_A	DDR3_DM1	LPDDR3_DM3
L2	DDR_DQS1P_A	DDR4_DQSU_P_A	LPDDR4_DQS1P_A	DDR3_DQS1P	LPDDR3_DQS3P
L1	DDR_DQS1N_A	DDR4_DQSU_N_A	LPDDR4_DQS1N_A	DDR3_DQS1N	LPDDR3_DQS3N
B10	DDR_DQ0_B	DDR4_DQU7_B	LPDDR4_DQ0_B	DDR3_DQ16	LPDDR3_DQ1
A9	DDR_DQ1_B	DDR4_DQU5_B	LPDDR4_DQ1_B	DDR3_DQ17	LPDDR3_DQ5
D12	DDR_DQ2_B	DDR4_DQU3_B	LPDDR4_DQ2_B	DDR3_DQ18	LPDDR3_DQ6
E12	DDR_DQ3_B	DDR4_DQU1_B	LPDDR4_DQ3_B	DDR3_DQ19	LPDDR3_DQ4
A12	DDR_DQ4_B	DDR4_DQU0_B	LPDDR4_DQ4_B	DDR3_DQ20	LPDDR3_DQ2
D15	DDR_DQ5_B	DDR4_DQU6_B	LPDDR4_DQ5_B	DDR3_DQ21	LPDDR3_DQ3
E15	DDR_DQ6_B	DDR4_DQU4_B	LPDDR4_DQ6_B	DDR3_DQ22	LPDDR3_DQ7
E14	DDR_DQ7_B	DDR4_DQU2_B	LPDDR4_DQ7_B	DDR3_DQ23	LPDDR3_DQ0
D14	DDR_DM0_B	DDR4_DMU_B	LPDDR4_DM0_B	DDR3_DM2	LPDDR3_DM0
A11	DDR_DQS0P_B	DDR4_DQSU_P_B	LPDDR4_DQS0P_B	DDR3_DQS2P	LPDDR3_DQS0P
B11	DDR_DQS0N_B	DDR4_DQSU_N_B	LPDDR4_DQS0N_B	DDR3_DQS2N	LPDDR3_DQS0N
A16	DDR_DQ8_B	DDR4_DQL0_B	LPDDR4_DQ8_B	DDR3_DQ24	LPDDR3_DQ18
B17	DDR_DQ9_B	DDR4_DQL2_B	LPDDR4_DQ9_B	DDR3_DQ25	LPDDR3_DQ19
A17	DDR_DQ10_B	DDR4_DQL4_B	LPDDR4_DQ10_B	DDR3_DQ26	LPDDR3_DQ22
B18	DDR_DQ11_B	DDR4_DQL6_B	LPDDR4_DQ11_B	DDR3_DQ27	LPDDR3_DQ23
B13	DDR_DQ12_B	DDR4_DQL7_B	LPDDR4_DQ12_B	DDR3_DQ28	LPDDR3_DQ16
A13	DDR_DQ13_B	DDR4_DQL5_B	LPDDR4_DQ13_B	DDR3_DQ29	LPDDR3_DQ17
D17	DDR_DQ14_B	DDR4_DQL1_B	LPDDR4_DQ14_B	DDR3_DQ30	LPDDR3_DQ20
B14	DDR_DQ15_B	DDR4_DQL3_B	LPDDR4_DQ15_B	DDR3_DQ31	LPDDR3_DQ21
E17	DDR_DM1_B	DDR4_DML_B	LPDDR4_DM1_B	DDR3_DM3	LPDDR3_DM2
B15	DDR_DQS1P_B	DDR4_DQSL_P_B	LPDDR4_DQS1P_B	DDR3_DQS3P	LPDDR3_DQS2P
A15	DDR_DQS1N_B	DDR4_DQSL_N_B	LPDDR4_DQS1N_B	DDR3_DQS3N	LPDDR3_DQS2N
P5	DDR_ECC_DQ0	DDR4_ECC_DQ7	--	DDR3_ECC_DQ0	
M4	DDR_ECC_DQ1	DDR4_ECC_DQ0	--	DDR3_ECC_DQ1	
M5	DDR_ECC_DQ2	DDR4_ECC_DQ2	--	DDR3_ECC_DQ2	
R5	DDR_ECC_DQ3	DDR4_ECC_DQ1	--	DDR3_ECC_DQ3	
M7	DDR_ECC_DQ4	DDR4_ECC_DQ6	--	DDR3_ECC_DQ4	
R7	DDR_ECC_DQ5	DDR4_ECC_DQ4	--	DDR3_ECC_DQ5	
P4	DDR_ECC_DQ6	DDR4_ECC_DQ3	--	DDR3_ECC_DQ6	
R4	DDR_ECC_DQ7	DDR4_ECC_DQ5	--	DDR3_ECC_DQ7	
P7	DDR_ECC_DM	DDR4_ECC_DM	--	DDR3_ECC_DM	
P2	DDR_ECC_DQS_P	DDR4_ECC_DQS_P	--	DDR3_ECC_DQS_P	
P1	DDR_ECC_DQS_N	DDR4_ECC_DQS_N	--	DDR3_ECC_DQS_N	

	DDR4	LPDDR4	DDR3	LPDDR3
B6	DDR4_A0	LPDDR4_CLKP_B	DDR3_A9	---	AC0
F5	DDR4_A1	---	DDR3_A2	---	AC1
B1	DDR4_A2	LPDDR4_A1_A	DDR3_A4	LPDDR3_A6	AC2
F4	DDR4_A3	LPDDR4_CKE1_A	DDR3_A3	---	AC3
D9	DDR4_A4	LPDDR4_A3_B	DDR3_BA1	LPDDR3_A3	AC4
B7	DDR4_A5	LPDDR4_A5_B	DDR3_A11	LPDDR3_A2	AC5
A7	DDR4_A6	LPDDR4_A1_B	DDR3_A13	LPDDR3_A1	AC6
A8	DDR4_A7	LPDDR4_ODT0_CA_B	DDR3_A8	---	AC7
C1	DDR4_A8	LPDDR4_ODT0_CA_A	DDR3_A6	LPDDR3_A9	AC8
A5	DDR4_A9	LPDDR4_CLKN_B	DDR3_A5	---	AC9
D6	DDR4_A10	LPDDR4_CKE0_B	DDR3_A10	---	AC10
C2	DDR4_A11	LPDDR4_A0_A	DDR3_A7	LPDDR3_A8	AC11
C4	DDR4_A12	LPDDR4_A3_A	DDR3_BA2	---	AC12
B8	DDR4_A13	LPDDR4_A0_B	DDR3_A14	LPDDR3_A0	AC13
C5	DDR4_A14_WEn	LPDDR4_A4_A	DDR3_A15	LPDDR3_A5	AC14
E4	DDR4_A15_CASn	LPDDR4_A2_A	DDR3_A0	---	AC15
D5	DDR4_A16_RASn	LPDDR4_A5_A	DDR3_RASn	LPDDR3_A7	AC16
E6	DDR4_ACTn	LPDDR4_CKE1_B	DDR3_CASn	---	AC17
E11	DDR4_BA0	LPDDR4_A2_B	DDR3_A1	---	AC18
E9	DDR4_BA1	LPDDR4_A4_B	DDR3_A12	LPDDR3_A4	AC19
F8	DDR4_BG0	LPDDR4_ODT1_CA_B	DDR3_WEn	---	AC20
F7	DDR4_BG1	LPDDR4_ODT1_CA_A	DDR3_BA0	---	AC21
B3	DDR4_CKE	LPDDR4_CKE0_A	DDR3_CKE	LPDDR3_CKE	AC22
B4	DDR4_CLKP	LPDDR4_CLKP_A	DDR3_CLKP	LPDDR3_CLKP	AC23
A4	DDR4_CLKN	LPDDR4_CLKN_A	DDR3_CLKN	LPDDR3_CLKN	AC24
A2	DDR4_CS0n	LPDDR4_CS0n_A	DDR3_ODT1	LPDDR3_ODT0	AC25
B2	DDR4_CS1n	LPDDR4_CS1n_A	DDR3_CS1n	LPDDR3_ODT1	AC26
E8	DDR4_ODT0	LPDDR4_CS1n_B	DDR3_ODT0	LPDDR3_CS1n	AC27
D8	DDR4_ODT1	LPDDR4_CS0n_B	DDR3_CS0n	LPDDR3_CS0n	AC28
F11	DDR4_RESETn	LPDDR4_RESETn	DDR3_RESETn	---	AC29

Note: Sequences can not be swap

Note:
Except DDR3, other DQ sequences can not be swap

	DDR4	LPDDR4	DDR3	LPDDR3
H7	DDR_RZQ			
P8	DDR_VREFOUT			
J8	DDR_AVSS			

DDR3L	=1.35V
DDR3	=1.5V
DDR4	=1.2V
LPDDR3	=1.2V
LPDDR4	=1.1V
LPDDR4x	=1.1V

H9	DDRPHY_VDDQ_1
H11	DDRPHY_VDDQ_2
H12	DDRPHY_VDDQ_3
H14	DDRPHY_VDDQ_4
H15	DDRPHY_VDDQ_5
J9	DDRPHY_VDDQ_6
L9	DDRPHY_VDDQ_7
M9	DDRPHY_VDDQ_8

DDR3L	=1.35V
DDR3	=1.5V
DDR4	=1.2V
LPDDR3	=1.2V
LPDDR4	=1.1V
LPDDR4x	=0.6V

J11	DDRPHY_VDDQL_1
J12	DDRPHY_VDDQL_2
J14	DDRPHY_VDDQL_3
K10	DDRPHY_VDDQL_4
L10	DDRPHY_VDDQL_5
M10	DDRPHY_VDDQL_6

R1101
120R
R0402
5%

For DDR4/DDR3/LPDDR3 mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RZQ pin and VSS pin

For LPDDR4/LPDDR4x mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RZQ pin and DDRPHY_VDDQ pin

LPDDR4/LPDDR4x

VCC_DDR

C1100	C1101	C1102	C1103	C1104
100nF	100nF	4.7uF	4.7uF	10uF
X5R	X5R	X5R	X5R	X5R
10V	10V	6.3V	6.3V	10V
C0201	C0201	C0402	C0402	C0603

VCC0V6_DDR

C1105	C1106	C1107	C1108	C1109
100nF	100nF	4.7uF	4.7uF	4.7uF
X5R	X5R	X5R	X5R	X5R
10V	10V	6.3V	6.3V	6.3V
C0201	C0201	C0402	C0402	C0402

Caps should be placed under the U1000 package

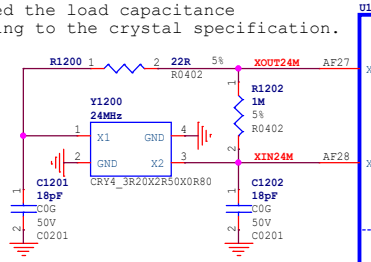
RK3568
BGA636_19R00X19R00X1R20

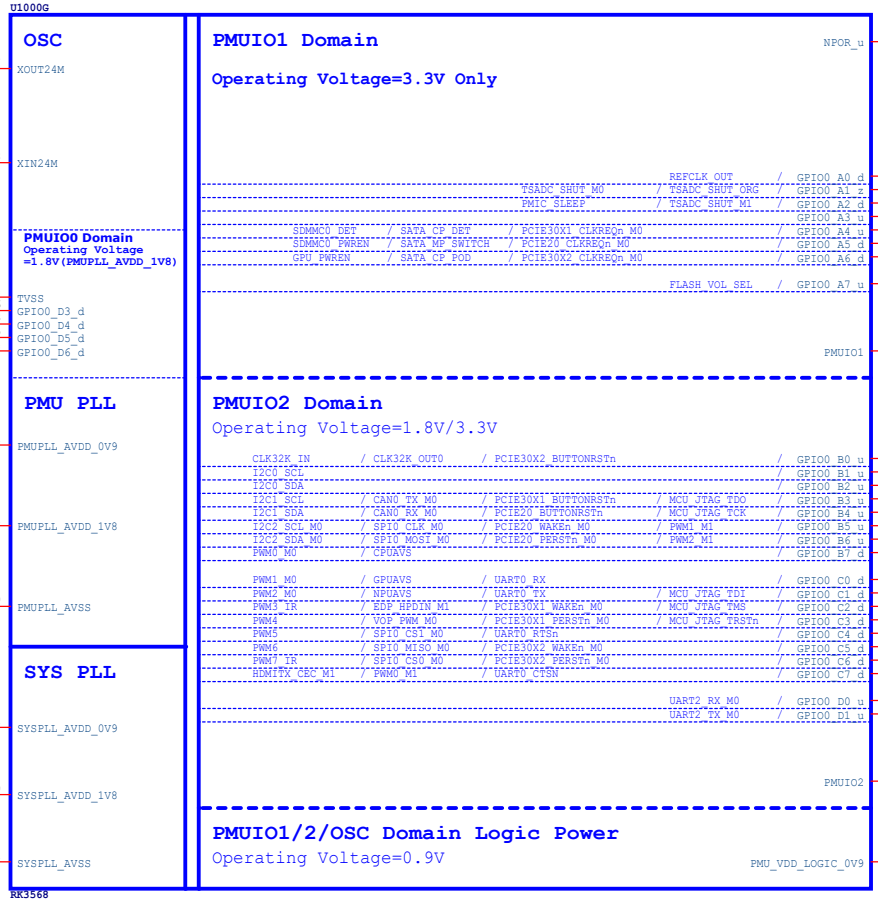
armsom https://www.armsom.org/

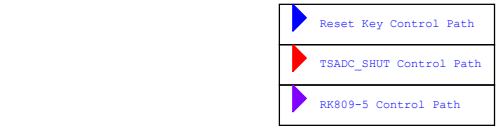
Project:	ArmSoM-Sige3		
File:	07.RK3568_DDR PHY		
Date:	Tuesday, July 09, 2024	Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by: <Checker>	Sheet: 7 of 35

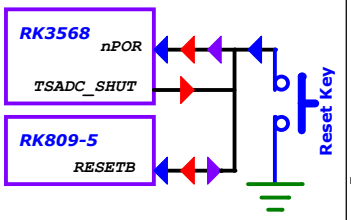
RK3568_G(OSC/PLL/PMUIO1/2)

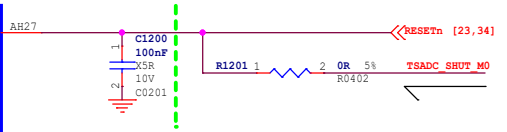
Note:
Adjusted the load capacitance according to the crystal specification.



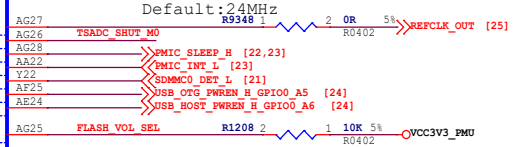


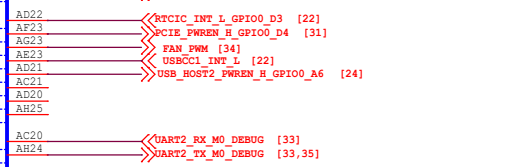


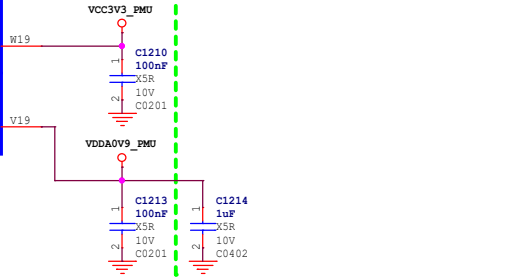


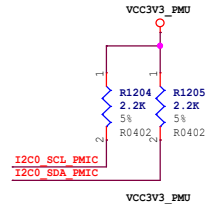


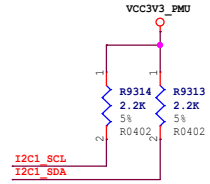
Default:24MHz

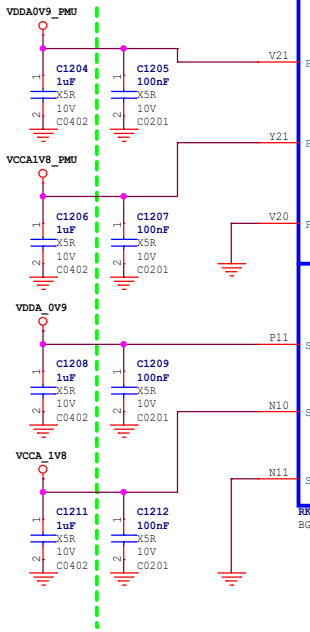








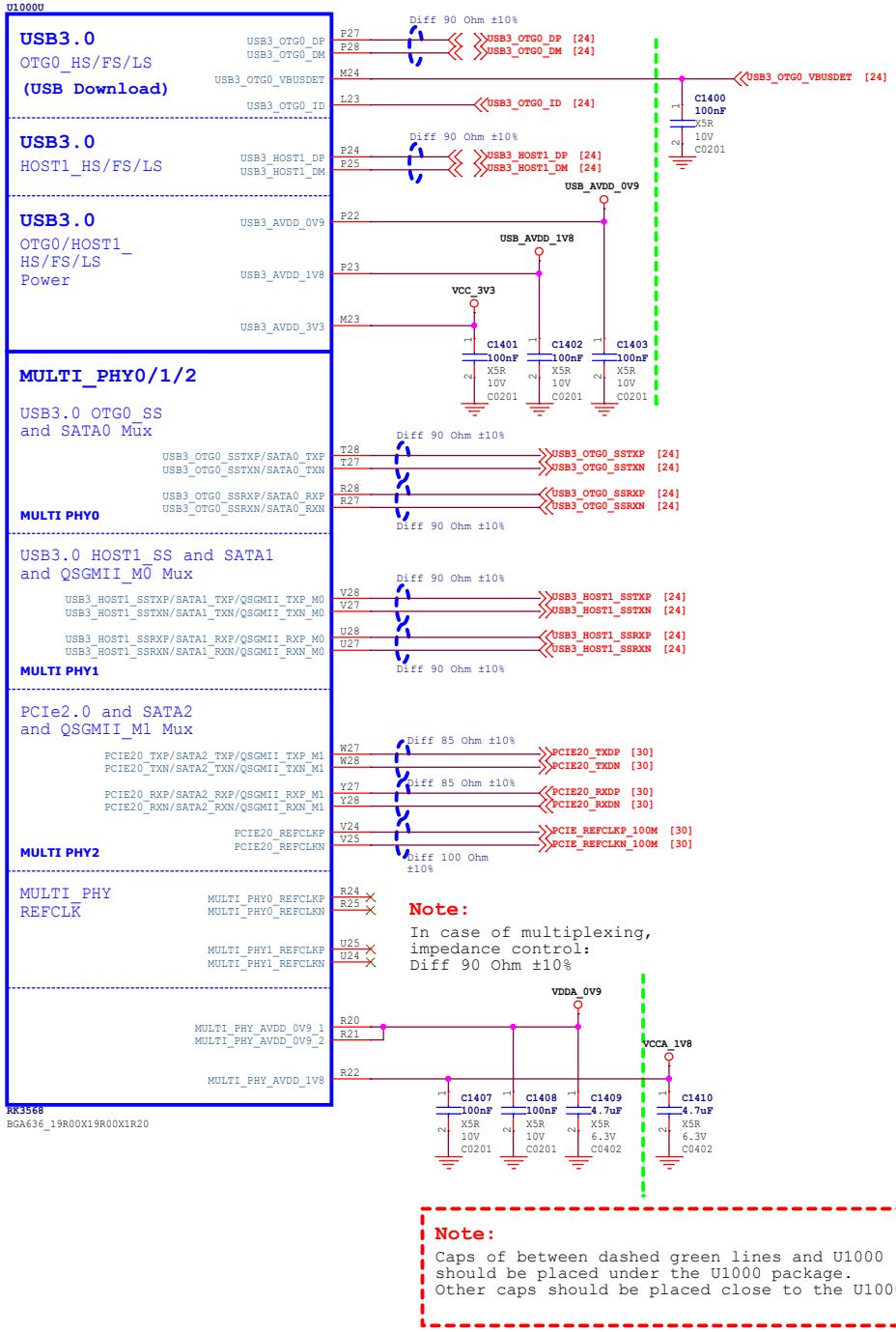




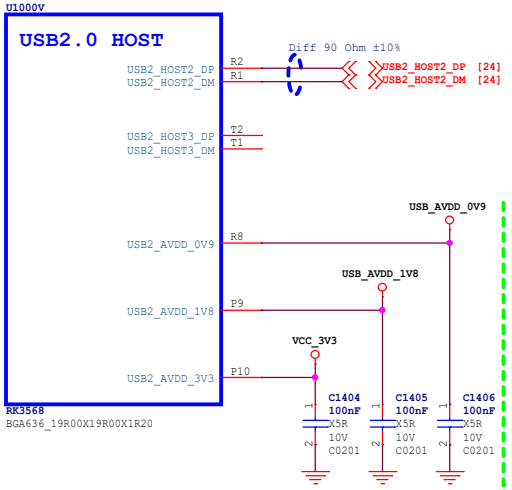
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

armsom	https://www.armsom.org/				
Project:	ArmSoM-Sige3				
File:	08.RK3568_OSC/PLL/PMUIO				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	8 of 35

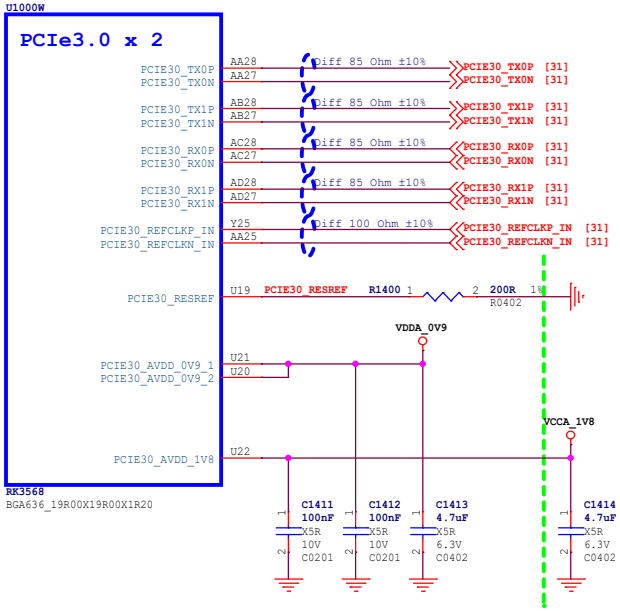
RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)



RK3568_V(USB2.0 HOST)

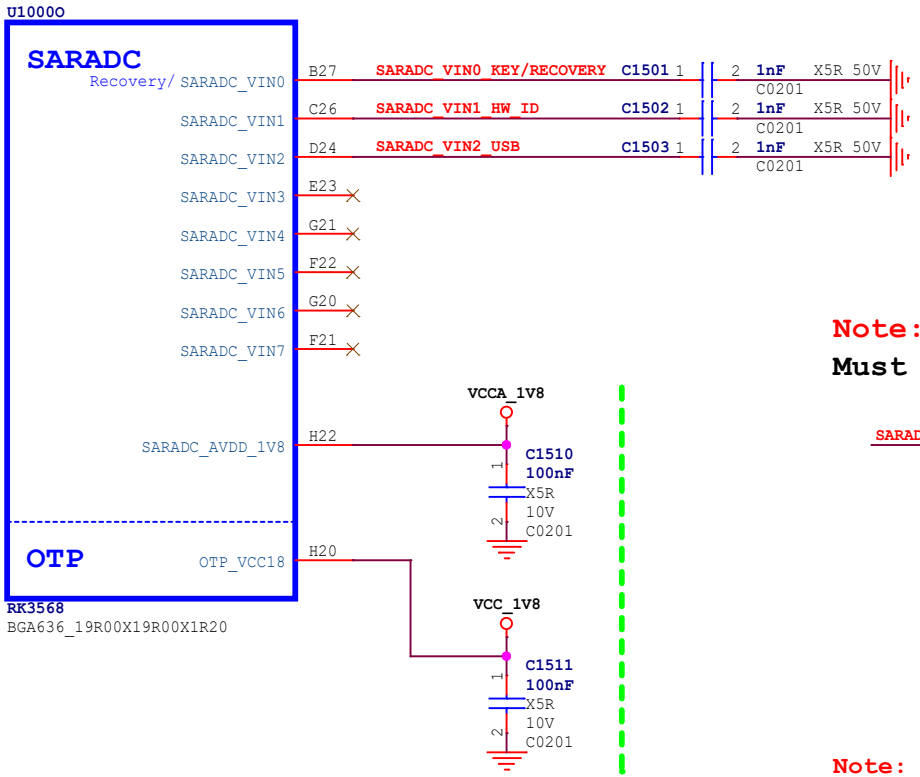


RK3568_W(PCIe3.0 x2)



armsom	https://www.armsom.org/				
Project:	ArmSoM-Sige3				
File:	09.RK3568_USB/PCIe/SATA PHY				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	9 of 35

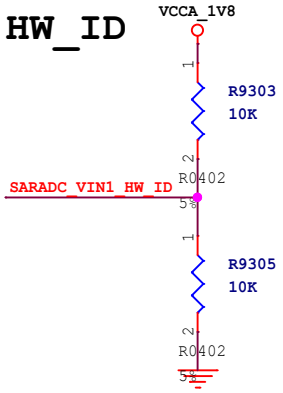
RK3568_O(SARADC/OTP)



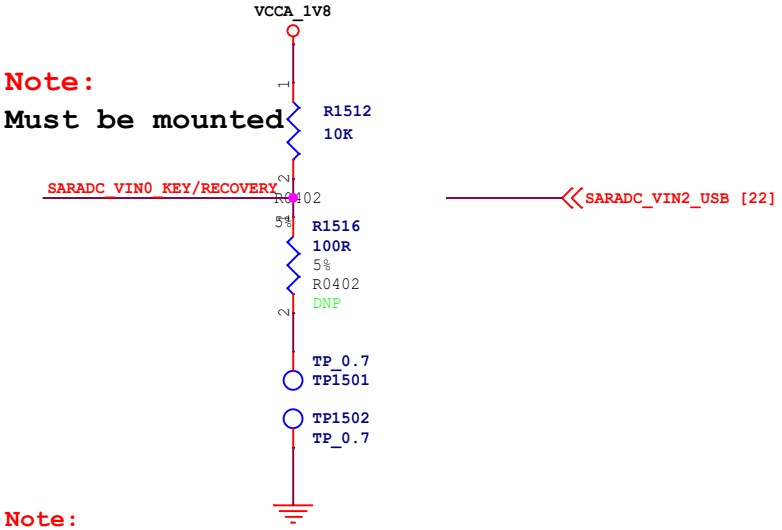
Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

HW_ID



SARADC_VIN1	Up Resistance	Down Resistance
HW_ID0	10K	DNP
HW_ID1	10K	110K
HW_ID2	20K	100K
HW_ID3	33K	100K
HW_ID4	18K	36K
HW_ID5	36K	51K
HW_ID6	51K	51K
HW_ID7	51K	36K
HW_ID8	36K	18K
HW_ID9	100K	33K
HW_ID10	100K	20K
HW_ID11	110K	10K
HW_ID12	DNP	10K



Note:

Must be mounted

Note:

If there is no Key requirement, two test points must be reserved to facilitate firmware update

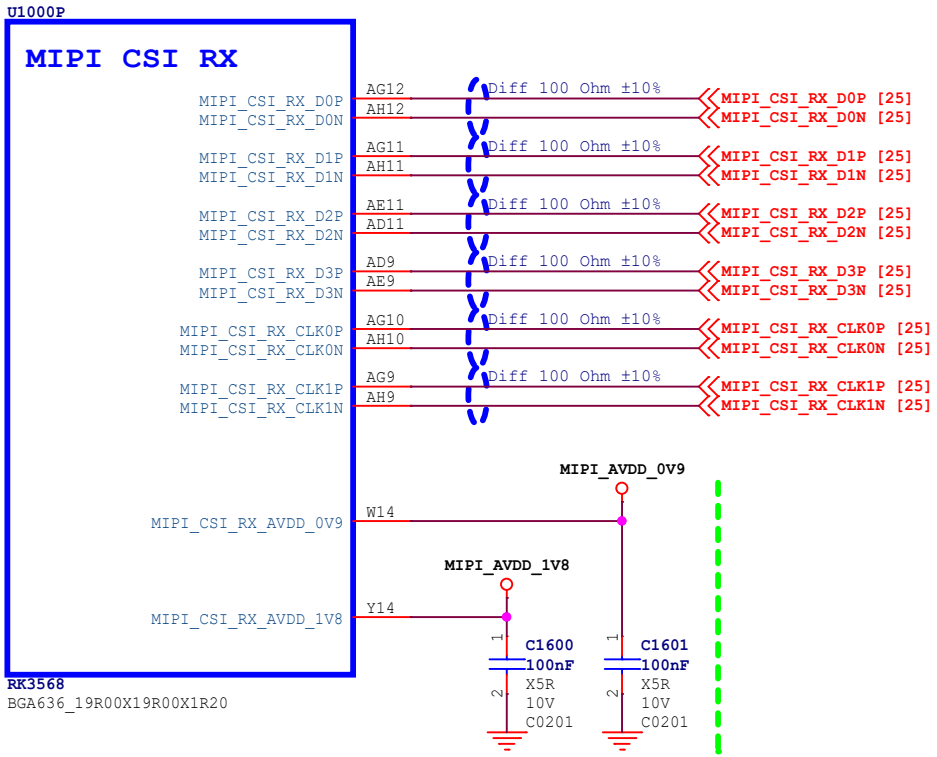
It is suggested to reserve a Key to facilitate the development debug

If SARADC_VIN0=0V at after power on and reset, then system will enter into loader mode.

armsom https://www.armsom.org/

Project:	ArmSoM-Sige3				
File:	10.RK3568_SARADC				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	10 of 35

RK3568_P(MIPI_CSI_RX)

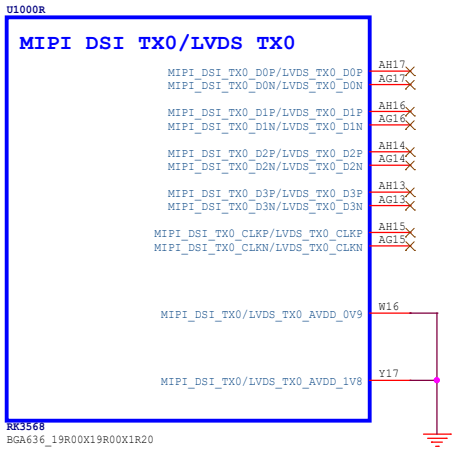


Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* *+* *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0* *MIPI_CSI_RX_D2-3* *MIPI_CSI_RX_CLK1*

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

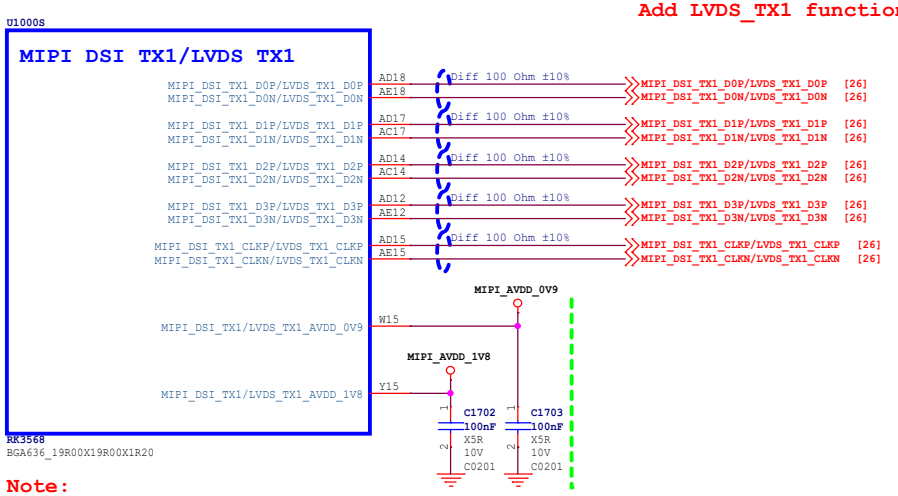
armsom	https://www.armsom.org/				
Project:	ArmSoM-Sige3				
File:	11.RK3568_VI Interface				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	11 of 35

RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



RK3568_S(MIPI_DSI_TX1/LVDS_TX1)

Note:
Add LVDS_TX1 function

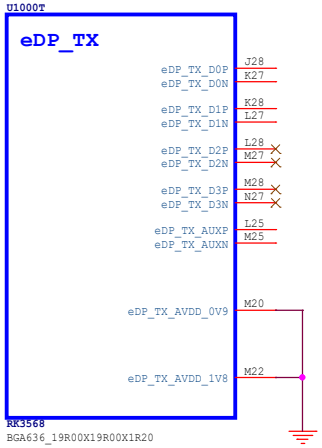


Note:

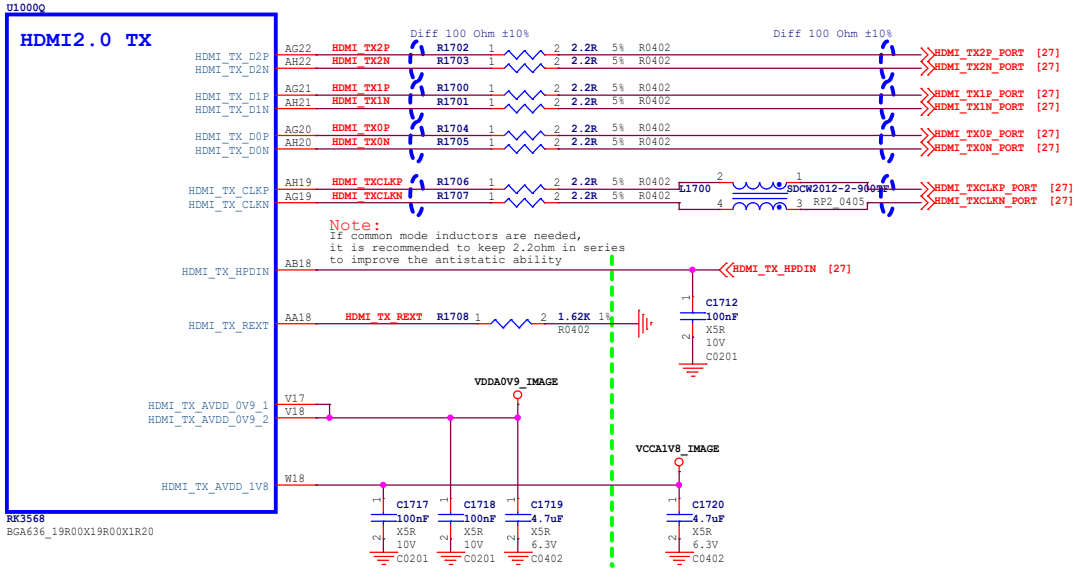
MIPI_DSI_TX0 + MIPI_DSI_TX1 support dual MIPI DSI TX interface,
Left and Right support redistribution.

LVDS_TX0 + LVDS_TX1 support dual LVDS TX interface,
Left and Right support redistribution

RK3568_T(eDP TX)



RK3568_Q(HDMI2.0 TX)



Note:

Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

armsom https://www.armsom.org/

Project:	ArmSoM-Sige3				
File:	12.RK3568_VO Interface				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	12 of 35

RK3568_H(VCCIO1 Domain)

U1000H

VCCIO1 Domain

Operating Voltage=1.8V/3.3V

I2C3_SDA_M0	/ UART3_RX_M0	/ CAN1_RX_M0		/ AUDIOPWM_LOUT_P	/ ACODEC_ADC_DATA	/ GPIO1_A0_u
I2C3_SCL_M0	/ UART3_TX_M0	/ CAN1_TX_M0		/ AUDIOPWM_LOUT_N	/ ACODEC_ADC_CLK	/ GPIO1_A1_u
I2S1_MCLK_M0	/ UART3_RTSn_M0	/ SCR_CLK	/ PCIE30X1_PERSTn_M2			/ GPIO1_A2_d
I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ SCR_IO	/ PCIE30X1_WAKEn_M2		/ ACODEC_DAC_CLK	/ GPIO1_A3_d
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0		/ SPDIF_TX_M0		/ GPIO1_A4_d
I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ SCR_RST	/ PCIE30X1_CLKREQn_M2		/ ACODEC_DAC_SYNC	/ GPIO1_A5_d
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0		/ AUDIOPWM_ROUT_P		/ GPIO1_A6_d
I2S1_SDO0_M0	/ UART4_CTSn_M0	/ SCR_DET		/ AUDIOPWM_ROUT_N	/ ACODEC_DAC_DATAL	/ GPIO1_A7_d
I2S1_SDO1_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0	/ PCIE20_CLKREQn_M2		/ ACODEC_DAC_DATAR	/ GPIO1_B0_d
I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_WAKEn_M2		/ ACODEC_ADC_SYNC	/ GPIO1_B1_d
I2S1_SDO3_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_PERSTn_M2			/ GPIO1_B2_d
	I2S1_SDI0_M0	/ PDM_SDI0_M0				/ GPIO1_B3_d

VCCIO1

RK3568

BGA636_19R00X19R00X1R20

D18
E18
A19 — I2S1_MCLK_M0_SOC — R1902 1 2 22R 5% R0402 — I2S1_MCLK_M0_RK809 [23]
B19 — I2S1_SCLK_TX_M0_SOC — R1903 1 2 22R 5% R0402 — I2S1_SCLK_TX_M0_RK809 [23]
F18
A20 — I2S1_LRCK_TX_M0_SOC — R1905 1 2 22R 5% R0402 — I2S1_LRCK_TX_M0_RK809 [23]
C20 — PDM_CLK0_M0_SOC — R1906 1 2 22R 5% R0402 — PDM_CLK0_M0_RK809 [23]
B20 — I2S1_SDO0_M0_RK809 [23]
D20
E20 — HP_DET_L_GPIO3_C2 [32]
A21
B21 — I2S1_SDI0_M0/PDM_SDI0_M0_RK809 [23]

VCCIO_ACODEC

Default 3.3V

H17 — C1900 100nF X5R 10V C0201

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

armsom	https://www.armsom.org/				
Project:	ArmSoM-Sige3				
File:	13.RK3568_Audio				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	13 of 35

RK3568_I(VCCIO2 Domain)

U1000I

VCCIO2 Domain

Operating Voltage=1.8V/3.3V

EMMC_D0	/ FLASH_D0	/ GPIO1_B4_u	A24	eMMC_D0/FLASH_D0 [20,34]
EMMC_D1	/ FLASH_D1	/ GPIO1_B5_u	C21	eMMC_D1/FLASH_D1 [20]
EMMC_D2	/ FLASH_D2	/ GPIO1_B6_u	B24	eMMC_D2/FLASH_D2 [20]
EMMC_D3	/ FLASH_D3	/ GPIO1_B7_u	D21	eMMC_D3/FLASH_D3 [20]
EMMC_D4	/ FLASH_D4	/ GPIO1_C0_u	A25	eMMC_D4/FLASH_D4 [20]
EMMC_D5	/ FLASH_D5	/ GPIO1_C1_u	E21	eMMC_D5/FLASH_D5 [20]
EMMC_D6	/ FLASH_D6	/ GPIO1_C2_u	E22	eMMC_D6/FLASH_D6 [20]
EMMC_D7	/ FLASH_D7	/ GPIO1_C3_u	B25	eMMC_D7/FLASH_D7 [20]
EMMC_CMD	/ FLASH_WRn	/ GPIO1_C4_u	B22	eMMC_CMD/FLASH_WRn [20]
EMMC_CLKOUT	/ FLASH_DQS	/ GPIO1_C5_d	A23	eMMC_CLKOUT — R1300 22R 5% R0402 — eMMC_CLKOUT/FLASH_DQS [20]
EMMC_DATA_STROBE	/ FSPI_CS1n / FLASH_CLE	/ GPIO1_C6_d	A26	eMMC_DATA_STROBE/FLASH_CLE [20]
EMMC_RSTn	/ FSPI_D2	/ FLASH_WPn / GPIO1_C7_d	F20	eMMC_RSTn/FSPI_D2/FLASH_WPn [20]
	FSPI_CLK	/ FLASH_ALE / GPIO1_D0_d	A22	
	FSPI_D0	/ FLASH_RDY / GPIO1_D1_u	C24	
	FSPI_D1	/ FLASH_RDn / GPIO1_D2_u	D23	
	FSPI_CS0n	/ FLASH_CS0n / GPIO1_D3_u	C23	
	FSPI_D3	/ FLASH_CS1n / GPIO1_D4_u	A27	

Default is determined by Pin
FLASH_VOL_SEL/GPIO0_A7_u:
L:VCCIO2 must supply 3.3V
H:VCCIO2 must supply 1.8V

VCCIO2 — H18

VCCIO_FLASH — C1300 100nF X5R 10V C0201

RK3568
BGA636_19R00X19R00X1R20

Note:

"FLASH_VOL_SEL" status and VCCIO_FLASH power supply voltage must match otherwise the IO function of VCCIO2 will be abnormally or the IO of VCCIO2 will be damaged!

When VCCIO2 voltage is connected to 1.8V, FLASH_VOL_SEL must be high
When VCCIO2 voltage is connected to 3.3V, FLASH_VOL_SEL must be low
If VCCIO2 power supply voltage and FLASH_VOL_SEL fails to meet the above relationship,
its function will be abnormally(for example, it cannot be started normally) or IO will be damaged.

RK3568_J(VCCIO3 Domain)

SDMMC0_D2/ARMJTAG_TCK — R1302 22R 5% R0402 — TP1304 TP_0.7
SDMMC0_D3/ARMJTAG_TMS — R1303 22R 5% R0402 — TP1305 TP_0.7
For ARM JTAG

Default
SDMMC0&JTAG

U1000J

VCCIO3 Domain

Operating Voltage=1.8V/3.3V

SDMMC0_D0	/ UART2_TX_M1 / UART6_TX_M1	/ PWM8_M1 / GPIO1_D5_u	J25	SDMMC0_D0 [21]
SDMMC0_D1	/ UART2_RX_M1 / UART6_RX_M1	/ PWM9_M1 / GPIO1_D6_u	J24	SDMMC0_D1 [21]
SDMMC0_D2	/ ARMJTAG_TCK / UART5_CTSn_M0	/ GPIO1_D7_u	H26	SDMMC0_D2/ARMJTAG_TCK [21]
SDMMC0_D3	/ ARMJTAG_TMS / UART5_RTSn_M0	/ GPIO2_A0_u	J23	SDMMC0_D3/ARMJTAG_TMS [21]
SDMMC0_CMD	/ PWM10_M1 / UART5_RX_M0	/ CAN0_TX_M1 / GPIO2_A1_u	H27	SDMMC0_CMD [21]
SDMMC0_CLK	/ TEST_CLKOUT / UART5_TX_M0	/ CAN0_RX_M1 / GPIO2_A2_d	H28	R1304 22R 5% R0402 — SDMMC0_CLK [21]

VCCIO3 — L22

VCCIO_SD — C1301 100nF X5R 10V C0201

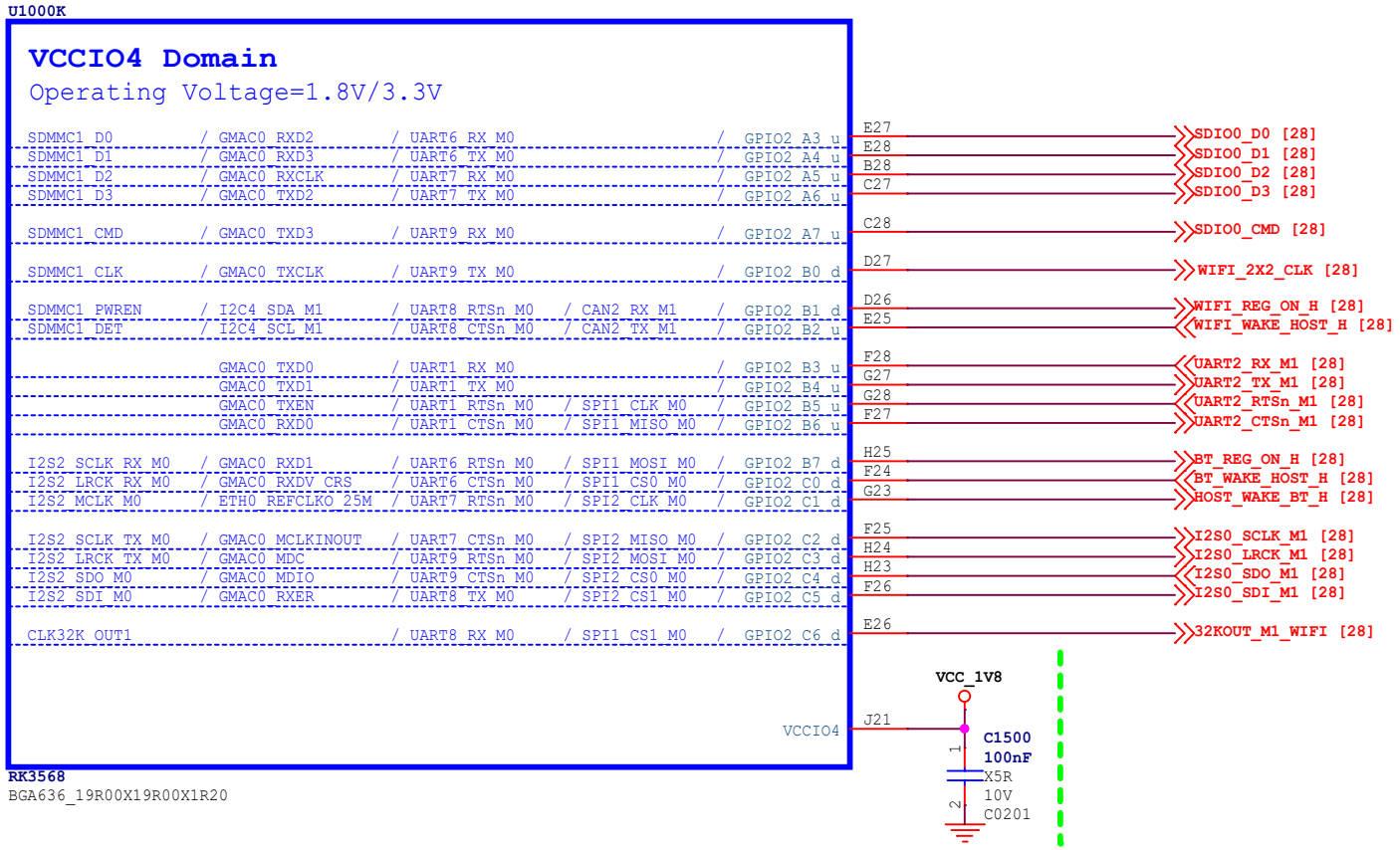
RK3568
BGA636_19R00X19R00X1R20

Note:
Caps of between dashed green lines and U10(
should be placed under the U1000 package

armsom https://www.armsom.org/

Project:	ArmSoM-Sige3				
File:	14.RK3568_Flash/SD Controller				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	14 of 35

RK3568_K(VCCIO4 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

armsom https://www.armsom.org/					
Project:	ArmSoM-Sige3				
File:	15.RK3568_WIFI/BT				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	15 of 35

RK3568_L(VCCIO5 Domain)

U1000L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0	/ VOP_BT656_D0_M0	/ SPI0_MISO_M1	/ PCIE20_CLKREQn_M1	/ I2S1_MCLK_M2	/ GPIO2_D0_d
LCDC_D1	/ VOP_BT656_D1_M0	/ SPI0_MOSI_M1	/ PCIE20_WAKEn_M1	/ I2S1_SCLK_TX_M2	/ GPIO2_D1_d
LCDC_D2	/ VOP_BT656_D2_M0	/ SPI0_CS0_M1	/ PCIE30X1_CLKREQn_M1	/ I2S1_LRCK_TX_M2	/ GPIO2_D2_d
LCDC_D3	/ VOP_BT656_D3_M0	/ SPI0_CLK_M1	/ PCIE30X1_WAKEn_M1	/ I2S1_SDI0_M2	/ GPIO2_D3_d
LCDC_D4	/ VOP_BT656_D4_M0	/ SPI2_CS1_M1	/ PCIE30X2_CLKREQn_M1	/ I2S1_SDI1_M2	/ GPIO2_D4_d
LCDC_D5	/ VOP_BT656_D5_M0	/ SPI2_CS0_M1	/ PCIE30X2_WAKEn_M1	/ I2S1_SDI2_M2	/ GPIO2_D5_d
LCDC_D6	/ VOP_BT656_D6_M0	/ SPI2_MOSI_M1	/ PCIE30X2_PERSTn_M1	/ I2S1_SDI3_M2	/ GPIO2_D6_d
LCDC_D7	/ VOP_BT656_D7_M0	/ SPI2_MISO_M1	/ UART8_TX_M1	/ I2S1_SDO0_M2	/ GPIO2_D7_d
LCDC_CLK	/ VOP_BT656_CLK_M0	/ SPI2_CLK_M1	/ UART8_RX_M1	/ I2S1_SDO1_M2	/ GPIO3_A0_d
LCDC_D8	/ VOP_BT1120_D0	/ SPI1_CS0_M1	/ PCIE30X1_PERSTn_M1	/ SDMMC2_D0_M1	/ GPIO3_A1_d
LCDC_D9	/ VOP_BT1120_D1	/ GMAC1_TXD2_M0	/ I2S3_MCLK_M0	/ SDMMC2_D1_M1	/ GPIO3_A2_d
LCDC_D10	/ VOP_BT1120_D2	/ GMAC1_TXD3_M0	/ I2S3_SCLK_M0	/ SDMMC2_D2_M1	/ GPIO3_A3_d
LCDC_D11	/ VOP_BT1120_D3	/ GMAC1_RXD2_M0	/ I2S3_LRCK_M0	/ SDMMC2_D3_M1	/ GPIO3_A4_d
LCDC_D12	/ VOP_BT1120_D4	/ GMAC1_RXD3_M0	/ I2S3_SDO_M0	/ SDMMC2_CMD_M1	/ GPIO3_A5_d
LCDC_D13	/ VOP_BT1120_CLK	/ GMAC1_TXCLK_M0	/ I2S3_SDI_M0	/ SDMMC2_CLK_M1	/ GPIO3_A6_d
LCDC_D14	/ VOP_BT1120_D5	/ GMAC1_RXCLK_M0		/ SDMMC2_DET_M1	/ GPIO3_A7_d
LCDC_D15	/ VOP_BT1120_D6	/ ETH1_REFCLKO_25M_M0		/ SDMMC2_PWREN_M1	/ GPIO3_B0_d
LCDC_D16	/ VOP_BT1120_D7	/ GMAC1_RXD0_M0	/ UART4_RX_M1	/ PWM8_M0	/ GPIO3_B1_d
LCDC_D17	/ VOP_BT1120_D8	/ GMAC1_RXD1_M0	/ UART4_TX_M1	/ PWM9_M0	/ GPIO3_B2_d
LCDC_D18	/ VOP_BT1120_D9	/ GMAC1_RXDV_CRS_M0	/ I2C5_SCL_M0	/ PDM_SDI0_M2	/ GPIO3_B3_d
LCDC_D19	/ VOP_BT1120_D10	/ GMAC1_RXER_M0	/ I2C5_SDA_M0	/ PDM_SDI1_M2	/ GPIO3_B4_d
LCDC_D20	/ VOP_BT1120_D11	/ GMAC1_TXD0_M0	/ I2C3_SCL_M1	/ PWM10_M0	/ GPIO3_B5_d
LCDC_D21	/ VOP_BT1120_D12	/ GMAC1_TXD1_M0	/ I2C3_SDA_M1	/ PWM11_IR_M0	/ GPIO3_B6_d
LCDC_D22	/ PWM12_M0	/ GMAC1_TXEN_M0	/ UART3_TX_M1	/ PDM_SDI2_M2	/ GPIO3_B7_d
LCDC_D23	/ PWM13_M0	/ GMAC1_MCLKINOUT_M0	/ UART3_RX_M1	/ PDM_SDI3_M2	/ GPIO3_C0_d
LCDC_HSYNC	/ VOP_BT1120_D13	/ SPI1_MOSI_M1	/ PCIE20_PERSTn_M1	/ I2S1_SDO2_M2	/ GPIO3_C1_d
LCDC_VSYNC	/ VOP_BT1120_D14	/ SPI1_MISO_M1	/ UART5_TX_M1	/ I2S1_SDO3_M2	/ GPIO3_C2_d
LCDC_DEN	/ VOP_BT1120_D15	/ SPI1_CLK_M1	/ UART5_RX_M1	/ I2S1_SCLK_RX_M2	/ GPIO3_C3_d
PWM14_M0	/ VOP_PWM_M1	/ GMAC1_MDC_M0	/ UART7_TX_M1	/ PDM_CLK1_M2	/ GPIO3_C4_d
PWM15_IR_M0	/ SPDIF_TX_M1	/ GMAC1_MDIO_M0	/ UART7_RX_M1	/ I2S1_LRCK_RX_M2	/ GPIO3_C5_d

VCCIO5_1
VCCIO5_2

RK3568
BGA636_19R00X19R00X1R20

AG6 PCIE20_CLKREQn [25]
AD7 PCIE20_WAKEn [25]
AC8
AC7 GPIO2_D3 [33]
AF5 SPI2_CS1 [33]
AF6 SPI2_CS0 [33]
AD6 SPI2_MOSI [33]
AH5 SPI2_MISO [33]
AH4 SPI2_CLK [33]
AB8 GPIO3_A1 [33]
AE5 GPIO3_A3 [33]
AG4 I2S3_SCLK_M0 [33]
AF4 I2S3_LRCK_M0 [33]
AH3 I2S3_SDO_M0 [33]
AG3 I2S3_SDI_M0 [33]
AH2 GPIO3_A7 [33]
AG2 GPIO3_B0 [33]
AG1 GPIO3_B1 [33]
AF2 GPIO3_B2 [33]
AF1 I2C5_SCL_M0 [33]
AE1 I2C5_SDA_M0 [33]
AE2 I2C3_SCL_M1 [33]
AE3 I2C3_SDA_M1 [33]
AD4 GPIO3_B7 [33]
AD2 GPIO3_C0 [33]
AD1 PCIE20_PERSTn [25]
AA7 GPIO3_C2 [33]
AC4 GPIO3_C3 [33]
AC3 PWM14_M0 [33]
AC2 PWM15_IR_M0 [33]

VCC_3V3
V10
V11
C1800 100nF X5R 10V C0201

VCC_3V3
R1206 2.2K 5% R0402
R1207 2.2K 5% R0402
I2C5_SCL_M0
I2C5_SDA_M0

VCC_3V3
R9325 2.2K 5% R0402
R9326 2.2K 5% R0402
I2C3_SCL_M1
I2C3_SDA_M1

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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Project:	ArmSoM-Sige3				
File:	16.RK3568_40PIN				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	16 of 35

RK3568_M(VCCIO6 Domain)

U1000M

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

CIF_D0	EBC_SDDO0	SDMMC2_D0_M0	I2S1_MCLK_M1	VOP_BT656_D0_M1 / GPIO3_C6_d
CIF_D1	EBC_SDDO1	SDMMC2_D1_M0	I2S1_SCLK_TX_M1	VOP_BT656_D1_M1 / GPIO3_C7_d
CIF_D2	EBC_SDDO2	SDMMC2_D2_M0	I2S1_LRCK_TX_M1	VOP_BT656_D2_M1 / GPIO3_D0_d
CIF_D3	EBC_SDDO3	SDMMC2_D3_M0	I2S1_SDO0_M1	VOP_BT656_D3_M1 / GPIO3_D1_d
CIF_D4	EBC_SDDO4	SDMMC2_CMD_M0	I2S1_SDI0_M1	VOP_BT656_D4_M1 / GPIO3_D2_d
CIF_D5	EBC_SDDO5	SDMMC2_CLK_M0	I2S1_SDI1_M1	VOP_BT656_D5_M1 / GPIO3_D3_d
CIF_D6	EBC_SDDO6	SDMMC2_DET_M0	I2S1_SDI2_M1	VOP_BT656_D6_M1 / GPIO3_D4_d
CIF_D7	EBC_SDDO7	SDMMC2_PWREN_M0	I2S1_SDI3_M1	VOP_BT656_D7_M1 / GPIO3_D5_d
CIF_D8	EBC_SDDO8	GMAC1_TXD2_M1	UART1_TX_M1	PDM_CLK0_M1 / GPIO3_D6_d
CIF_D9	EBC_SDDO9	GMAC1_TXD3_M1	UART1_RX_M1	PDM_SDI0_M1 / GPIO3_D7_d
CIF_D10	EBC_SDDO10	GMAC1_TXCLK_M1		PDM_CLK1_M1 / GPIO4_A0_d
CIF_D11	EBC_SDDO11	GMAC1_RXD2_M1		PDM_SDI1_M1 / GPIO4_A1_d
CIF_D12	EBC_SDDO12	GMAC1_RXD3_M1	UART7_TX_M2	PDM_SDI2_M1 / GPIO4_A2_d
CIF_D13	EBC_SDDO13	GMAC1_RXCLK_M1	UART7_RX_M2	PDM_SDI3_M1 / GPIO4_A3_d
CIF_D14	EBC_SDDO14	GMAC1_TXD0_M1	UART9_TX_M2	I2S2_LRCK_TX_M1 / GPIO4_A4_d
CIF_D15	EBC_SDDO15	GMAC1_TXD1_M1	UART9_RX_M2	I2S2_LRCK_RX_M1 / GPIO4_A5_d
ISP_FLASHTRIGOUT	EBC_SDCE0	GMAC1_TXEN_M1	SPI3_CS0_M0	I2S1_SCLK_RX_M1 / GPIO4_A6_d
CAM_CLKOUT0	EBC_SDCE1	GMAC1_RXD0_M1	SPI3_CS1_M0	I2S1_LRCK_RX_M1 / GPIO4_A7_d
CAM_CLKOUT1	EBC_SDCE2	GMAC1_RXD1_M1	SPI3_MISO_M0	I2S1_SDO1_M1 / GPIO4_B0_d
ISP_PRELIGHT_TRIG	EBC_SDCE3	GMAC1_RXDV_CRS_M1		I2S1_SDO2_M1 / GPIO4_B1_d
I2C4_SDA_M0	EBC_VCOM	GMAC1_RXER_M1	SPI3_MOSI_M0	I2S2_SDI_M1 / GPIO4_B2_d
I2C4_SCL_M0	EBC_GDOE	ETH1_REFCLKO_25M_M1	SPI3_CLK_M0	I2S2_SDO_M1 / GPIO4_B3_d
I2C2_SDA_M1	EBC_GDSP	CAN2_RX_M0	ISP_FLASH_TRIGIN	VOP_BT656_CLK_M1 / GPIO4_B4_d
I2C2_SCL_M1	EBC_SDSHR	CAN2_TX_M0		I2S1_SDO3_M1 / GPIO4_B5_d
CIF_HREF	EBC_SDLE	GMAC1_MDC_M1	UART1_RTSn_M1	I2S2_MCLK_M1 / GPIO4_B6_d
CIF_VSYNC	EBC_SDOE	GMAC1_MDIO_M1		I2S2_SCLK_TX_M1 / GPIO4_B7_d
CIF_CLKOUT	EBC_GDCLK		PWM11_IR_M1	GPIO4_C0_d
CIF_CLKIN	EBC_SDCLK	GMAC1_MCLKINOUT_M1	UART1_CTSn_M1	I2S2_SCLK_RX_M1 / GPIO4_C1_d

VCCIO6_1
VCCIO6_2

RK3568
BGA636_19R00X19R00X1R20

AC5 LCD_EN_H_GPIO3_C6 [26]
AA6 LCD_RST_L_GPIO3_C7 [26]
AB5 TP_INT_L_GPIO0_B5 [26]
AB1 TP_RST_L_GPIO0_B6 [26]
Y7
AC1 MIPI_CAM1_PDN_L_GPIO3_D3 [25]
AA1 MIPI_CAM0_RST_L_GPIO3_D4 [25]
AA5 MIPI_CAM0_PDN_L_GPIO3_D5 [25]

VCC_1V8
R1606 2.2K 5% R0402
R1607 2.2K 5% R0402
I2C2_SDA_M1
I2C2_SCL_M1

VCC_1V8
R1801 10K 5% R0402
GMAC1_INT/PMEB_GPIO3_A7

Y6 GMAC1_TXD2_M1_SOC R1600 22R 5% R0402 GMAC1_TXD2_M1 [29]
Y5 GMAC1_TXD3_M1_SOC R1601 22R 5% R0402 GMAC1_TXD3_M1 [29]
AA3 GMAC1_TXCLK_M1_SOC R1602 22R 5% R0402 GMAC1_TXCLK_M1 [29]
AA2 GMAC1_RXD2_M1 [29]
Y4 GMAC1_RXD3_M1 [29]
Y3 GMAC1_RXCLK_M1 [29]
Y2 GMAC1_TXD0_M1_SOC R1603 22R 5% R0402 GMAC1_TXD0_M1 [29]
Y1 GMAC1_TXD1_M1_SOC R1604 22R 5% R0402 GMAC1_TXD1_M1 [29]
W2 GMAC1_TXEN_M1_SOC R1605 22R 5% R0402 GMAC1_TXEN_M1 [29]
W1 GMAC1_RXD0_M1 [29]
V7 GMAC1_RXD1_M1 [29]
V2 GMAC1_RXDV_CRS_M1 [29]
V4 GMAC1_INT/PMEB_GPIO3_A7 [29]
V1 ETH1_REFCLKO_25M_M1_SOC R1608 22R 5% R0402 ETH1_REFCLKO_25M_M1 [29]
V6 I2C2_SDA_M1 [25]
V5 I2C2_SCL_M1 [25]
U5 R1611 0R 5% R0402 GMAC1_MDC_M1 [29]
U4 GMAC1_MDIO_M1 [29]
U3 CIF_CLKOUT_SOC R1609 22R 5% R0402 CIF_CLKOUT [25]
U2 GMAC1_MCLKINOUT_M1 [29]

VCC_1V8
R9
U9
C1602 100nF X5R 10V C0201

GMAC	Direction	GEPHY
GMACx_MDC	------>	PHYx_MDC
GMACx_MDIO	<------>	PHYx_MDIO
ETHx_REFCLKO_25M	------>	PHYx OSC
GMACx_MCLKINOUT	<------	PHYx_CLKOUT125(Option)
GPIO	------>	PHYx_RSTn
GPIO	<------	PHYx_INT/PMEB
GMACx_RXER		NC

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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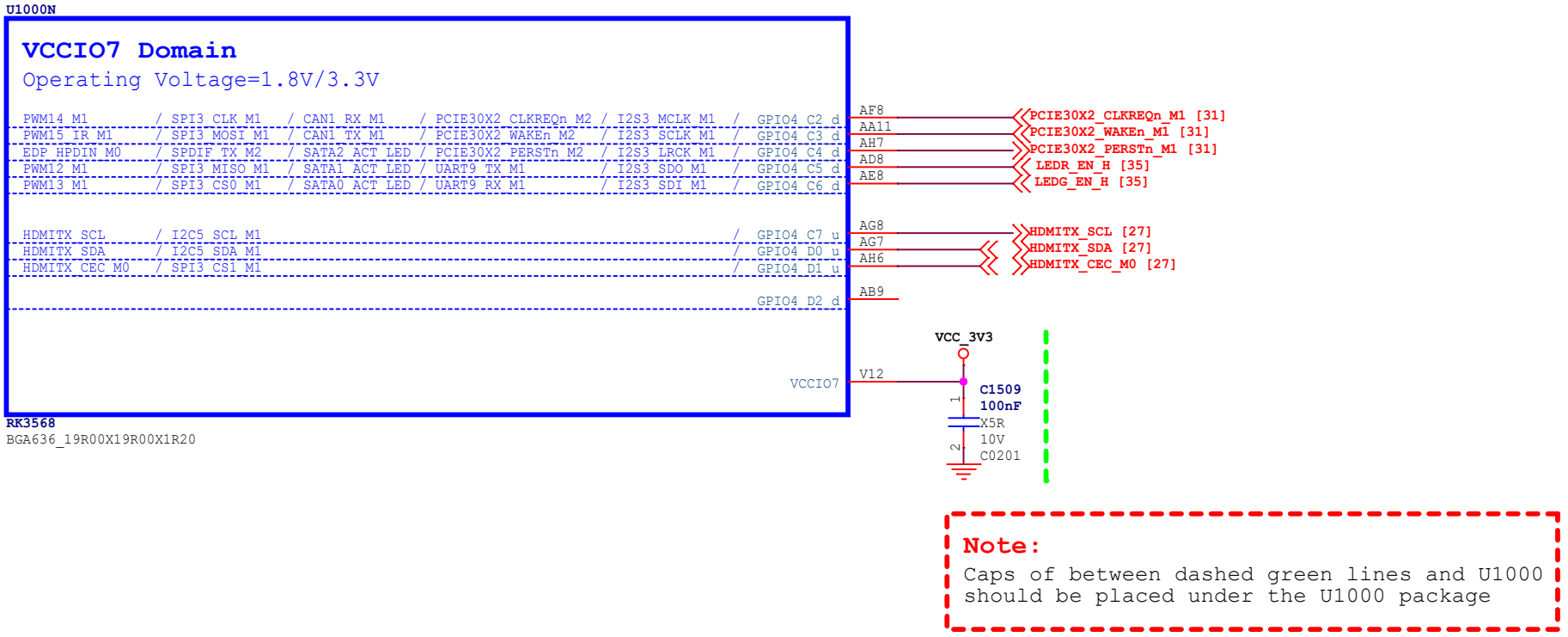
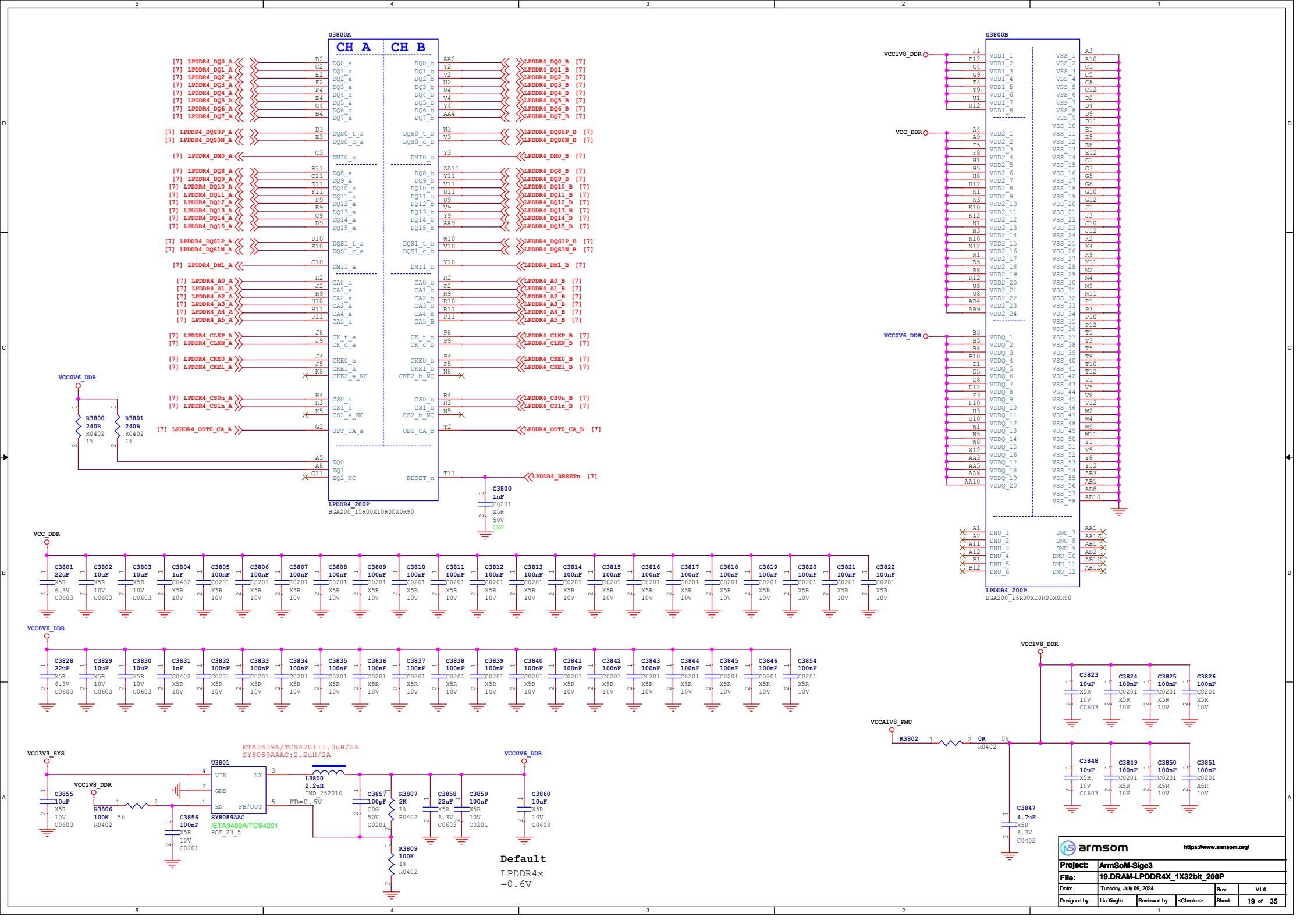
Project:	ArmSoM-Sige3				
File:	17.RK3568_Ethernet/Camera/LCD				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	17 of 35

RK3568_N(VCCIO7 Domain)

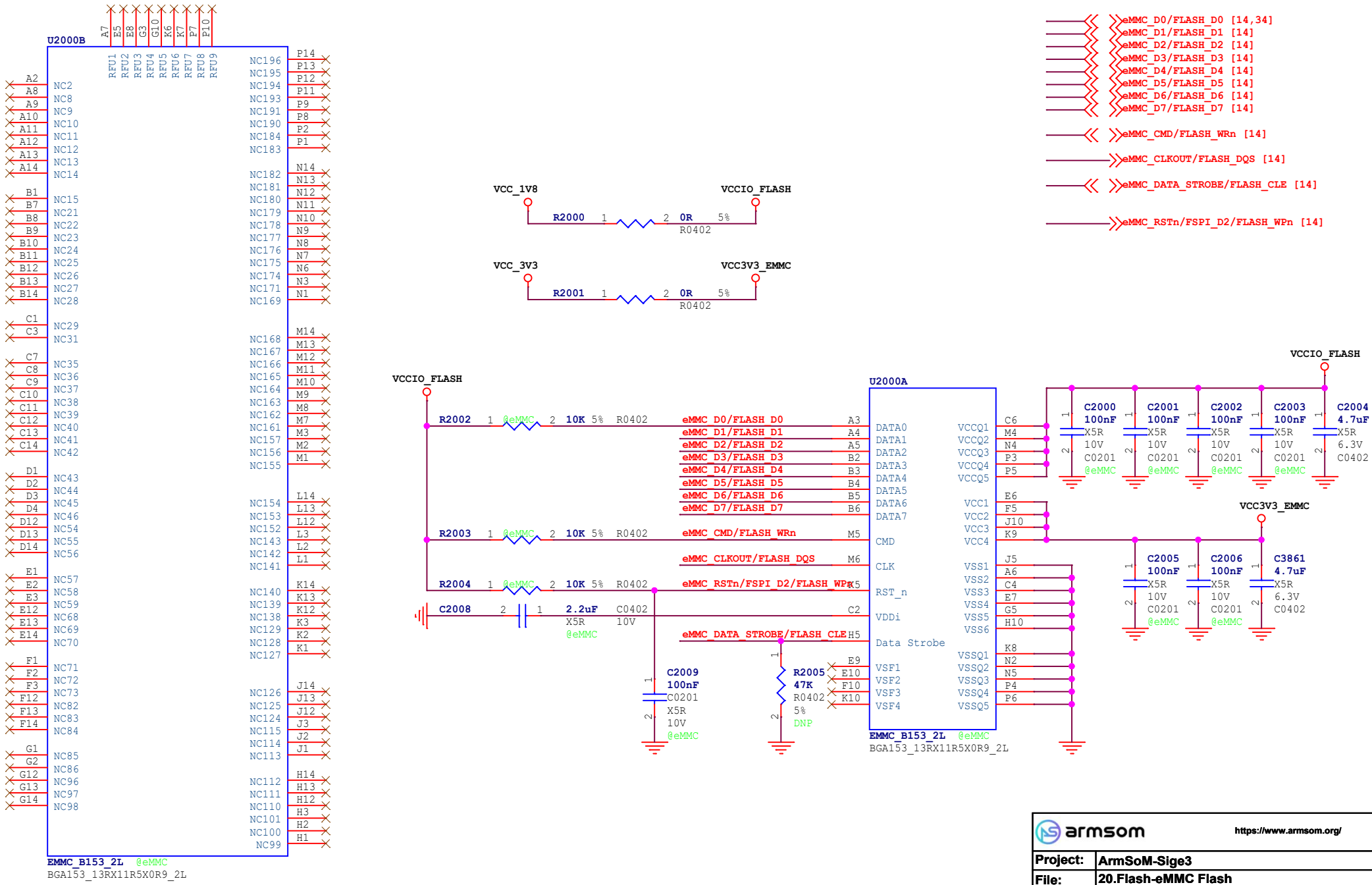


Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

armsom https://www.armsom.org/					
Project:	ArmSoM-Sige3				
File:	18.RK3568_PCIE30x2/HDMITX Contr				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	18 of 35


U3800A
CH A
CH B
LPDDR4_200P
BGA200_15R00X10R00X0R90
U3800B
LPDDR4_200P
BGA200_15R00X10R00X0R90
VCC_DDR
VCC0V6_DDR
VCC1V8_DDR
VCCA1V8_PMU
VCC3V3_SYS
R3800 240R R0402 1%
R3801 240R R0402 1%
C3800 1nF C0201 X5R 50V DNP
U3801
SY8089AAC
/ETA3409A/TCS4201
SOT_23_5
ETA3409A/TCS4201:1.0uH/2A
SY8089AAAC:2.2uH/2A
L3800 2.2uH IND_252010
FB=0.6V
R3806 100K R0402 5%
R3807 2K 1% R0402
R3809 100K 1% R0402
C3855 10uF X5R 10V C0603
C3856 100nF X5R 10V C0201
C3857 100pF C0G 50V C0201
C3858 22uF X5R 6.3V C0603
C3859 100nF X5R 10V C0201
C3860 10uF X5R 10V C0603
R3802 0R R0402 5%
C3847 4.7uF X5R 6.3V C0402
Default
LPDDR4x
=0.6V
armsom
https://www.armsom.org/
Project: ArmSoM-Sige3
File: 19.DRAM-LPDDR4X_1X32bit_200P
Date: Tuesday, July 09, 2024
Rev: V1.0
Designed by: Liu Xinglin
Reviewed by: <Checker>
Sheet: 19 of 35

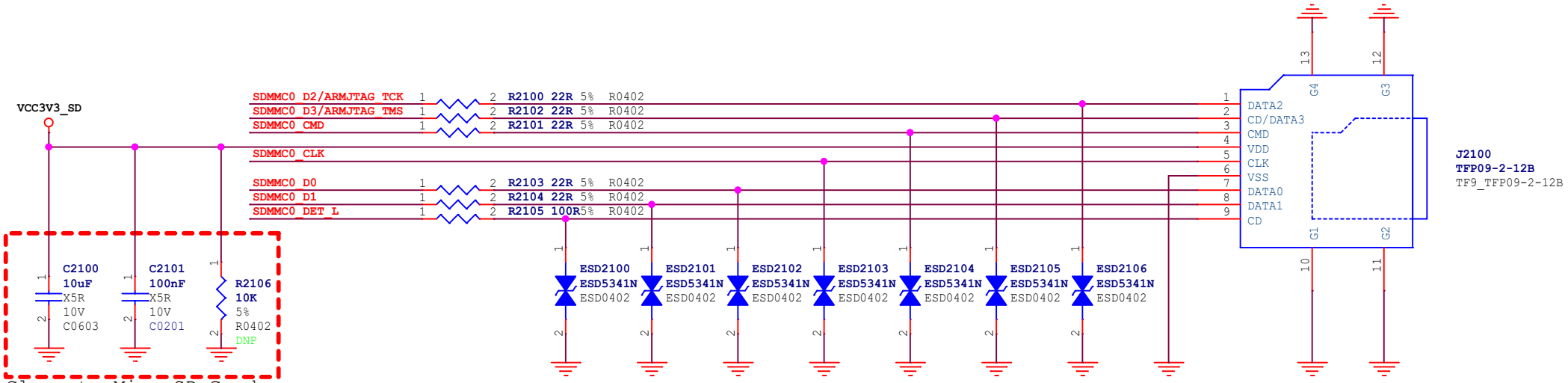
eMMC Flash



armsom	https://www.armsom.org/				
Project:	ArmSoM-Sige3				
File:	20.Flash-eMMC Flash				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	20 of 35

MicroSD Card

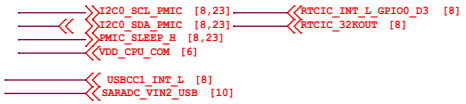
SDMMC0_D0 [14]
SDMMC0_D1 [14]
SDMMC0_D2/ARMJTAG_TCK [14]
SDMMC0_D3/ARMJTAG_TMS [14]
SDMMC0_CMD [14]
SDMMC0_CLK [14]
SDMMC0_DET_L [8]

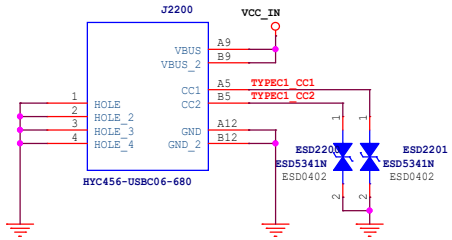


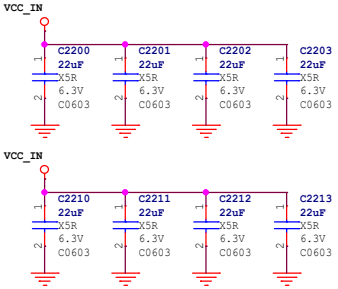
MicroSD Card

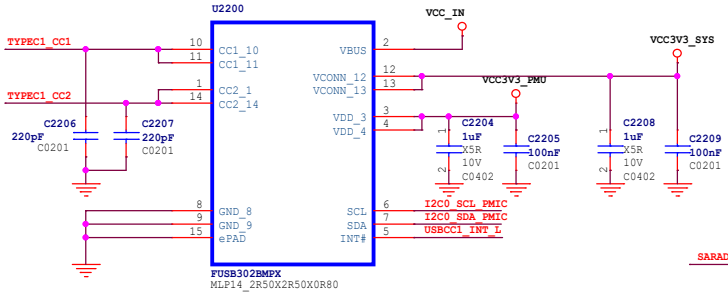
armsom	https://www.armsom.org/				
Project:	ArmSoM-Sige3				
File:	21.Flash-MicroSD Card				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	21 of 35

DCIN

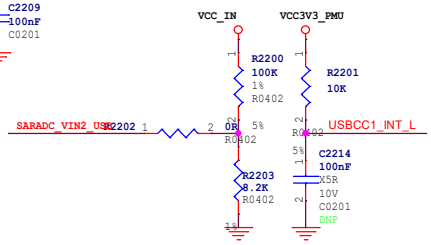








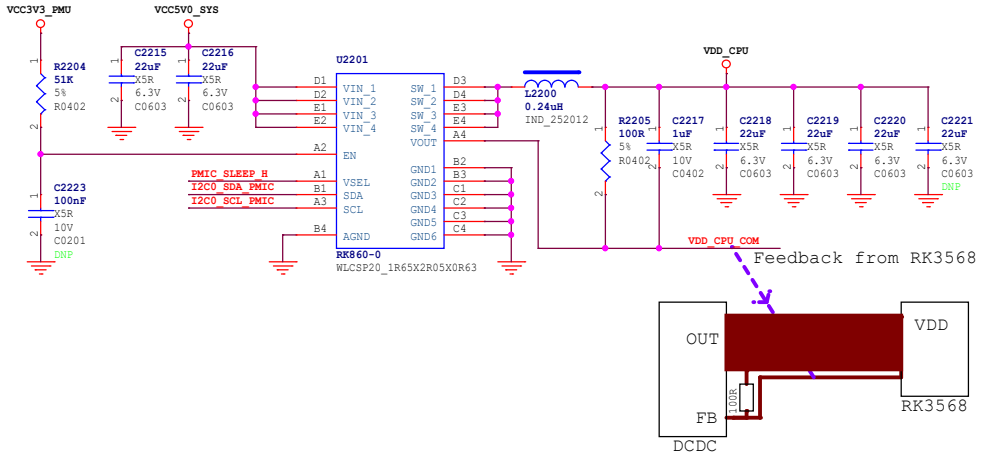
TYPEC_IN	12bit_ADC	ADC6
5V	35E	0.37V
9V	610	0.68V
12V	815	0.9V
15V	A1A	1.136V
20V	D79	1.51V



7bit address=0x22

VBUS of FUSB302BMPX: 4 to 21 TYP = 5V
VDD of FUSB302BMPX: 3 to 5.5 TYP = 3.3V
VCONN of FUSB302BMPX: 3 to 5.5

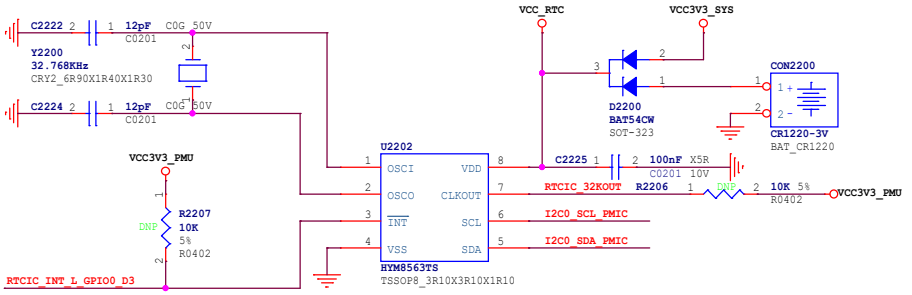
VDD_CPU



RTC IC

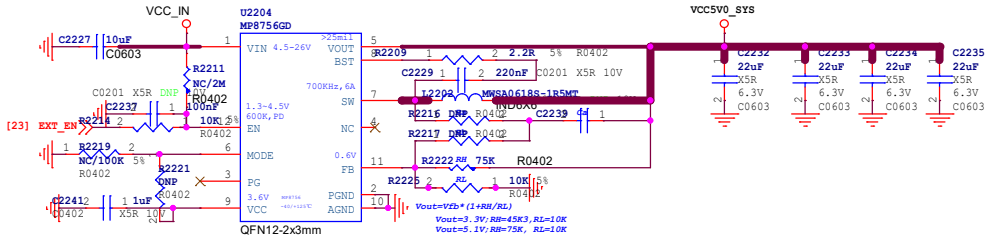
Note:

The power off hold time scheme is required,
It is recommended to use external RTC IC
But, it will not support the timing poweron function

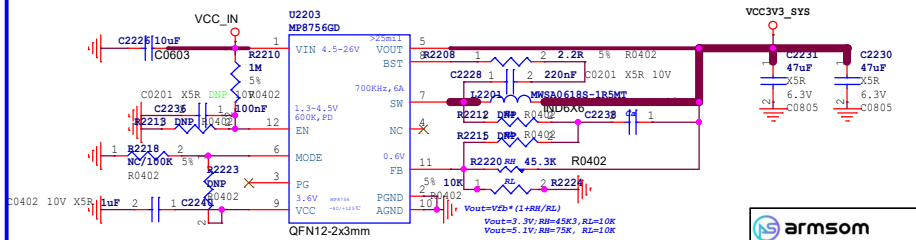


Address:Read A3H,Write A2H

VCC5V0_SYS



VCC3V3_SYS



armsom https://www.armsom.org/

Project:	ArmSoM-Sige3				
File:	22.Power_DC IN/Ext Discrete/RTC				
Date:	Friday, July 19, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	22 of 35

I2C0_SCL_PMIC [8,22]
I2C0_SDA_PMIC [8,22]
PMIC_INT_L [8]
PMIC_SLEEP_H [8,22]
RESETn [8,34]
RK809_PWRON [34]
I2S1_MCLK_M0_RK809 [13]
I2S1_SCLK_TX_M0_RK809 [13]
I2S1_LRCK_TX_M0_RK809 [13]
I2S1_SDO0_M0_RK809 [13]
I2S1_SDI0_M0/PDM_SDI0_M0_RK809 [13]
PDM_CLK0_M0_RK809 [13]
EXT_EN [22]
HPL_OUT [32]
HP_SNS [32]
HPR_OUT [32]
SPKN_OUT [32]
SPKP_OUT [32]
MIC1_INP [32]
MIC1_INN [32]

OUT
VDD
FB
100R
BUCK4
RK3568

PMIC RK809 DCDC

VDD_LOGIC
VCC3V3_SYS
U2300A
C2306 22uF X5R 6.3V C0603
C2310 100nF X5R 10V C0201
R2300 100R 5% R0402
C2311 22uF X5R 6.3V C0603
C2312 22uF X5R 6.3V C0603
L2300 470nH SW1 IND_252010 DCR<50mohm ON 0.9V
VCC1 BUCK1 2.5A 0.5-2.4V FB1 SW1
Feedback from RK3568
VDD_GPU
C2322 100nF X5R 10V C0201
R2302 100R 5% R0402
C2323 22uF X5R 6.3V C0603
C2324 22uF X5R 6.3V C0603
L2302 470nH SW2 IND_252010 DCR<50mohm ON 0.9V
VCC2 BUCK2 2.5A 0.5-2.4V FB2 SW2
BUCK3 1.5A 0.5-2.4V FB3=0.8V VCC3 SW3 VBUCK3 FB3
VCC4 BUCK4 1.5A 0.5-3.4V FB4 SW4
RK809-5 QFN68_7R00X7R00X0R80_T
C2307 10uF X5R 10V C0603
L2301 470nH IND_252010 DCR<50mohm OFF 0.9V
C2313 22uF X5R 6.3V C0603
C2314 22uF X5R 6.3V C0603
VDD_NPU
R2301 100R 5% R0402
C2315 100nF X5R 10V C0201
Feedback from RK3568
C2320 10uF X5R 10V C0603
L2303 470nH IND_252010 DCR<50mohm
C2325 22uF X5R 6.3V C0603
C2326 10uF X5R 10V C0603
VCC_DDR
R2303 62K 1% R0402
Default DDR4
FB=0.8V
R2304 120K 1% R0402

DDR4	1.21V	62K 1%
LPDDR4/4x	1.11V	47K 1%
DDR3	1.53V	110K 1%
DDR3L	1.35V	82K 1%
LPDDR3	1.25V	68K 1%

VDD Pin
OUT
FB
100R
RK3568
BUCK1/BUCK2

PMIC RK809 LDO

VCC3V3_SYS
U2300B
400mA LDO: 400mA@Vin>3V 200mA@Vin>2V
Default ON/OFF
VCC5 LDO1 400mA C2301 1uF X5R 10V C0402 OFF 0.9V C2300 1uF X5R 10V C0402 VDDA0V9_IMAGE
VCC6 LDO2 400mA ON 0.9V C2302 1uF X5R 10V C0402 VDDA_0V9
Low noise LDO3 100mA ON 0.9V C2303 1uF X5R 10V C0402 VDDA0V9_PMU
Codec vddio LDO4 400mA C2308 1uF X5R 10V C0402 OFF 3.3V C2304 4.7uF X5R 6.3V C0402 VCCIO_ACODEC
LDO5 400mA ON 3.3V C2305 1uF X5R 10V C0402 VCCIO_SD
LDO6 400mA ON 3.3V C2309 1uF X5R 10V C0402 VCC3V3_PMU
VCC7 LDO7 400mA C2317 1uF X5R 10V C0402 ON 1.8V C2316 1uF X5R 10V C0402 VCCA_1V8
LDO8 400mA ON 1.8V C2318 1uF X5R 10V C0402 VCCA1V8_PMU
LDO9 400mA OFF 1.8V C2319 1uF X5R 10V C0402 VCCA1V8_IMAGE
VCC8 2.1A SWOUT2 C2327 1uF X5R 10V C0402 ON 3.3V C2321 1uF X5R 10V C0402 VCC3V3_SD
2.1A SWOUT1 ON 3.3V C2328 10uF X5R 10V C0603 VCC_3V3
VCC8\9: 2.7V-5.5V
BUCK5 1.5V-3.6V 2.5A SW5 FB5 ON 1.8V L2304 470nH DCR<50mohm IND_252010 C2329 22uF X5R 6.3V C0603 C2330 22uF X5R 6.3V C0603 VCC_1V8
VCC9 C2331 10uF X5R 10V C0603
RK809-5 QFN68_7R00X7R00X0R80_T
R2305
R2306 0R 5% R0402
DNP USB_AVDD_0V9 R0402 C2332 1uF X5R 10V C0402
USB_AVDD_1V8 C2333 1uF X5R 10V C0402
MIPI_AVDD_0V9 C2334 1uF X5R 10V C0402
MIPI_AVDD_1V8 C2335 1uF X5R 10V C0402
VDDA_0V9 FB2300 0.030ohm 120R-100MHz L0603
VCCA_1V8 FB2301 0.030ohm 120R-100MHz L0603
VDDA0V9_IMAGE FB2302 0.030ohm 120R-100MHz L0603
VCCA1V8_IMAGE FB2303 0.030ohm 120R-100MHz L0603

PMIC RK809 Managerment

Note:
If the external RTC IC is used,
Can choose not mounted

U2300C
VCC3V3_SYS
C2337 1uF X5R 10V RK809_VREF C0402
VREF GNDREF ePAD
C2342 22pF C0G 50V C0201
Y2300 32.768KHz CRY2_6R90X1R40X1R30
C2345 22pF C0G 50V C0201
XIN XOUT
Gas Gauge
VCC_RTC C2338 1uF X5R 10V C0402
BATDIV SNSP SNSN EXT_EN VDC PWRON
I2C0_SDA_PMIC R2308 22R 5% R0402 SDA_809 SDA
I2C0_SCL_PMIC R2309 22R 5% R0402 SCL_809 SCL
PMIC_INT_L INT
PMIC_SLEEP_H SLEEP
CLK32K
VCC3V3_PMU R2311 10K 5% R0402 RESETn RESETB
C2351 100nF X5R 10V C0201
RK809-5 QFN68_7R00X7R00X0R80_T
EXT_EN
RK809_VDC 1.2V
RK809_PWRON
C2352 100nF X5R 10V C0201
C2353 10nF X5R 25V C0201
R2310 20K R0402
R2312 11K 5% R0402
U2301 /Reset Vcc GND SGM803B-SXN3LG/TR RESET THRESHOLD =2.93V SOT_23 DNP
C2354 100nF X5R 10V C0201 DNP

Note:
For quick Power ON/OFF
Application

PMIC RK809 CODEC

VCC5V0_SYS
FB2304 120R-100MHz L0603 2A
U2300D
C2336 10uF X5R 10V C0603
C2339 4.7uF X5R 6.3V C0402
C2340 1uF X5R 10V C0402 VCC_CPVDD
C2343 2.2uF X5R 10V C0402 VCC_CPVSS
C2344 1uF X5R 10V C0402 VCC_1P8D
C2346 1uF X5R 10V C0402 VCC_1P8A
VCC_SPK_HP CPn CPp VCC_CPVDD VCC_CPVSS VCC_1P8D Power from VCC_RTC VCC_1P8A
I2S1_MCLK_M0_RK809
I2S1_SCLK_TX_M0_RK809
I2S1_LRCK_TX_M0_RK809
I2S1_SDO0_M0_RK809
I2S1_SDI0_M0/PDM_SDI0_M0_RK809
PDM_CLK0_M0_RK809
MCLK BCLK LRCLK SDI SDO/PDMDATA PDMCLK
IO Power =LDO4
HPL_OUT HP_SNS HPR_OUT SPK_OUTn SPK_OUTp MIC1p MIC_L MIC1n MIC_R
HPL_OUT
HP_SNS R2307 0R 5% R0402 DNP
HPR_OUT
C2341 680pF C0G 50V C0201
SPKN FB2305 180R-100M 1.5A L0603 SPKN_OUT
SPKP FB2306 180R-100M 1.5A L0603 SPKP_OUT
C2347 680pF C0G 50V C0201
C2348 100nF X5R 10V C0201 MIC1_INP
C2349 27pF C0G 50V C0201
C2350 100nF X5R 10V C0201 MIC1_INN
C2355 27pF C0G 50V C0201
RK809-5 QFN68_7R00X7R00X0R80_T

Note:
If RK809-5 codec is not used,
then Pin 14,15,16,17,19,40 Tie VSS
Pin 18,36,37,38,35,39,41,34,32,43,42
Leave floating

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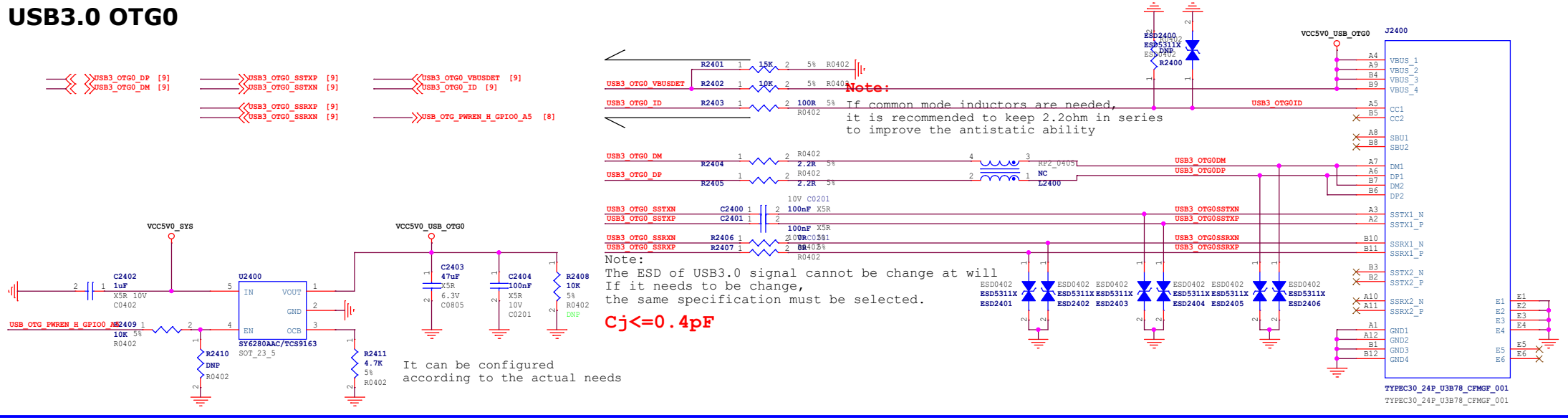
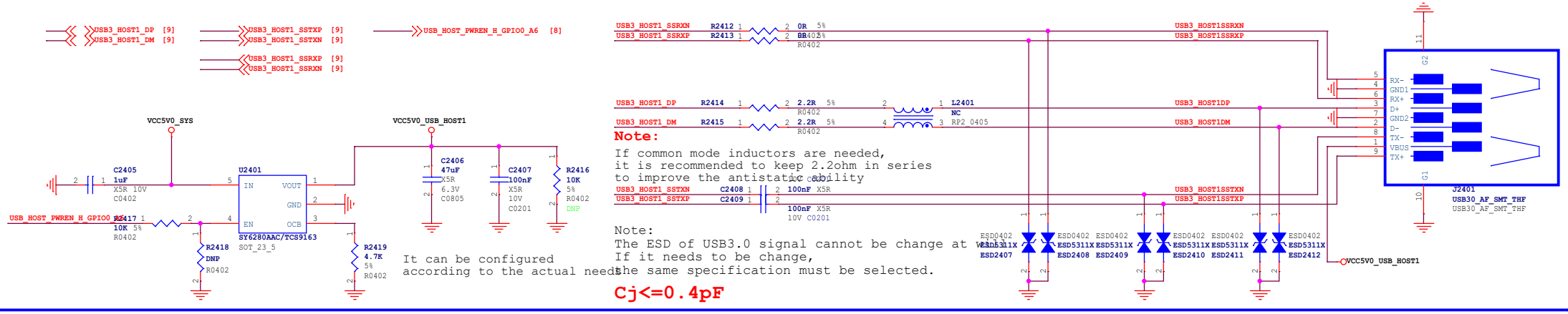
Project:	ArmSoM-Sige3				
File:	23.Power_PMIC				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	23 of 35

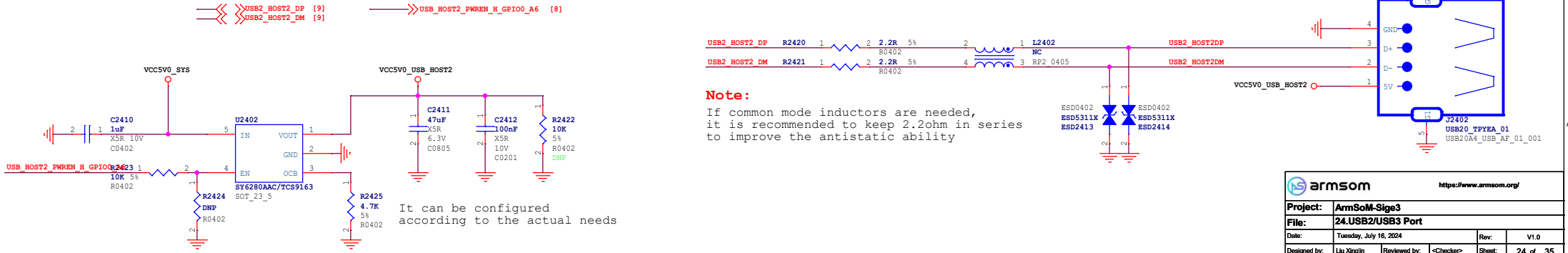
USB3.0 OTG0



USB3.0 HOST1

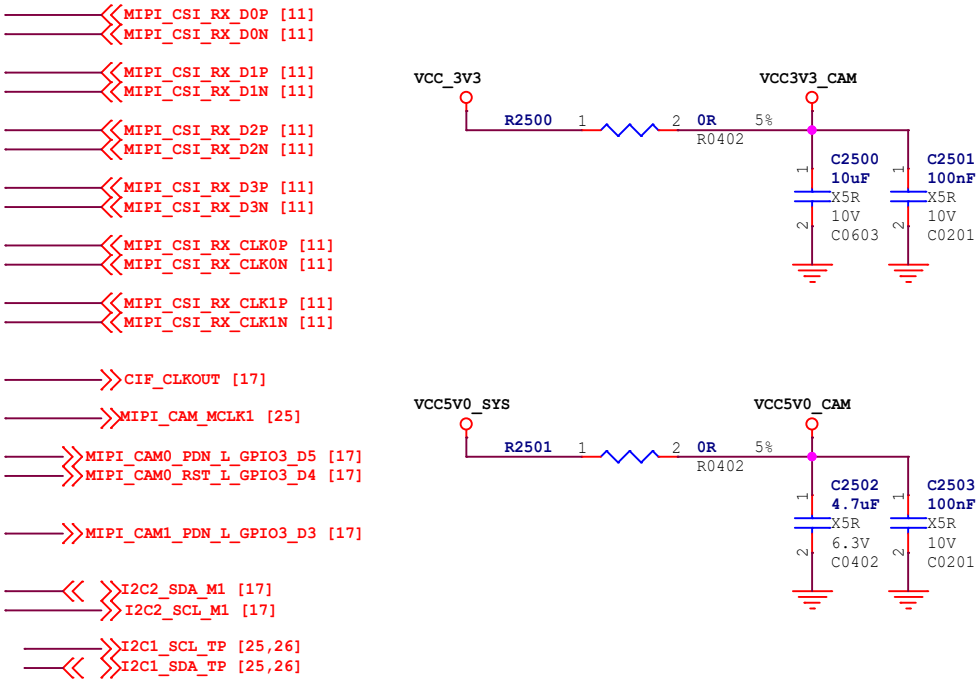


USB2.0 HOST2



armsom	https://www.armsom.org/				
Project:	ArmSoM-Sige3				
File:	24.USB2/USB3 Port				
Date:	Tuesday, July 16, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	24 of 35

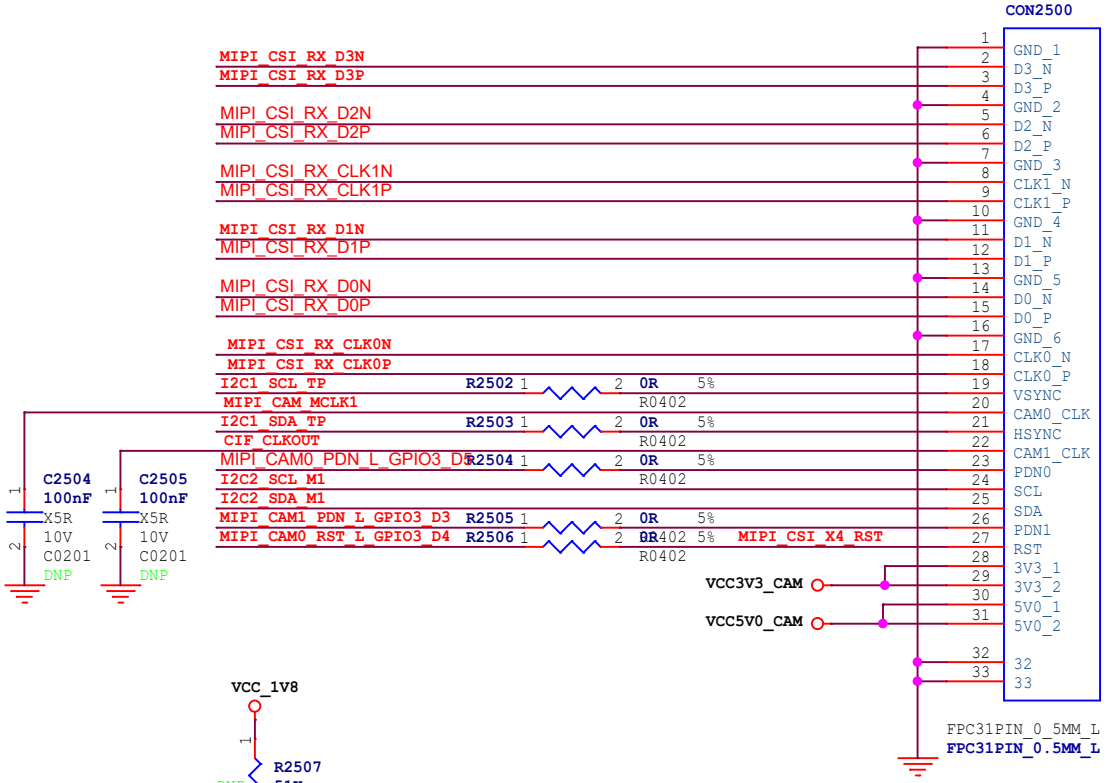
Camera0:MIPI_CSI_RX 4Lanes

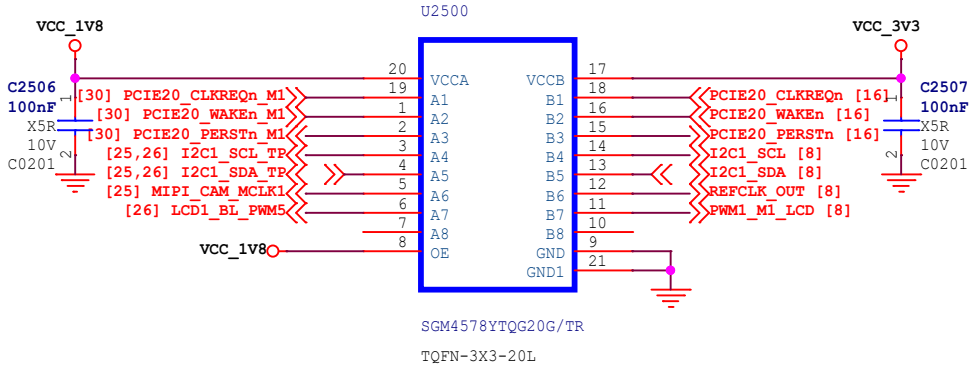


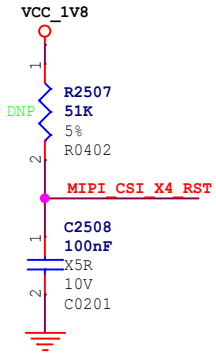
Note:

Camera MCLK can select the following clock:
1:CAM_CLKOUT0
2:CAM_CLKOUT1
3:CIF_CLKOUT
4:REFCLK_OUT(24MHz)

Attention to the voltage matching

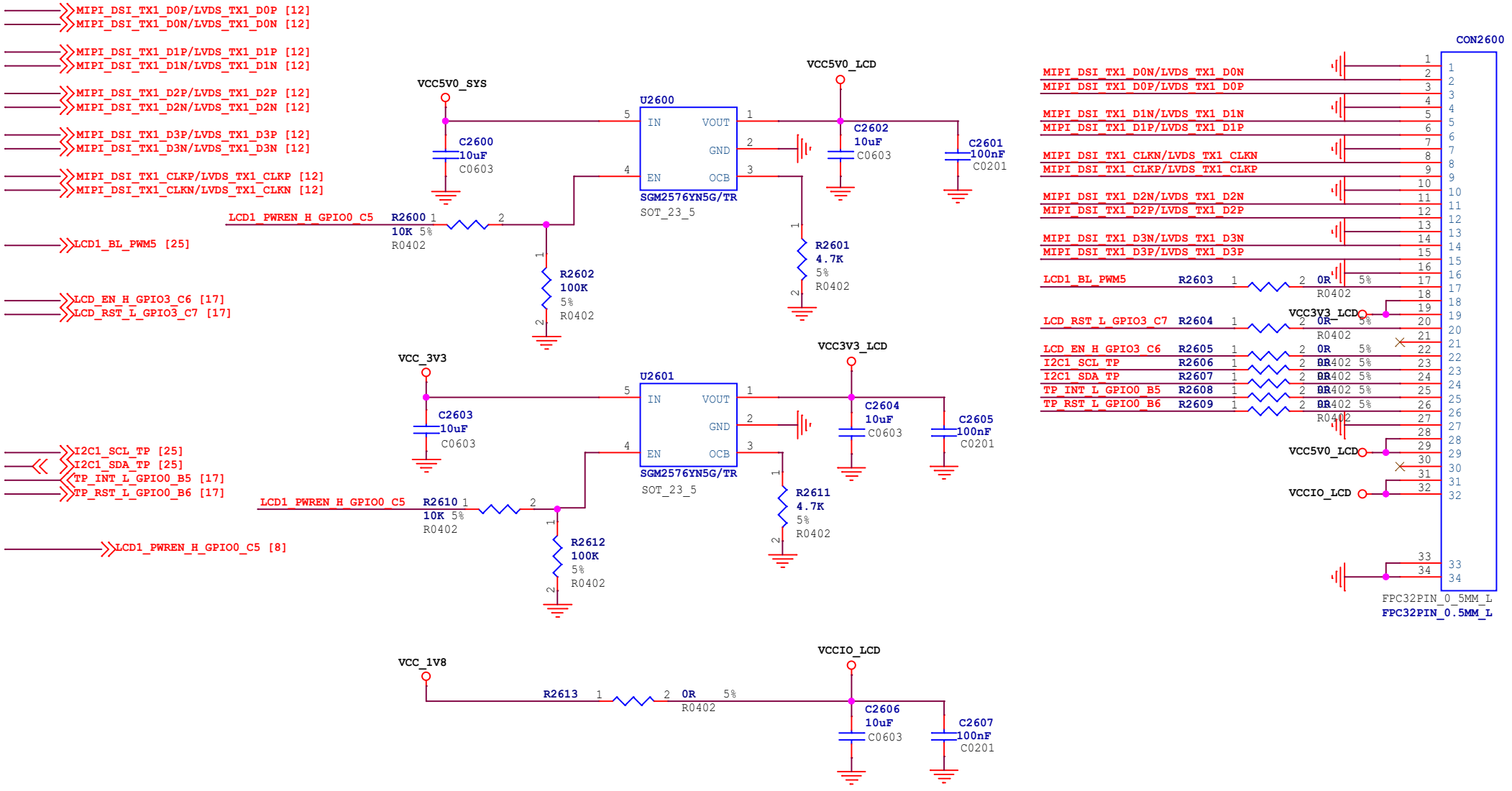






armsom https://www.armsom.org/					
Project:	ArmSoM-Sige3				
File:	25.VI-Camera_MIPI_CSI_1x 4Lanes				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	25 of 35

Single- MIPI1 LCM



armsom	https://www.armsom.org/				
Project:	ArmSoM-Sige3				
File:	26.VO-LCM_MIPI_DSI				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	26 of 35

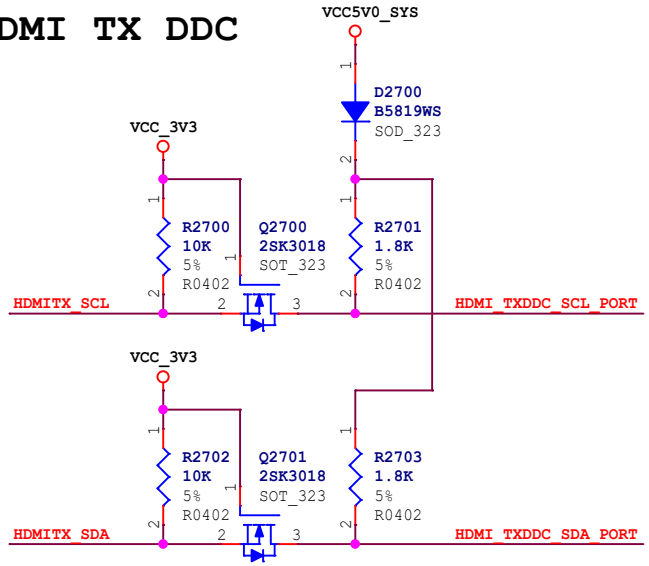
HDMI2.0 TX

HDMI_TX2P_PORT [12]
HDMI_TX2N_PORT [12]
HDMI_TX1P_PORT [12]
HDMI_TX1N_PORT [12]
HDMI_TX0P_PORT [12]
HDMI_TX0N_PORT [12]
HDMI_TXCLKP_PORT [12]
HDMI_TXCLKN_PORT [12]

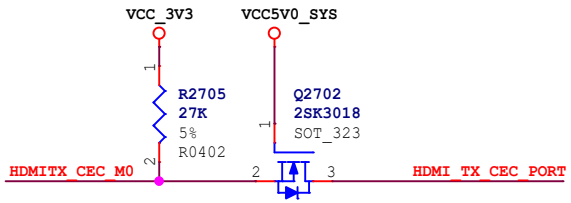
HDMITX_SCL [18]
HDMITX_SDA [18]

HDMITX_CEC_M0 [18]
HDMI_TX_HPDIN [12]

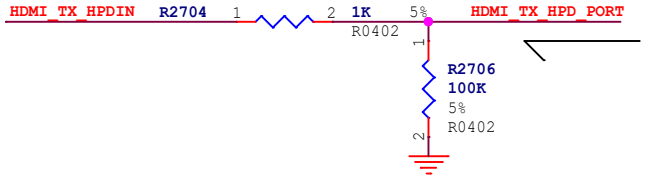
HDMI TX DDC

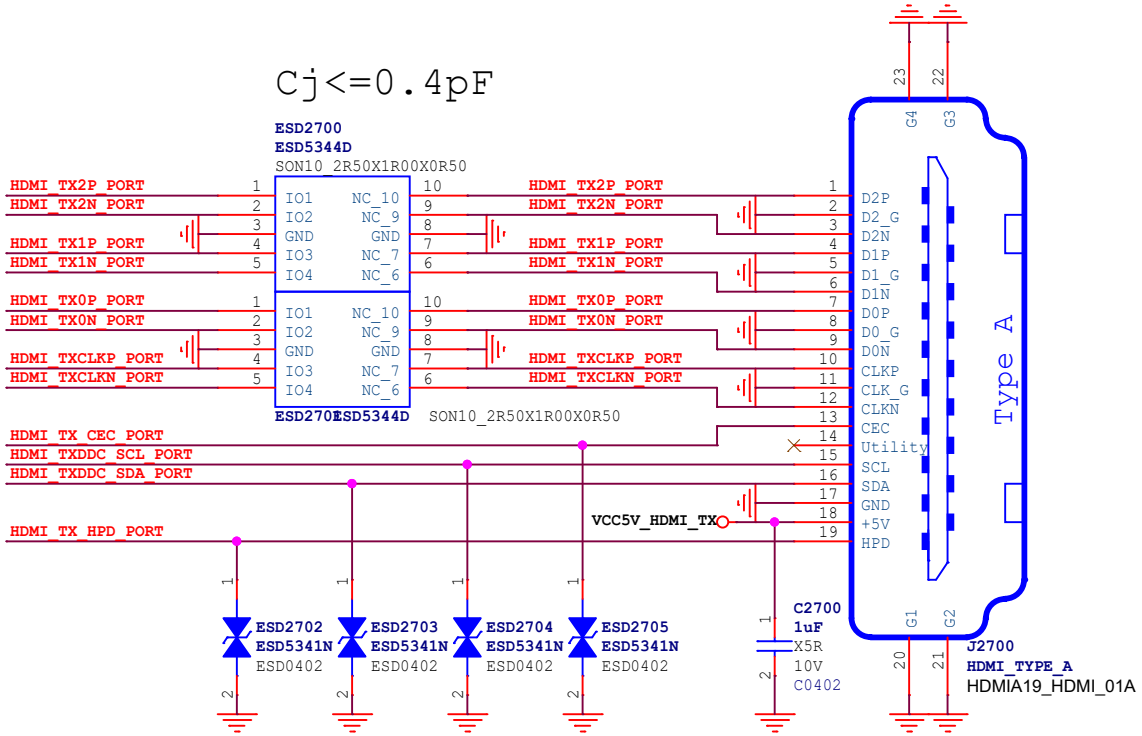


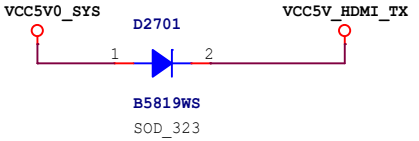
HDMI TX CEC



HDMI TX HPD

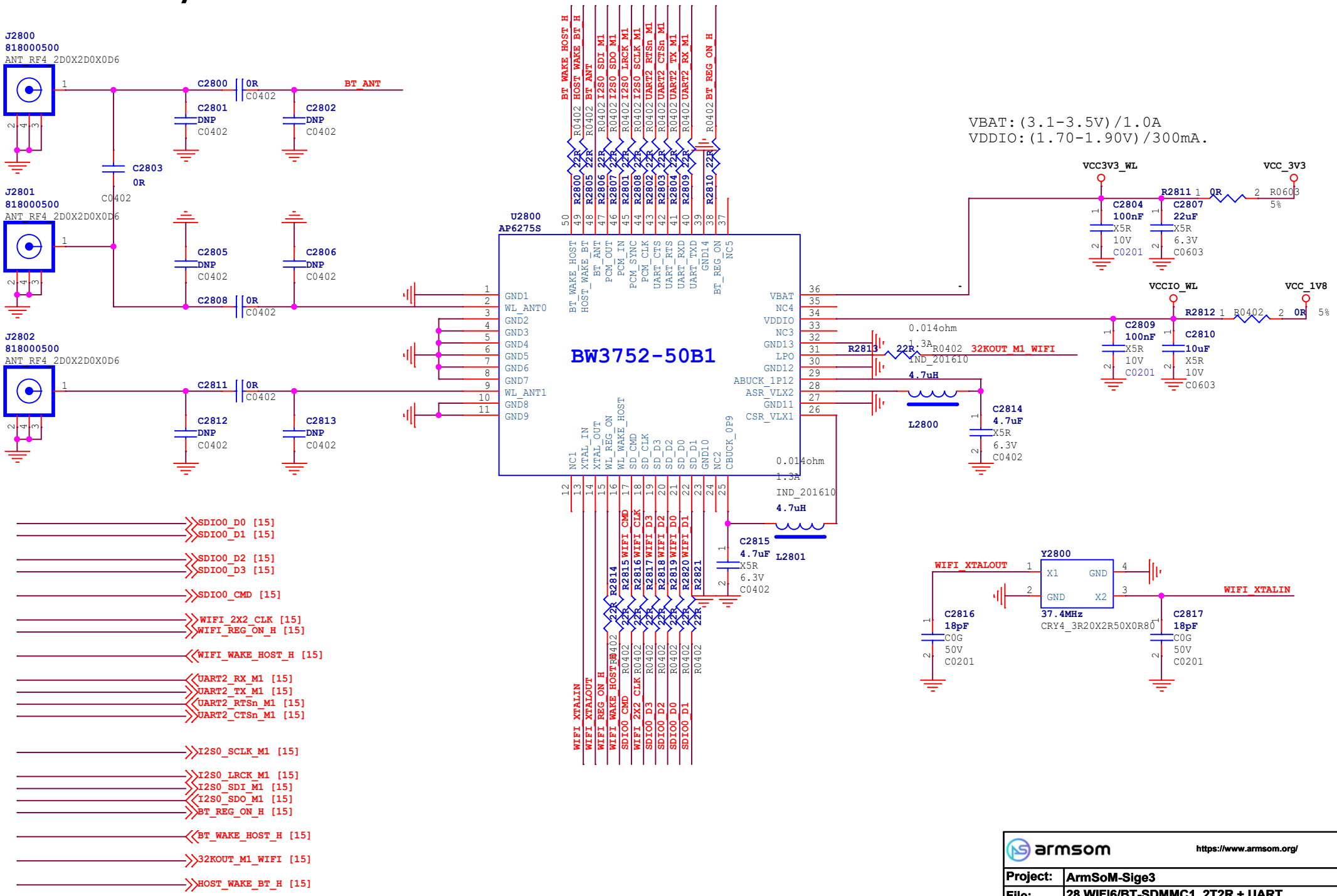






armsom	https://www.armsom.org/				
Project:	ArmSoM-Sige3				
File:	27.VO-HDMI2.0 TX				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	27 of 35

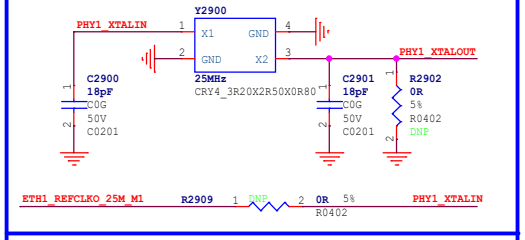
SDIO WIFI6/BT Module-2T2R

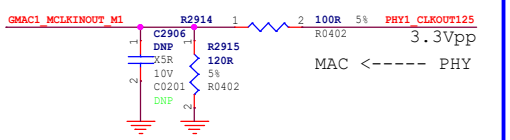


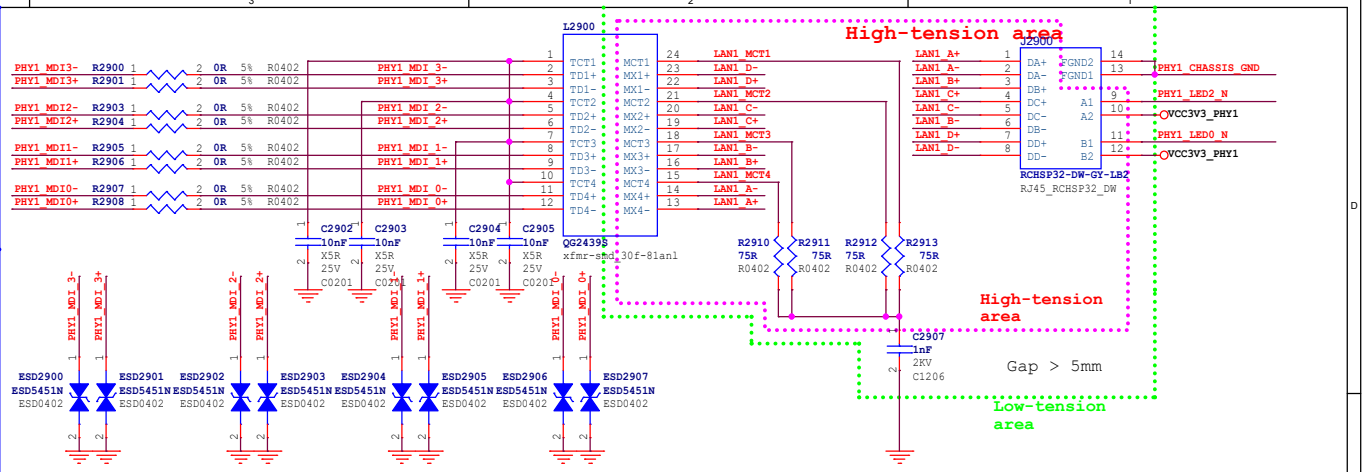
armsom	https://www.armsom.org/				
Project:	ArmSoM-Sige3				
File:	28.WIFI6/BT-SDMMC1_2T2R + UART				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	28 of 35

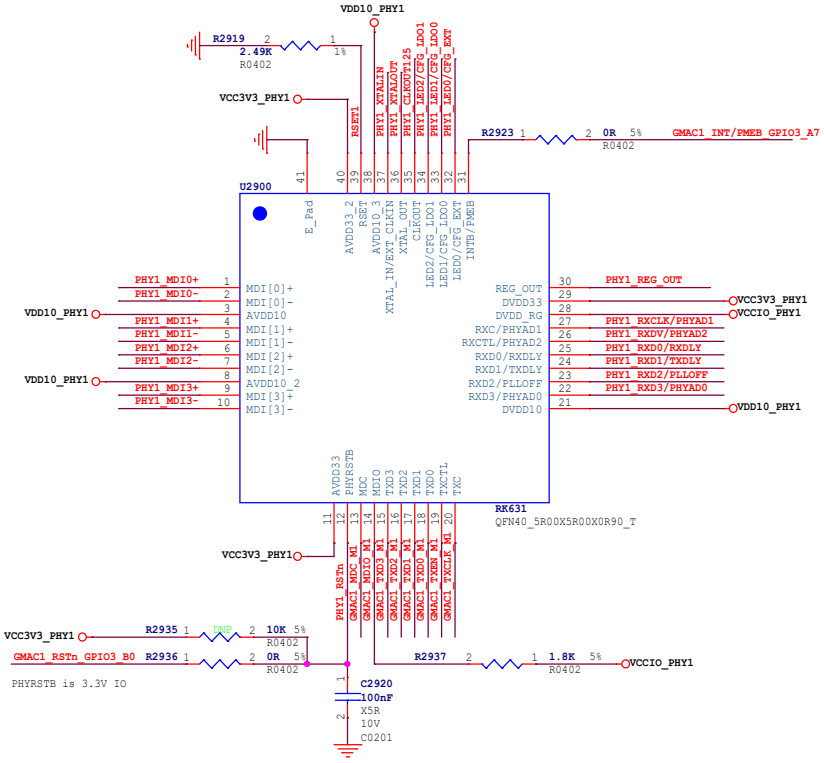
Giga PHY1

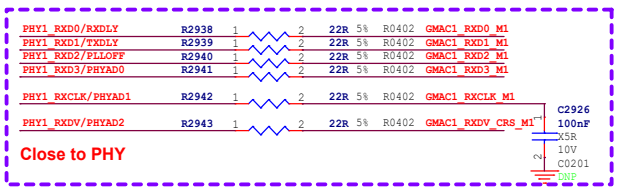
GMAC1_TXD0_M1 [17]
GMAC1_TXD1_M1 [17]
GMAC1_TXD2_M1 [17]
GMAC1_TXD3_M1 [17]
GMAC1_TXEN_M1 [17]
GMAC1_TXCLK_M1 [17]
GMAC1_RXD0_M1 [17]
GMAC1_RXD1_M1 [17]
GMAC1_RXD2_M1 [17]
GMAC1_RXD3_M1 [17]
GMAC1_RXDV_CRS_M1 [17]
GMAC1_RXCLK_M1 [17]
ETH1_REFCLKO_25M_M1 [17]
GMAC1_MCLKINOUT_M1 [17]
GMAC1_MDC_M1 [17]
GMAC1_MDIO_M1 [17]
GMAC1_RSTn_GPIO3_B0 [8]
GMAC1_INT/PMEB_GPIO3_A7 [17]

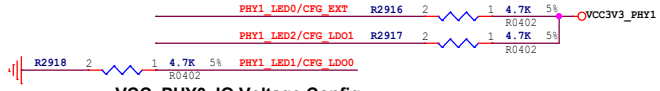


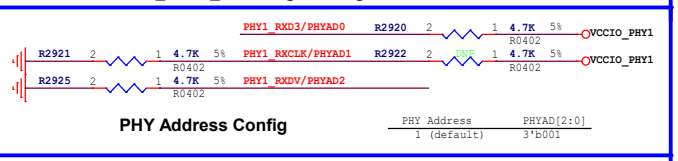


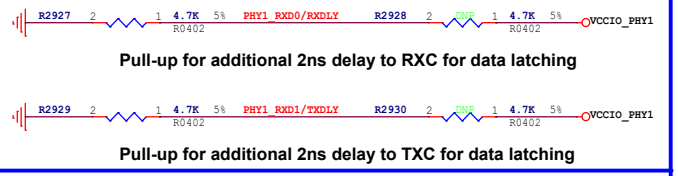


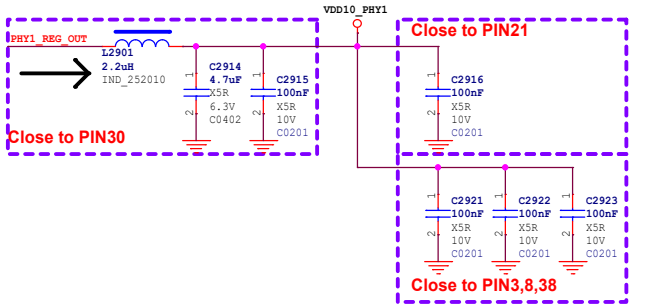




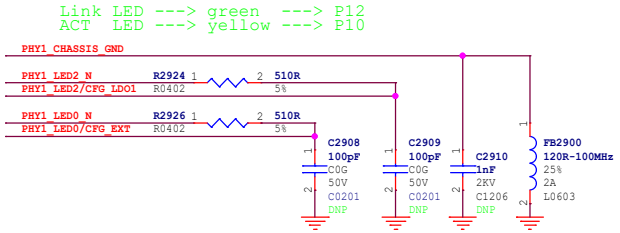




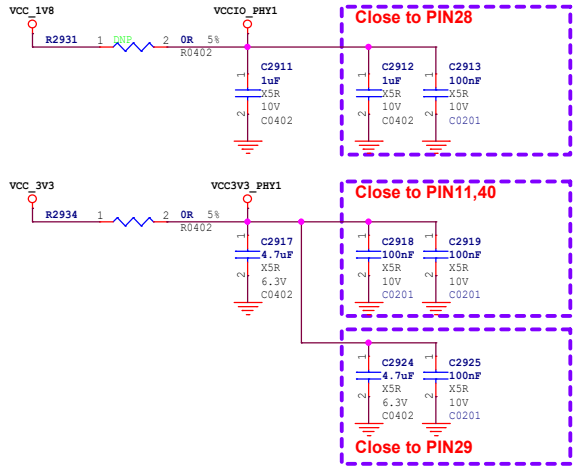




RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V	1'b1	2'b00	
External 1.8V	1'b1	2'b10	
Internal 1.8V(default)	1'b0	2'b10	



Note:
According to the actual choice of mounted Cannot be mounted at the same time



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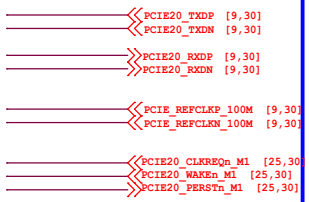
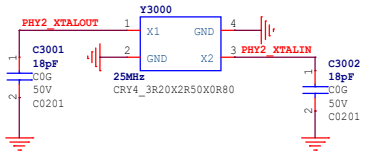
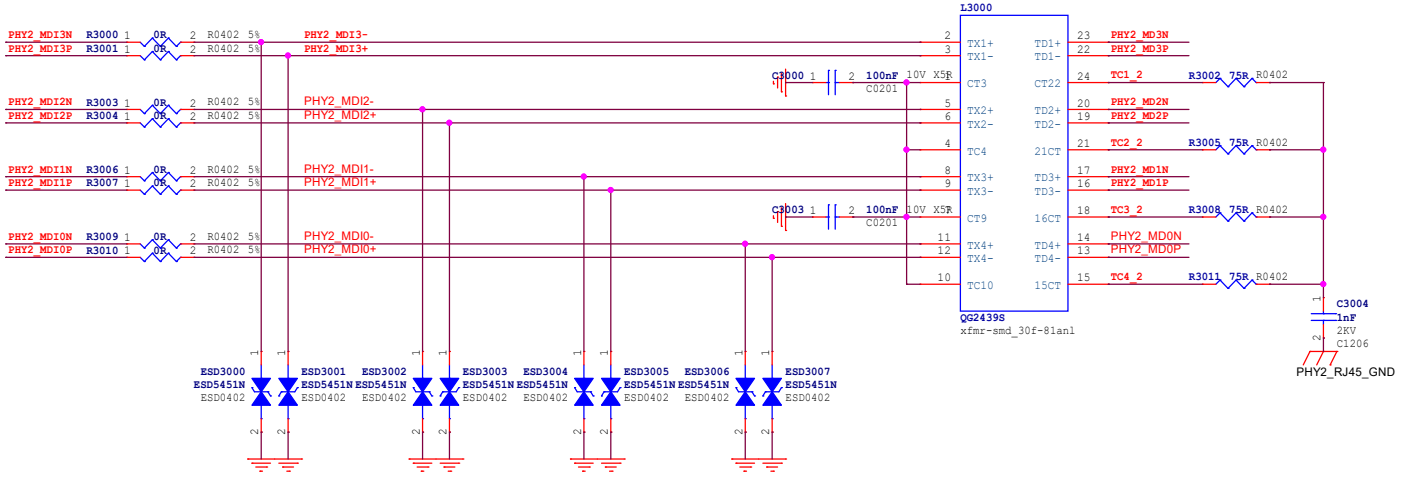
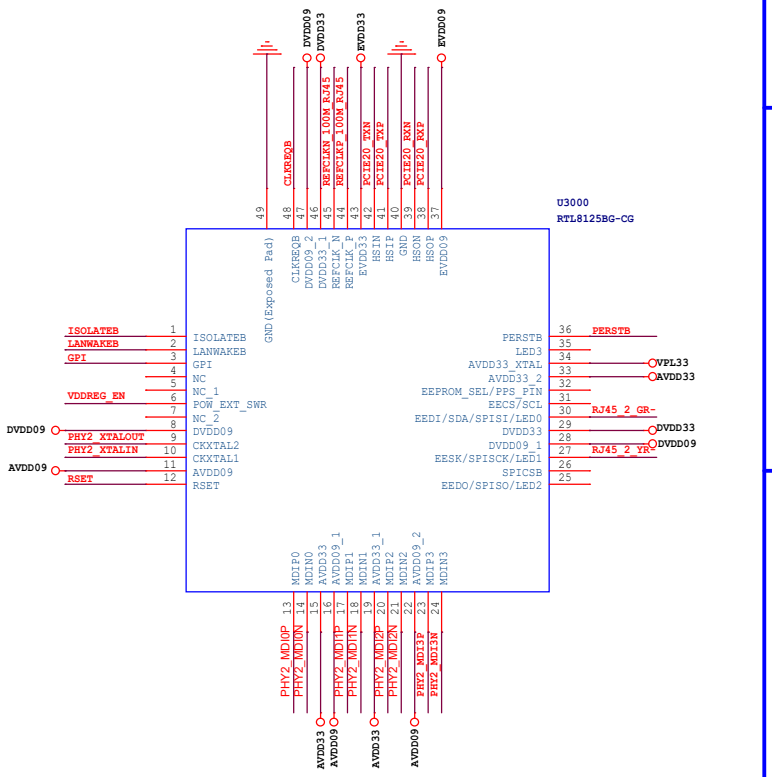
Project:	ArmSoM-Sige3				
File:	29.Ethernet-GEPHY_RGMII1				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	29 of 35

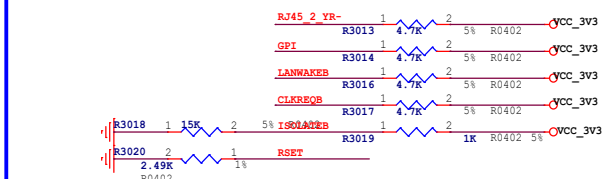
PCIE TO RJ45

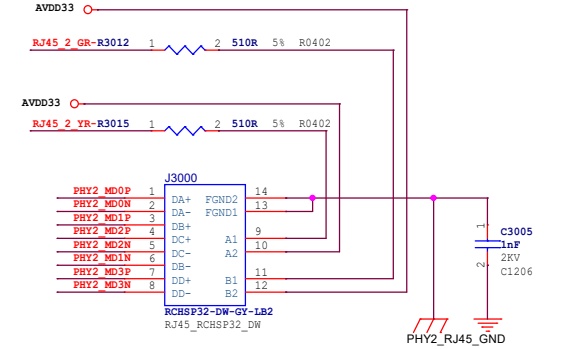


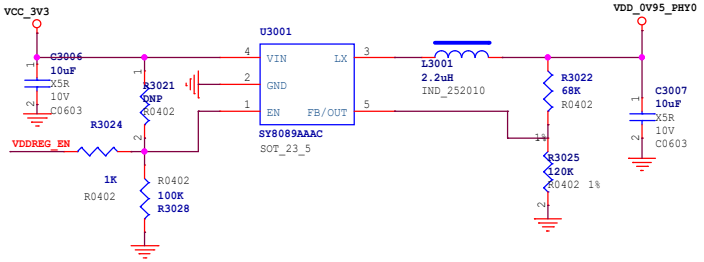


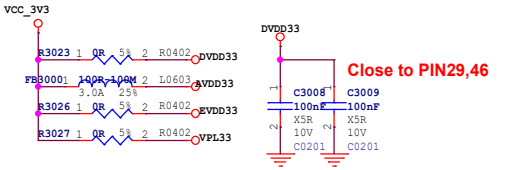


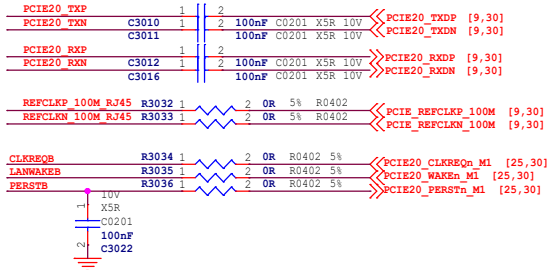


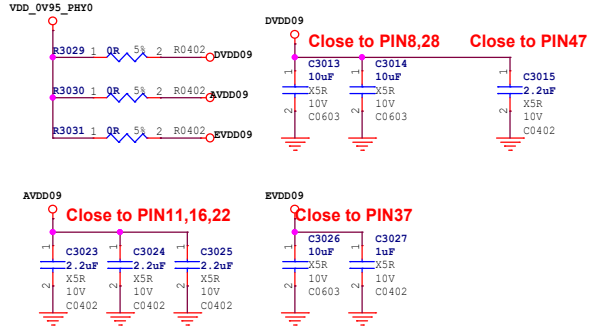


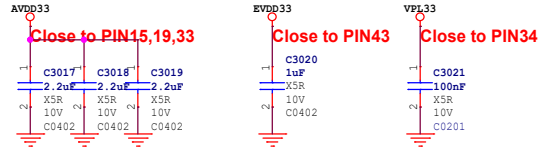




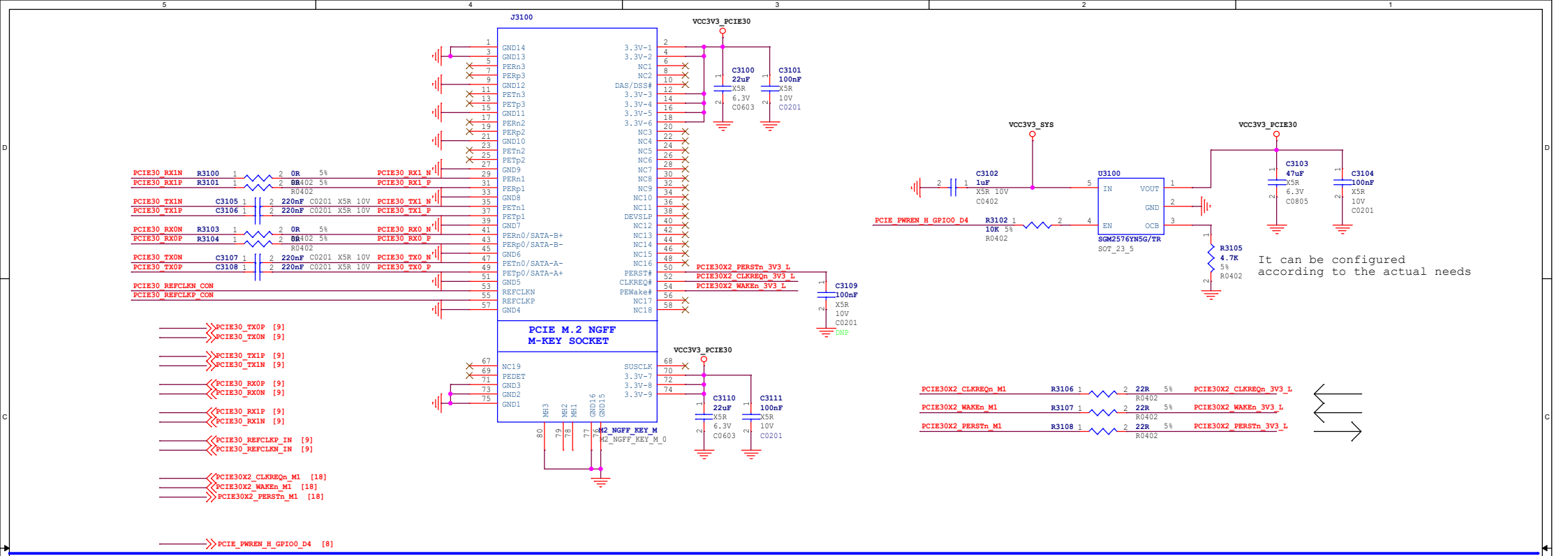


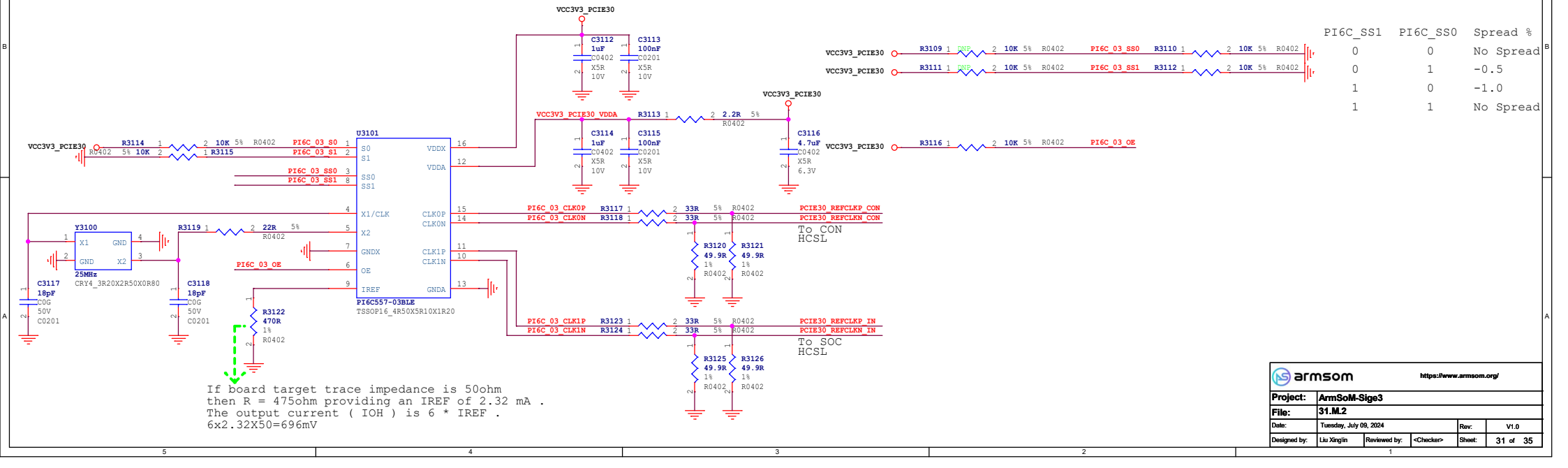






armsom	https://www.armsom.org/			
Project:	ArmSoM-Sige3			
File:	30.Ethernet-PCIE_Ethernet			
Date:	Tuesday, July 09, 2024		Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet: 30 of 35





PI6C_SS1	PI6C_SS0	Spread %
0	0	No Spread
0	1	-0.5
1	0	-1.0
1	1	No Spread

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Project:	ArmSoM-Sige3				
File:	31.M.2				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	31 of 35

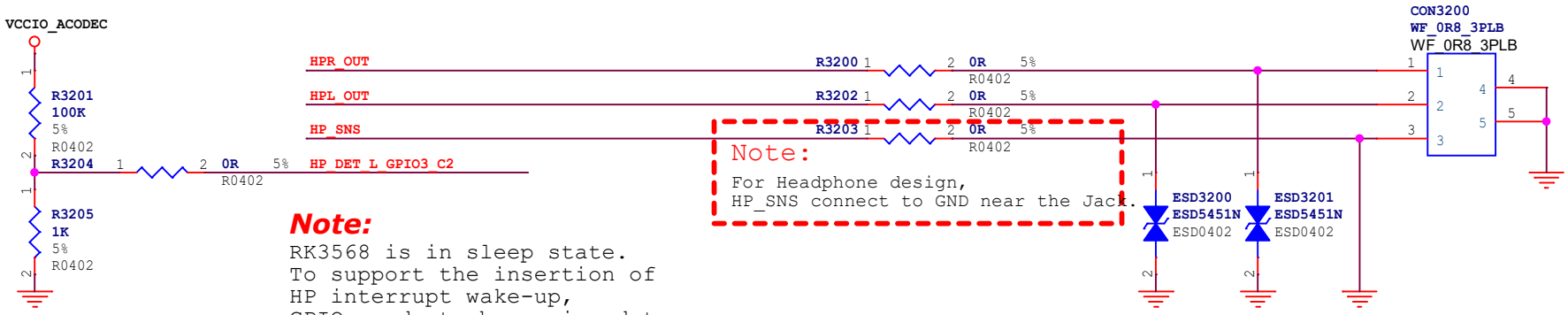
Headphone Jack

HPL_OUT [23]
HP_SNS [23]
HPR_OUT [23]
HP_DET_L_GPIO3_C2 [13]
SPKN_OUT [23]
SPKP_OUT [23]
MIC1_INP [23]
MIC1_INN [23]
SPKN_OUT — 1MM T1 T3200
SPKP_OUT — 1MM T1 T3201

GND
HPR_OUT
HP_SNS
HPL_OUT
GND

Layout note:

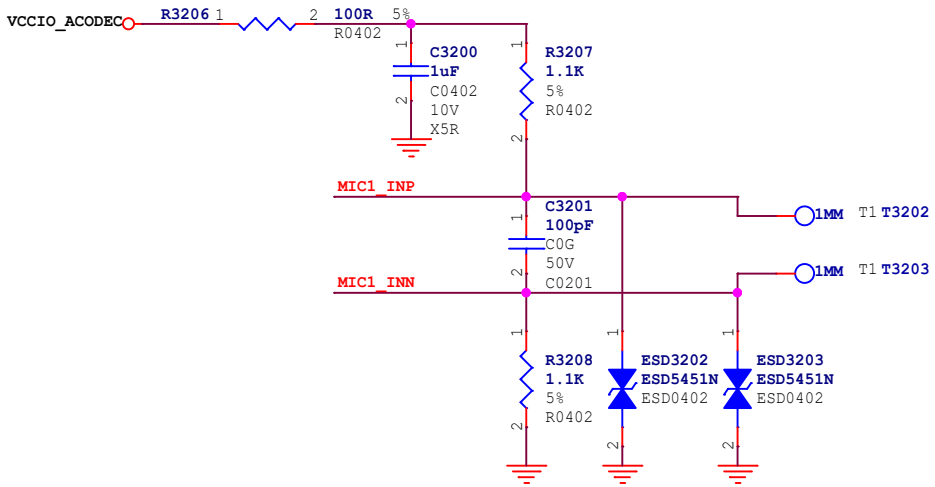
Place 0ohm resister close to GND pin
of Headphone Jack ,
at layout,HP_SNS walks in the middle
of HPL/HPR and acts as an accompanying
line to avoid interference.



Note:

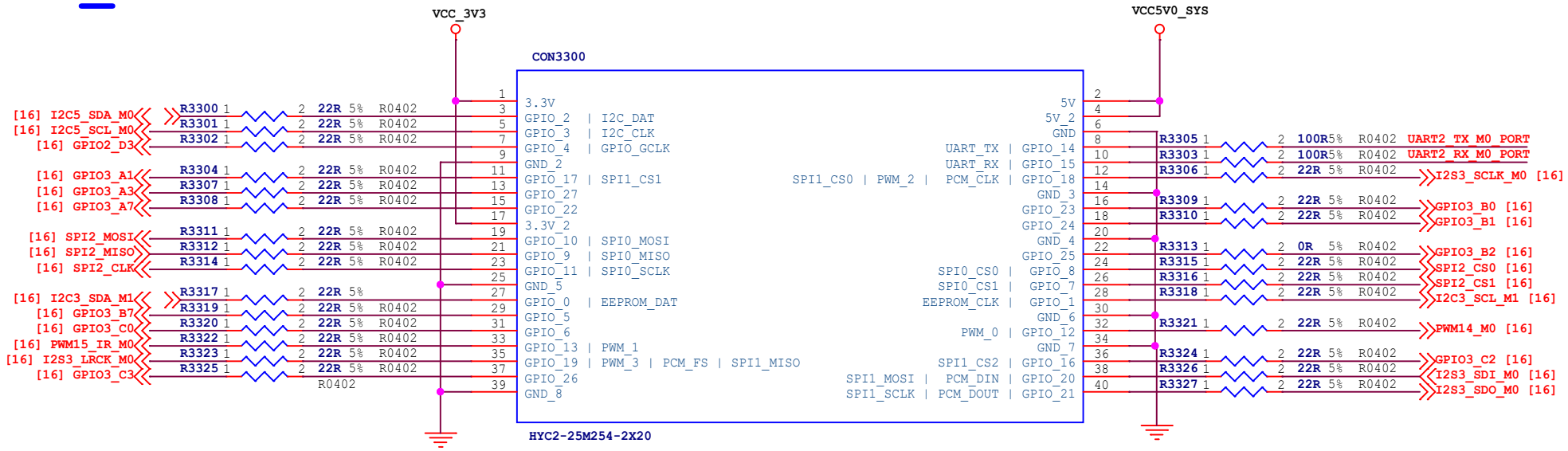
RK3568 is in sleep state.
To support the insertion of
HP interrupt wake-up,
GPIO needs to be assigned to
PMUIO0 or PMUIO1 or PMUIO2 domain

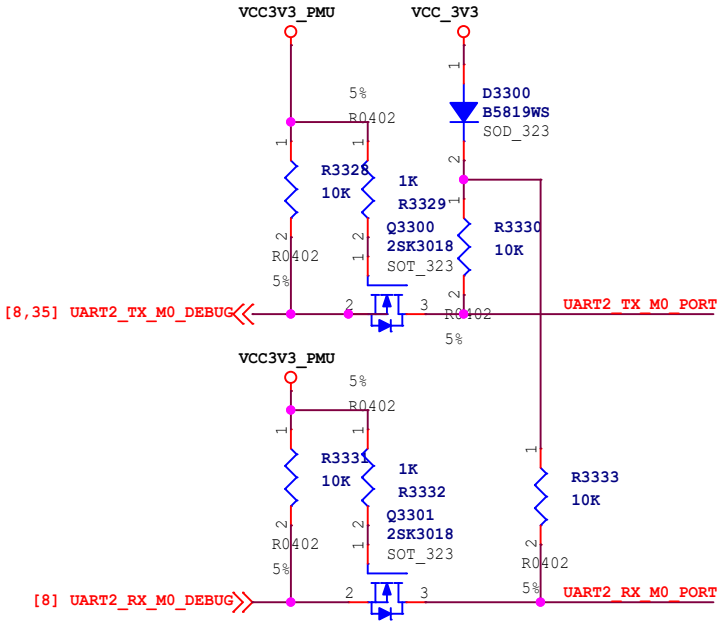
MIC

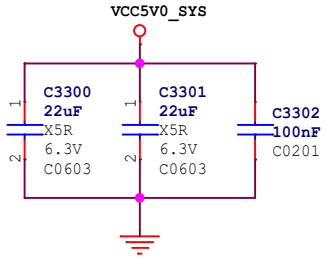


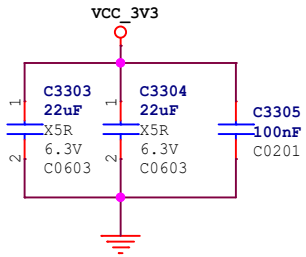
armsom	https://www.armsom.org/				
Project:	ArmSoM-Sige3				
File:	32.Audio-Headphone Port				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	32 of 35

40PIN_GPIO







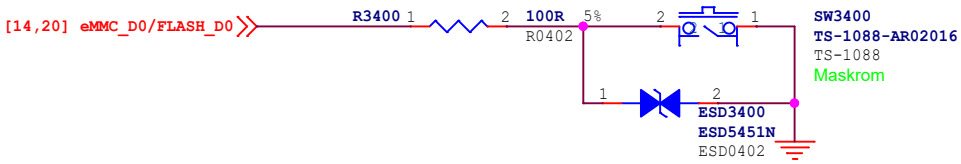


armsom	https://www.armsom.org/				
Project:	ArmSoM-Sige3				
File:	33.40PIN				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	33 of 35

Maskrom

Note:

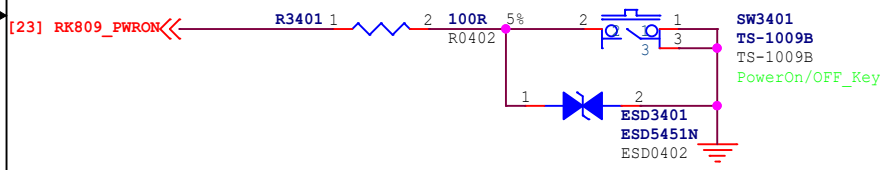
For eMMC or Nand Flash:
If eMMC_D0/FLASH_D0=0V at after power on and reset,
then system will enter into Maskrom mode.



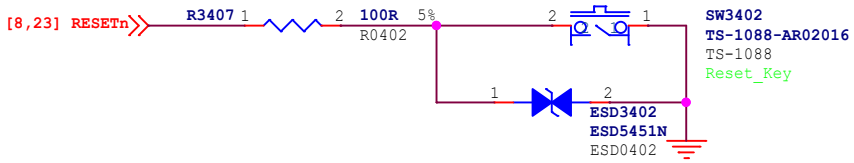
Layout note:

eMMC_D0/FLASH_D0 Key must be placed on the line, and no branch can be added

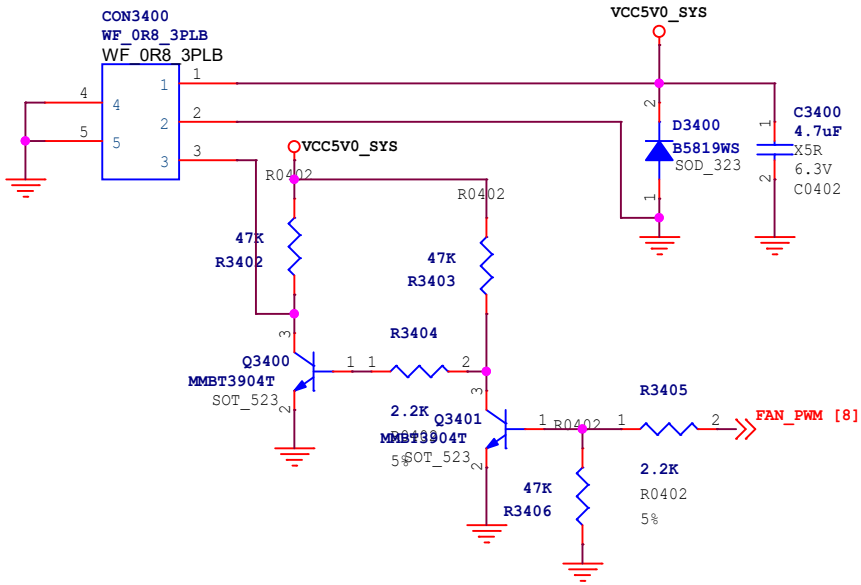
PowerOn/OFF_Key



Reset_Key



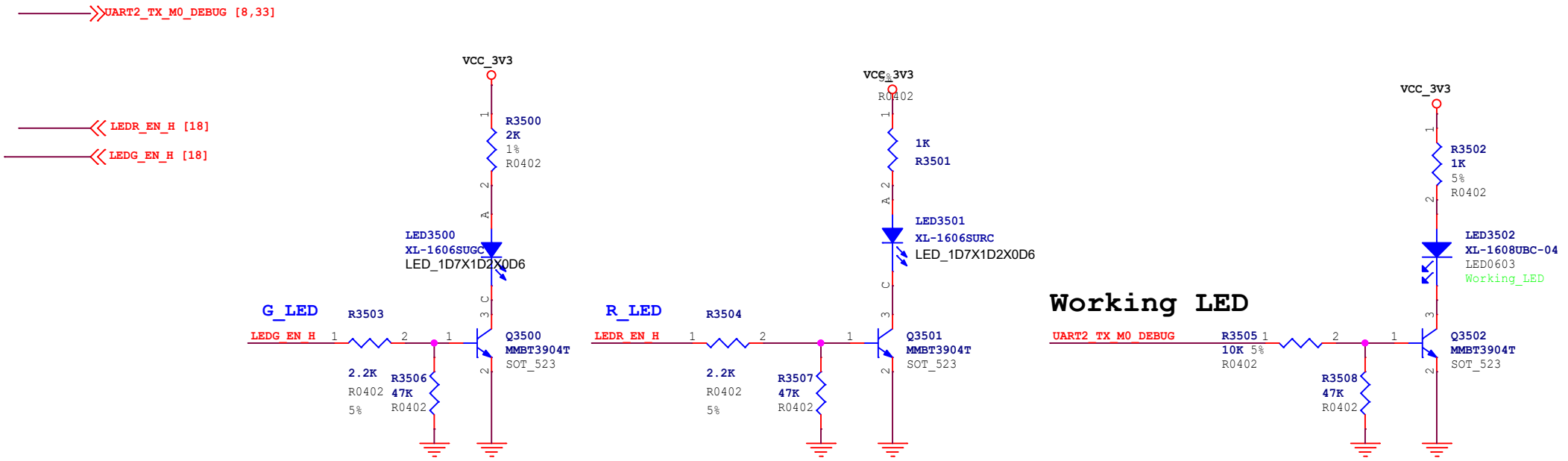
FAN



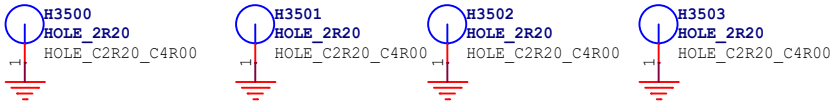
armsom https://www.armsom.org/

Project:	ArmSoM-Sige3				
File:	34.KEY Array/FAN				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	34 of 35

LED



HOLE



armsom https://www.armsom.org/

Project:	ArmSoM-Sige3				
File:	35.LED/HOLD				
Date:	Tuesday, July 09, 2024			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	35 of 35