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Rockchip RK3576 EVB1 User Guide

(Fuzhou Hardware Development Center)

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Preface

Overview

This guide mainly introduces the basic functions, hardware features, multi-function hardware configuration, and software debugging operation methods of RK3576 EVB1. It aims to help debuggers use RK3576 EVB1 be faster and more accurately, and be familiar with RK3576 chip development and application solutions.

Product version

The product versions corresponding to this document are as follows:

Product name	Product version
RK3576 EVB1	RK_EVB1_RK3576_LP4XD200P132SD6_V10_20231211YWQ_final

Intended Audience

This guide is mainly intended for:

- Hardware development engineers
- Layout engineers
- Technical support engineers
- Test engineers

Revision History

This revision history recorded description of each version, and any updates of previous versions are included in the latest one.

Version No.	Author	Revision Date	Revision Description	Remark
V1.0	LZX	2024-05	Initial release	

Abbreviation

缩略语包括文档中常用词组的简称。

缩略词	英文描述	中文描述
RK/Rockchip	Rockchip Electronics Co.,Ltd.	瑞芯微电子股份有限公司
ADB	Android Debug Bridge	安卓调试桥
CPU	Central Processing Unit	中央处理器
NPU	Neural Network Processing Unit	神经网络处理器
GPU	Graphics Processing Unit	图像处理器
DDR	Double Data Rate	双倍速率同步动态随机存储器
UFS	Universal Flash Storage	通用闪存存储
eMMC	Embedded Multi Media Card	内嵌式多媒体存储卡
DP	DisplayPort	视频接口
eDP	Embedded DisplayPort	嵌入式数码音视讯传输接口
HDMI	High Definition Multimedia Interface	高清晰度多媒体接口
RGB	Red,Green,Blue ; RGB color mode is a color standard in industry	红绿蓝,RGB 色彩模式, 是工业界的一种颜色标准
VGA	Video Graphics Array	电脑显示视频图像标准接口
MIPI	Mobile Industry Processor Interface	移动产业处理器接口
LVDS	Low-Voltage Differential Signaling	低电压差分信号
CIF	Camera Interface	摄像头接口
USB	Universal Serial Bus	通用串行总线
SATA	Serial Advanced Technology Attachment	串行高级技术附件
PCIe	Peripheral Component Interconnect Express	外围组件快速互连
RGMII	Reduced Gigabit Media Independent Interface	精简吉比特介质独立接口
WIFI	Wireless Fidelity	无线保真
FlexBus	FlexBus	灵活的并行总线
DSMC	Double Data Rate Serial Memory Controller	双倍数据速率存储器控制接口
I2C	Inter-Integrated Circuit	内部整合电路(两线式串行通讯总线)
SAI	Serial Audio Interface	串行音频接口
SPDIF	Sony/Philips Digital Interface	索尼/飞利浦数字音频接口
CAN	Controller Area Network	控制器局域网络
SARADC	Successive Approximation Register Analog to Digital Converter	逐次逼近寄存器型模数转换器
UART	Universal Asynchronous Receiver/ Transmitter	通用异步收发传输器
JTAG	Joint Test Action Group	联合测试行为组织
PWM	Pulse Width Modulation	脉冲宽度调制
IR	Infrared Radiation	红外线
RTC	Real-time clock	实时时钟
PMIC	Power Management IC	电源管理芯片
PMU	Power Management Unit	电源管理单元
LDO	Low Drop Out Linear Regulator	低压差线性稳压器
DCDC	Direct Current to Direct Current	直流电转直流电

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1 System Introduction

1.1 RK3576 Introduction

K3576 is a high performance, low power processor for ARM-based PC and Edge Computing device, personal mobile internet device and other digital multimedia applications, and integrates quad-core Cortex-A72 and quad-core Cortex-A53 with separately NEON coprocessor.

RK3576 video decoder supports H.265, VP9, AV1 and AVS2 etc. up to 4K@120fps and H.264 up to 4k@60fps, and video encoder supports H.264 and H.265 up to 4k@60fps, high-quality JPEG encoder/decoder supports up to 4k@60fps.

Embedded 3D GPU makes RK3576 completely compatible with OpenGL ES 1.1/2.0/3.2, OpenCL 2.0 and Vulkan 1.1. Dedicated 2D hardware engine with MMU will maximize display performance and provide very smoothly operation.

RK3576 introduces a new generation 16-Megapixel ISP(Image Signal Processor). It implements a lot of algorithm accelerators, such as HDR, 3A, CAC, 3DNR, 2DNR, Sharpening, Dehaze, Enhance, Debayer, Small Angle Lens-Distortion Correction and so on.

The build-in NPU supports INT4/INT8/INT16/FP16/BF16/TF32 hybrid operation, with a computing power of up to 6 TOPS. In addition, with its strong compatibility, network models based on a series of frameworks such as TensorFlow/MXNet/PyTorch/Caffe can be easily converted.

RK3576 supports high-performance dual channel external memory interface(LPDDR4/LPDDR4X/LPDDR5) capable of sustaining demanding memory bandwidths, also provides a complete set of peripheral interface to support very flexible applications.

1.2 RK3576 Chip Block Diagram

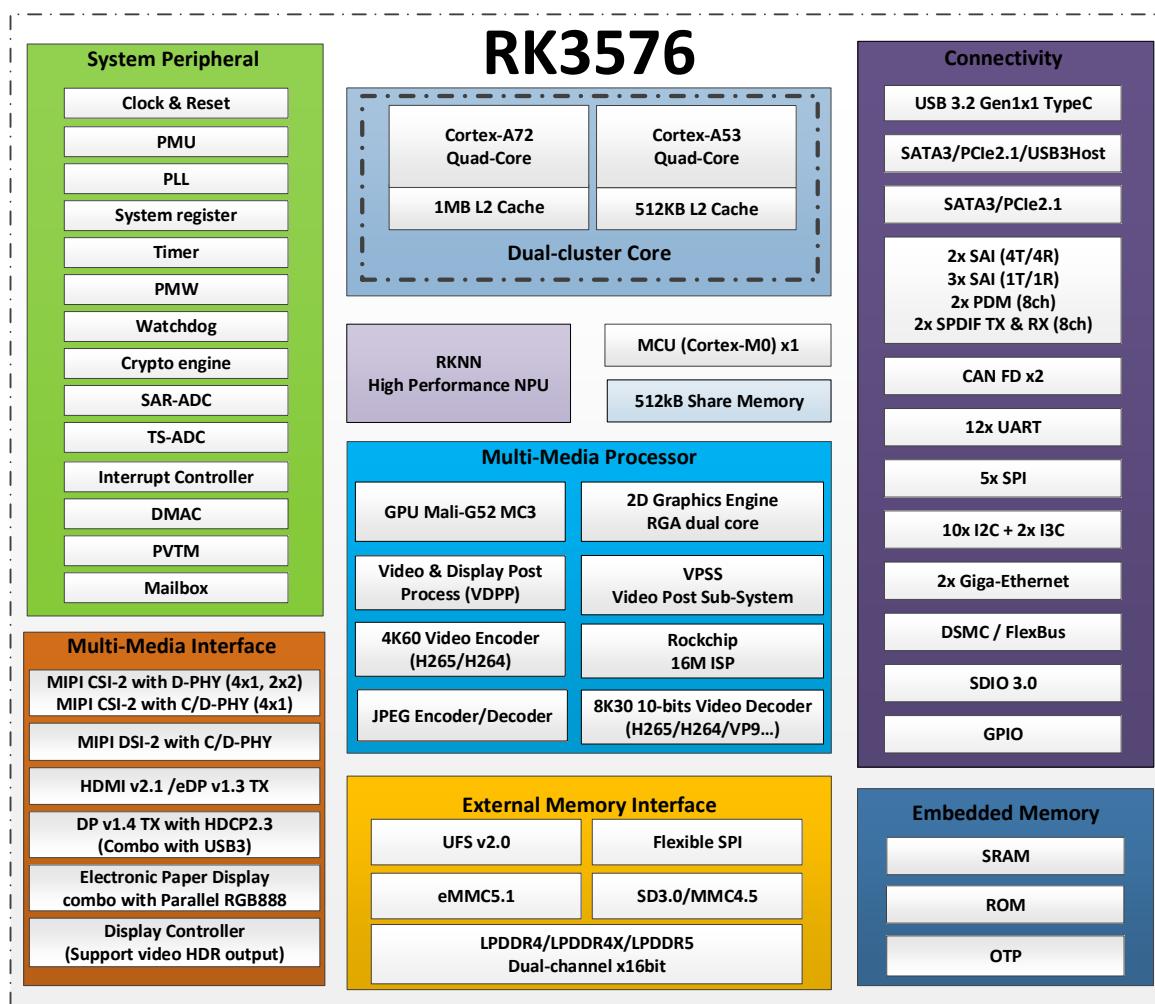


Figure 1-1 RK3588 Chip Block Diagram

1.3 System Framework

1.3.1 System Block Diagram

The RK3576 EVB1 system utilizes the RK3576 chip, RK806S-5 power management chip, along with a power supply scheme consisting of peripheral BUCK and LDO components. The memory options include LPDDR4x, UFS, eMMC (not soldered by default, with compatibility for SPI Flash design). The system features MIPI DCPHY CSI RX, MIPI DPHY CSI RX, MIPI DPHY DSI TX, PCIe 2.1, HDMI 2.1 TX, Gigabit Ethernet port, Micro SD Card 3.0, USB Type-C with DP Alt Mode, UART debug, Wi-Fi/BT expansion interface, and more. It integrates a stable and mass-producible solution. Please refer to the detailed system diagram below:

RK3576 Ref Block Diagram(Typical Application Case)

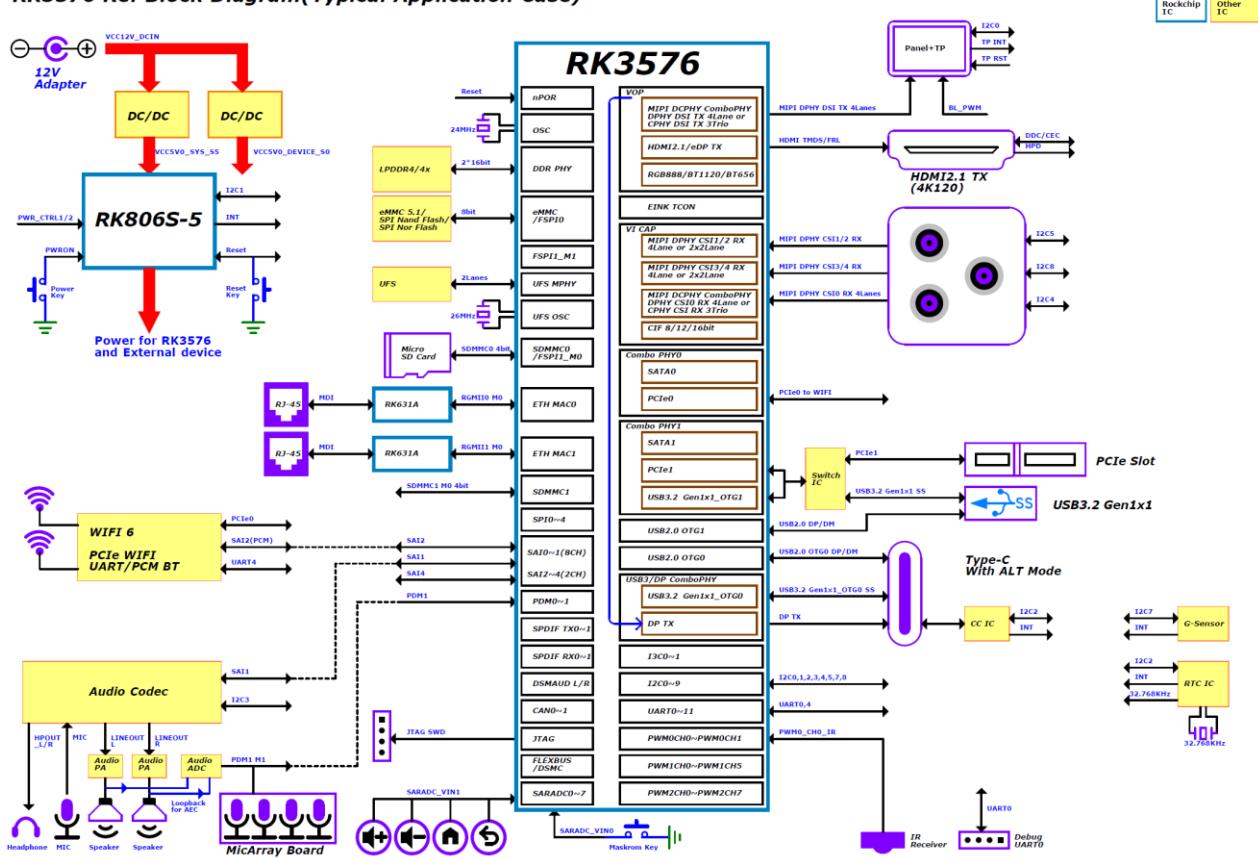


Figure 1-2 RK3576 EVB1 system diagram

1.3.2 Function Summary

RK3576 EVB1 includes the following functions:

- DC Power: DC 12V adapter power supply interface
 - TYPEC: One complete TYPEC interface, compatible with system firmware upgrade channel and DP1.4 output interface
 - USB Host: one-way USB3.2 Gen1x1 Host standard-A interface
 - HDMI2.1 TX: one-way HDMI2.1 TX standard-A interface, single channel supports up to 4K@120Hz output
 - Ethernet: Support two channels RJ45 ports 10/100/1000M Ethernet;
 - PCIe2.1 Slot: A standard PCIe x4 gold finger interface; supports RC function for expanding PCIe devices (Option with USB3.0 Host).
 - MIPI DCPHY CSI RX: One 4-lane DPHY or one 3-trios MIPI CPHY signal input, connected via an 80-pin connector. It can be used with the IMX415 monocular board of the matching EVB to enable photo and video shooting function.
 - MIPI DPHY CSI RX: Two 4-lane DPHY signal inputs, both support splitting into 2x2 lanes; connected via an 80-pin connector. It can be used with the IMX415 monocular board of the matching EVB to enable photo and video shooting function.
 - MIPI DPHY DSI TX: One 4-lane MIPI signal output, connected to the EVB's matching MIPI screen via an FPC cable.

- SD Flash: Supports Micro SD Card 3.0.
- Audio interface: With onboard Codec, it can support 1 headphone + 2 speakers + 1 analog microphone. In addition, it has an array microphone expansion connector, which can be modified with resistors to support an 8-microphone expansion solution.
- IR: Supports infrared interface.
- Gyroscope + G-sensor: Supports 3-axis gyroscope and 3-axis accelerometer.
- JTAG: Supports system JTAG debugging interface (Option with SD Card).
- CAN: Supports one CAN interface (Option with SD Card).
- UART Debug: Used for user debugging and viewing LOG information; adopts a Type-C connector.
- System Key: Includes RESET, MASKROM, POWER, Volume+/RECOVERY, Volume-, MENU, and ESC buttons.

1.3.3 Function Interface

Table 1-1 PCB Functional Interface Introduction Table

Function	usable or not
LPDDR4x	8GB
UFS	128GB
eMMC	N/A
TYPEC with Alt Mode	1 Port
MIPI DPHY DSI TX	1 Port
HDMI2.1 TX	1 Port
千兆网口 10M/100M/1000M	2 Port
MIPI DCPHY CSI RX	1x4Lane or 1x3trios
MIPI DPHY CSI RX	2x4Lane
PCIe2.1 Slot	1 Lane, (Option with USB3.0 Host))
USB3.2 Gen1x1 Host (1 Port)	1Port
WI-FI/BT	1 x a/b/g/n/ac/ax 2T2R PCIe WIFI6+UART/PCM BT
Audio Interface	1 x Headphone+2 x SPK+1 x Analog MIC MIC Array connecter
IR	YES
Sensor	1 x Gyroscope/G-sensor
UART Debug	YES
System Key	YES
Maskrom Key	YES
JTAG	YES

1.3.4 Function Module Distribution

RK3576 EVB1 functional interface distribution diagram:

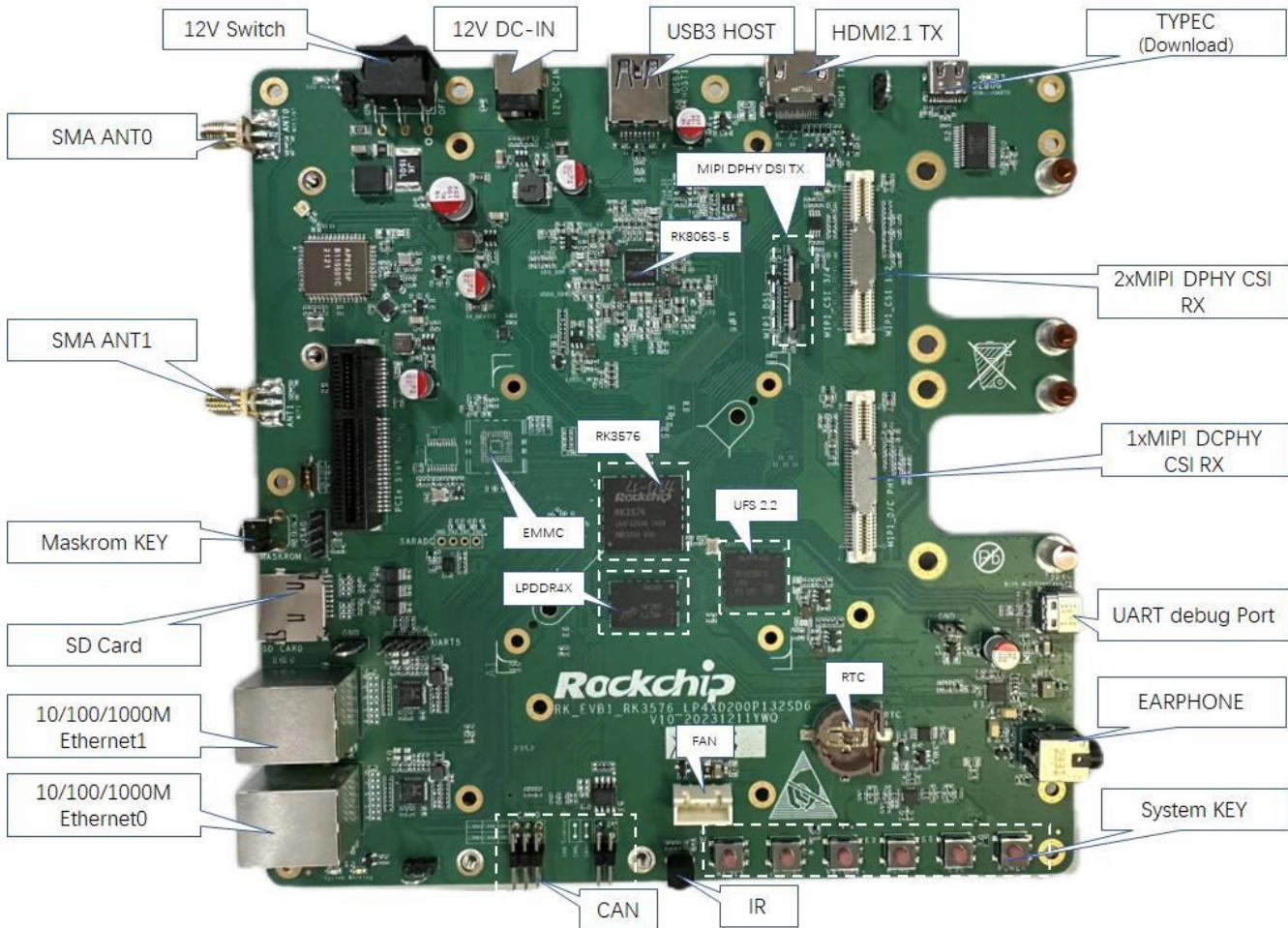


Figure 1-3 RK3576 EVB1 Functional Interface Distribution Diagram (front)

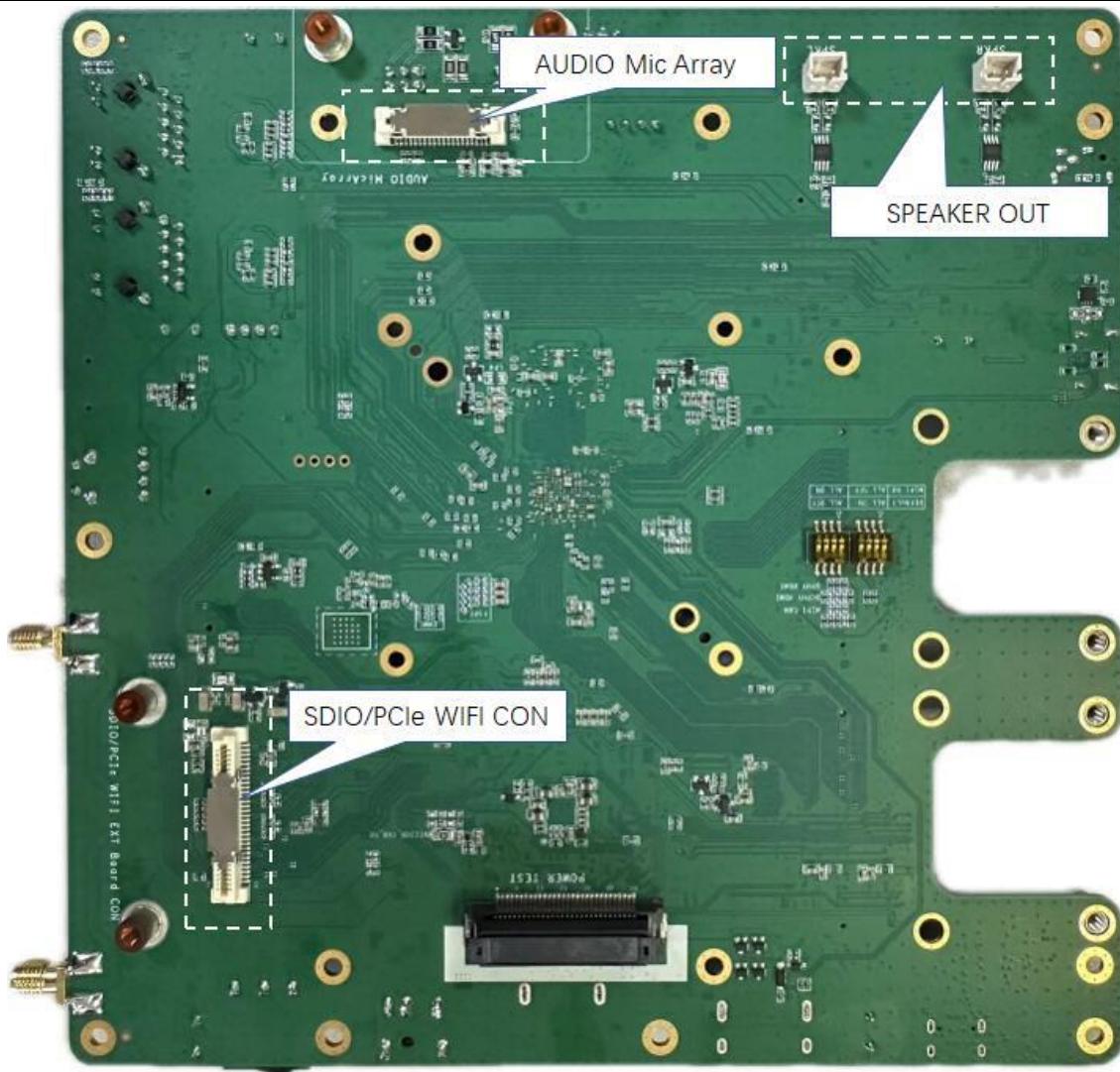


Figure 1-4 RK3576 EVB1 Functional Interface Distribution Diagram (back)

1.4 Modules

The RK3576 EVB1 kit includes the following items:

- RK3576 EVB1
- Power adapter, default specification: input 100V AC~240V AC, 50Hz; output 12V DC, 3A
- Display, specification: MIPI; size: 5.5 inches/vertical screen; resolution: 1080*1920
- two 2.4G/5G dual-band SMA female connector antennas
- IMX415 monocular camera module

1.5 Power on and off and Standby

The EVB1 power on, power off and standby methods are introduced as follows:

- Power on: Use DC 12V power supply, turn on the main power switch; wait to enter the Android interface, it means that the default firmware has been successfully started.
- Power off: When simultaneously pressing the Volume+ and POWER buttons for more than 500ms, the system

interface will display the POWER-OFF and RESTART options. Clicking on the POWER-OFF option will shut down the device. Alternatively, long-pressing the POWER button for 6 seconds will forcibly shut down the system.

- Standby: Press the power button, the system will enter the first-level standby state. When there is no USB OTG connection, and there is no other operation (such as key operation), and the software does not have a Wake_Lock source. After about 3s, it will switch from the first-level standby to the second-level standby state. Standby mode can be launched through the Power button.

1.6 Firmware Upgrade

1.6.1 USB Drive Installation

The driver needs to be installed before the EVB driver is upgraded. The following describes the driver installation process under Windows system.

Find DriverAssitant_v5.13 in the provided tool folder, and click DriverInstall.exe to pop up the following interface. Click "Install Driver" and wait for the prompt to install the driver successfully. If the old driver has been installed, please click "Uninstall Driver" and reinstall the driver.

名称	修改日期	类型	大小
ADBDriver	2020/11/10 14:13	文件夹	
bin	2020/11/10 14:14	文件夹	
Driver	2023/11/9 11:09	文件夹	
config.ini	2014/6/3 15:38	配置设置	1 KB
DriverInstall.exe	2023/11/9 11:06	应用程序	491 KB
Readme.txt	2018/1/31 17:44	文本文档	1 KB
revision.log	2023/11/9 11:08	文本文档	1 KB

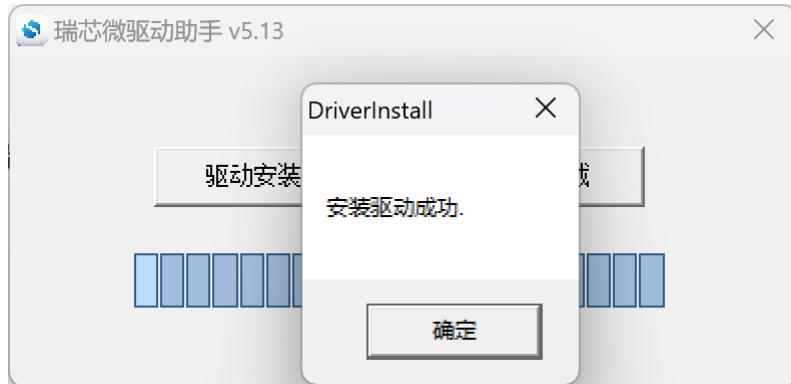


Figure 1-5 Successful Driver Installation

1.6.2 Firmware Upgrade Method

There are two ways to upgrade RK3576 EVB1 firmware:

- To enter the MASKROM upgrade mode, follow these steps:

Before the system is powered on, SARADC_IN0 needs to be kept low, and the system will enter the MASKROM state.

- (1) Connect the TYPEC port to the PC end and hold down the MASKROM button
- (2) The EVB1 powered by 12V with DCIN and turn on the power switch.
- (3) When the burning tool (version 3.28 or above) detects a MASKROM device, release the MASKROM button. In the rectangular area of the tool's interface, right-click and select "Import Configuration." Then, locate the firmware path and choose the config.cfg file.
- (4) Select the corresponding Loader, Parameter, Uboot, and other files in the burning tool.

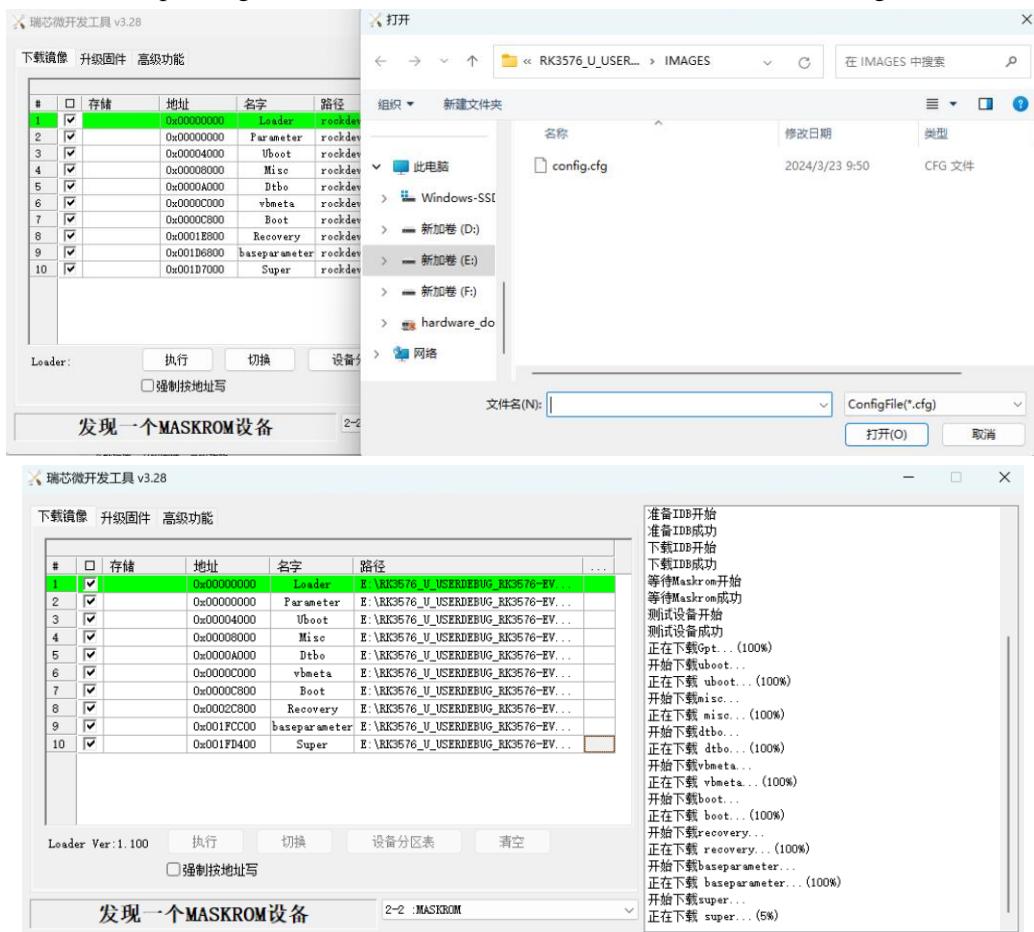


Figure 1-6 Entering MASKROM Programming Mode

- To enter the Loader upgrade mode, follow these steps:

Before powering on the system, keep SARADC_IN1 low.

- (1) connect the EVB1 device to the PC end and hold down the Volume+ (RECOVERY) button.
- (2) The EVB1 powered by 12V with DCIN and turn on the power switch.
- (3) If the device is already powered on, press and release the reset button.
- (4) When the burning tool (version 3.28 or above) detects a Loader device, release the RECOVERY button. In the rectangular area of the tool's interface, right-click and select "Import Configuration." Then, locate the firmware path and choose the config file.
- (5) Select the corresponding Loader, Parameter, Uboot, and other files in the burning tool.
- (6) Click "Execute" to enter the upgrade mode. The tool's right side will display a progress bar, showing the

download progress and verification status.

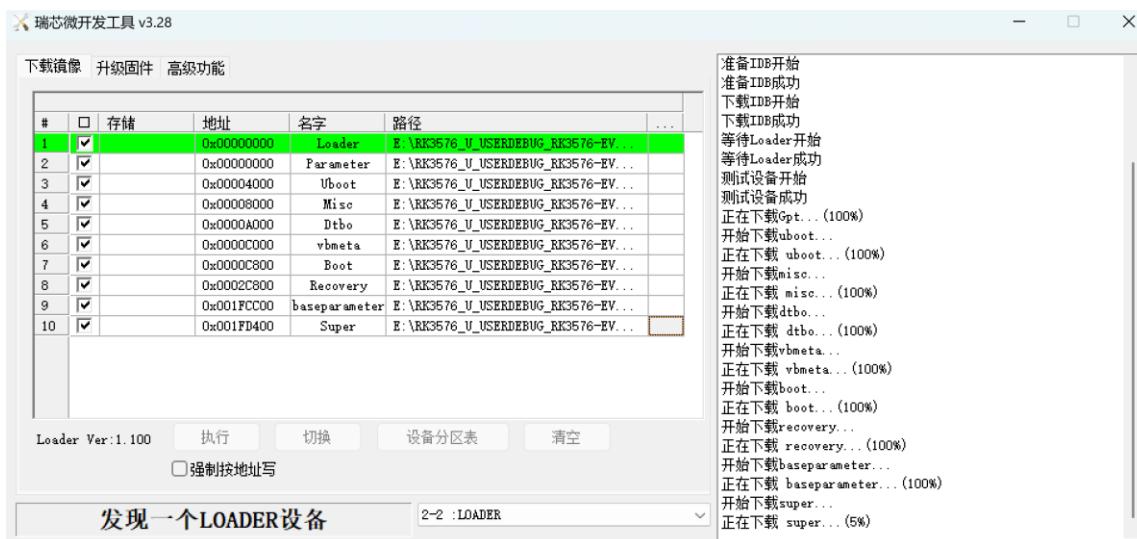


Figure 1-7 Entering Loader Programming Mode

- USB3 upgrade method

When using Rockchip development tool version v3.28 or higher, after configuring "USB3_TRANSFER=TRUE" in the "config.ini" file, the firmware upgrade process will automatically switch modes based on whether the device supports USB 3.2 GEN1 transfer functionality.

名称	修改日期	类型	大小
bin	2017/9/11 15:07	文件夹	
Language	2017/9/11 15:07	文件夹	
Log	2024/3/25 15:09	文件夹	
config.ini	2023/12/25 17:23	配置设置	3 KB
revision.txt	2024/2/27 17:06	文本文档	4 KB
RKDevTool.exe	2024/2/27 17:12	应用程序	2,914 KB
开发工具使用文档_v1.0.pdf	2021/8/27 10:28	Adobe Acrobat 文档	450 KB

Figure 1-8 location of the config.ini file

```

FW_NOT_CHECK=TRUE
#当设置RB_CHECK_OFF=FALSE时,固件升级时才进行回读校验
RB_CHECK_OFF=
#LBA_PARITY=TRUE时,设备端开启写后校验
LBA_PARITY=
#NorFlash单个IDBlock
NOR_SINGLE_IDB=
#USB3_TRANSFER=TRUE时,设备端如果支持USB3传输, 工具会采用USB3模式进行下载
USB3_TRANSFER=TRUE
#当设置CLOSE_CHECK_IDB=TRUE时,不检查IDBLOCK是否会被覆盖
CLOSE_CHECK_IDB=
#自动保存配置
AUTO=true

```

Figure 1-9 modifying configuration

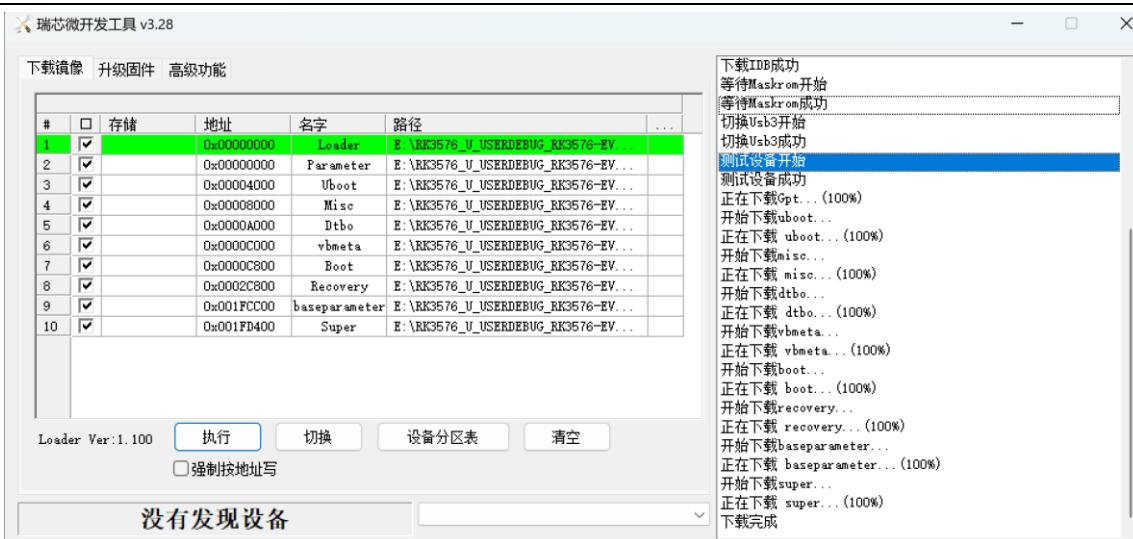


Figure 1-10 displaying USB3 in the download tool,

1.7 Debugging

1.7.1 Serial Port Tool

Connect EVB1 USB-UART Debug port to PC end, and get the port COM number from the device manager in the PC end.

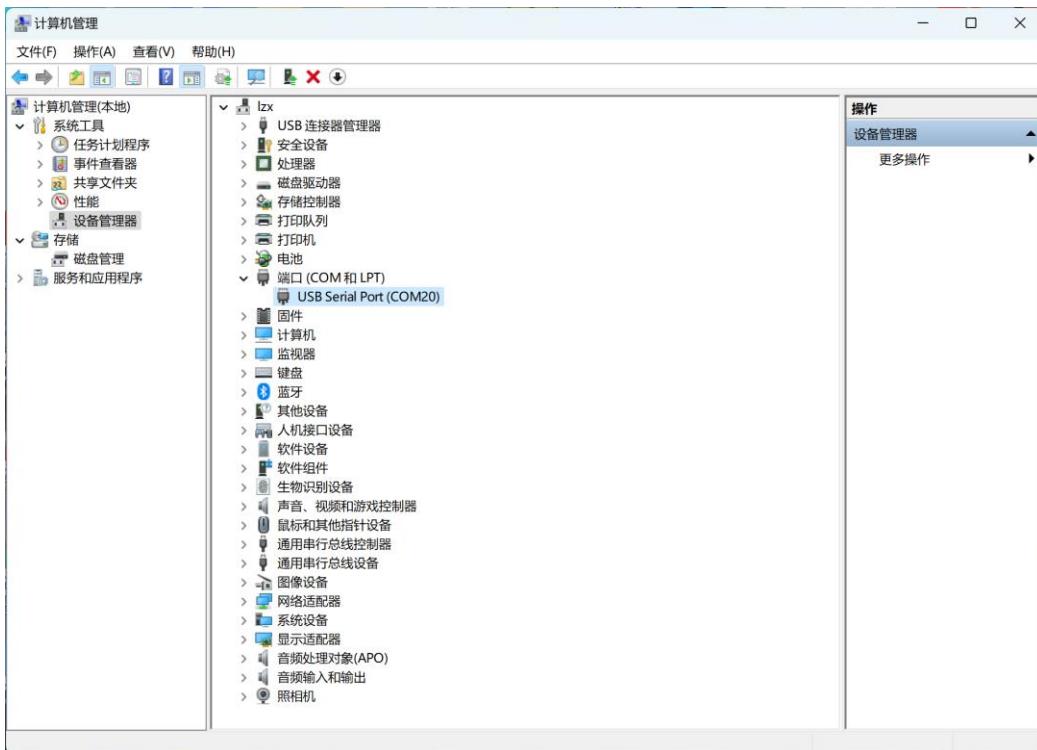


Figure 1-11 Get the Current Port COM Number

Open the serial port tool, under the “Session” interface, first select the serial port, then set the Serial line to the corresponding COM number, and change the speed to 1.5M(RK3576 supports 1.5M baud rate by default), finally, click the “Open” to enter the serial port debugging interface.

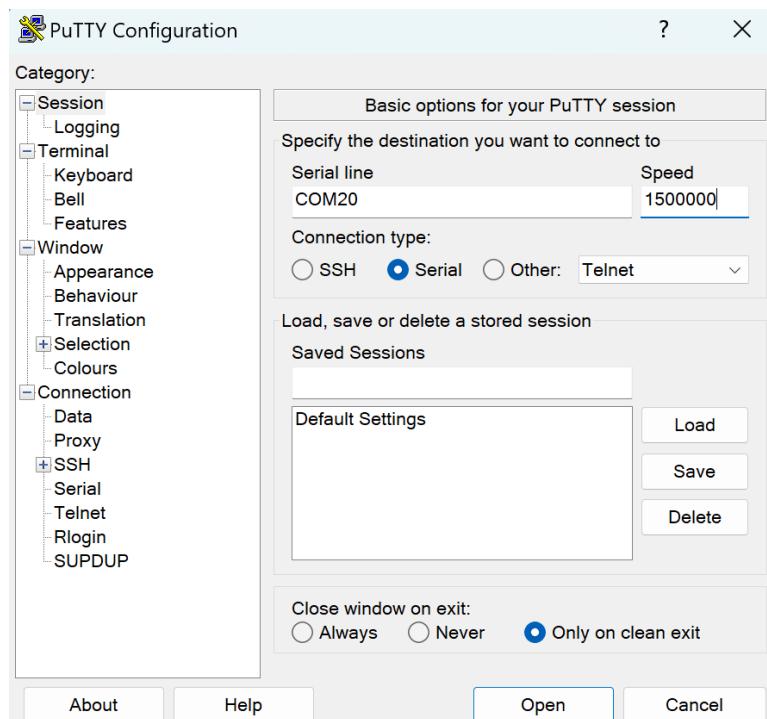


Figure 1-12 Serial Port Tool Configuration

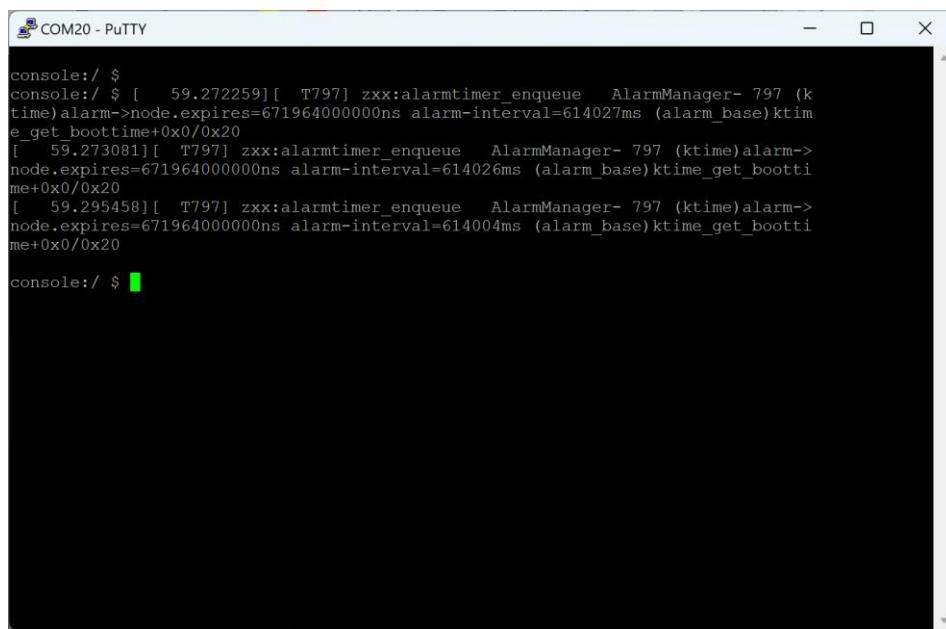


Figure 1-13 Serial Port Tool Debug Interface

1.7.2 Adb Debug

- 1) Ensure that the driver is installed successfully, and the PC is connected to the TYPE_C port above the power supply of the development board;
- 2) Power on the development board and boot into the system;
- 3) Open the adb tool on the PC side;
- 4) Type "adb shell" to enter adb debugging.

```
D:\RK_Soft\ADB\cmdr
λ adb devices
List of devices attached
249016592df6a7c2        device

D:\RK_Soft\ADB\cmdr
λ adb shell
rk3576_u:/ $ |
```

Figure 1-14 adb debugging

2 Hardware Introduction

2.1 The Pictures



Figure 2-1 RK3576 EVB1 picture

2.2 Power Block Diagram

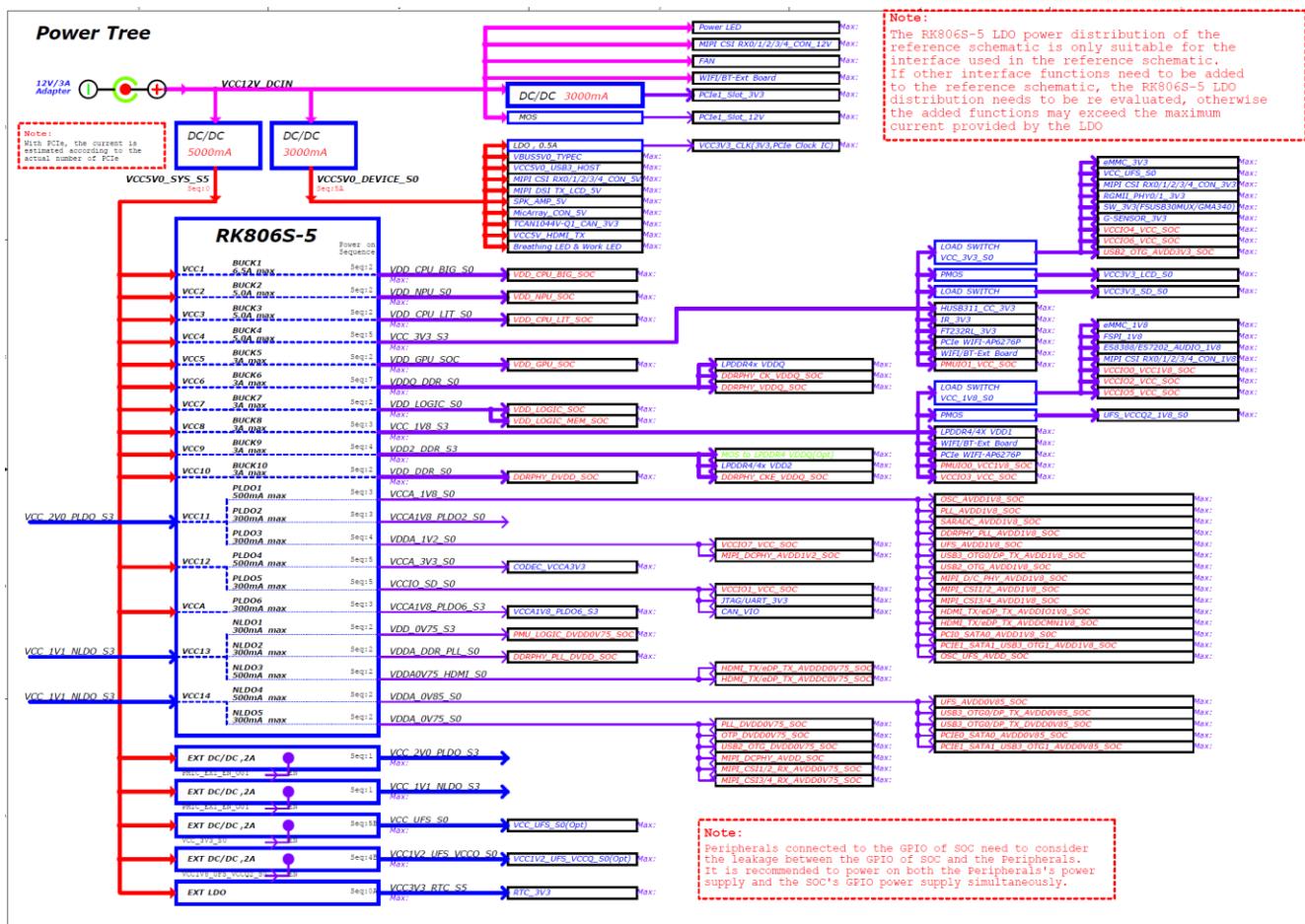


Figure 2-2 RK3576 power supply diagram

2.3 I2C Address

The development board reserves a wealth of peripheral interfaces. The user debugging I2C peripherals will involve I2C channel multiplexing. Table 2-1 shows the I2C address and level values corresponding to the existing development board devices.

Table 2-1 Correspondence Table of Peripheral Address and IO Level Value

I2C channel	Device	I2C address	Power domain
I2C0_M1	TP (Touch Panel)	TBD	3.3V
I2C1_M0	RK806S-5	0x23	1.8V
I2C2_M0	HYM8563TS(RTC)	0x51	3.3V
I2C2_M0	HUSB311(CC IC)	0x4E	3.3V
I2C3_M0	ES8388	0x11	1.8V
I2C3_M0	ES7202	0x30	1.8V
I2C3_M0	MicArray	TBD	1.8V
I2C4_M3	CAM0	0x1A	1.8V
I2C4_M3	CAM4	TBD	1.8V

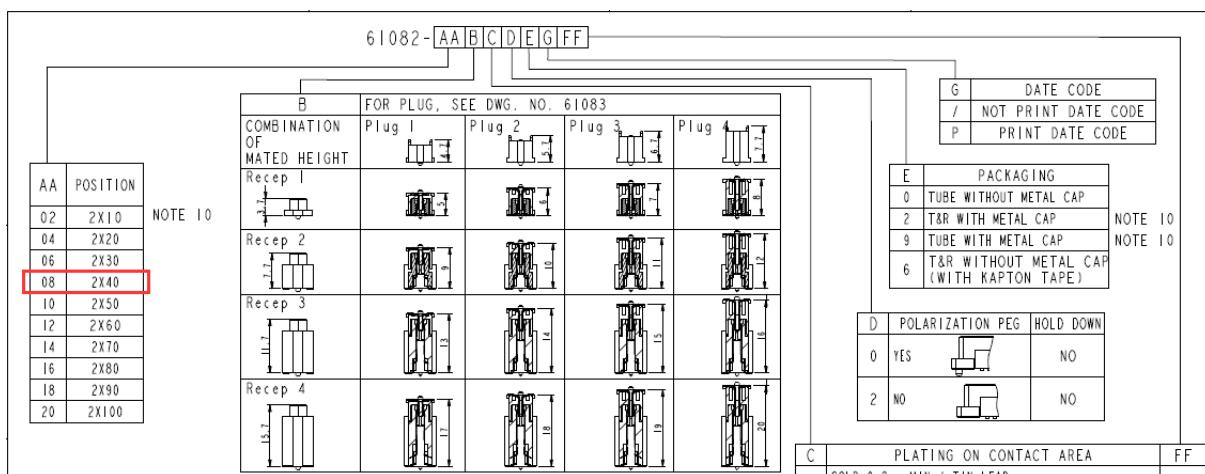
I2C channel	Device	I2C address	Power domain
I2C5_M3	CAM1	TBD	1.8V
I2C6_M3	CAM2	TBD	1.8V
I2C7_M1	ICM-42607-C	0x68	3.3V
I2C8_M2	CAM3	TBD	3.3V
HDMI_TX_I2C	HDMI TX	TBD	3.3V

Note: When using the expansion board, make sure that the I2C address on the board does not conflict with the I2C address on the EVB board.

2.4 MIPI DCPHY CSI RX Extension Connector Information

In actual use, the user may make an expansion board. The model of the development board connector is as follows:

CON4600 and CON4700 are vertical double-row 80PIN card sockets with 0.3mm pins and 0.8mm spacing. The dimensions are as follows:



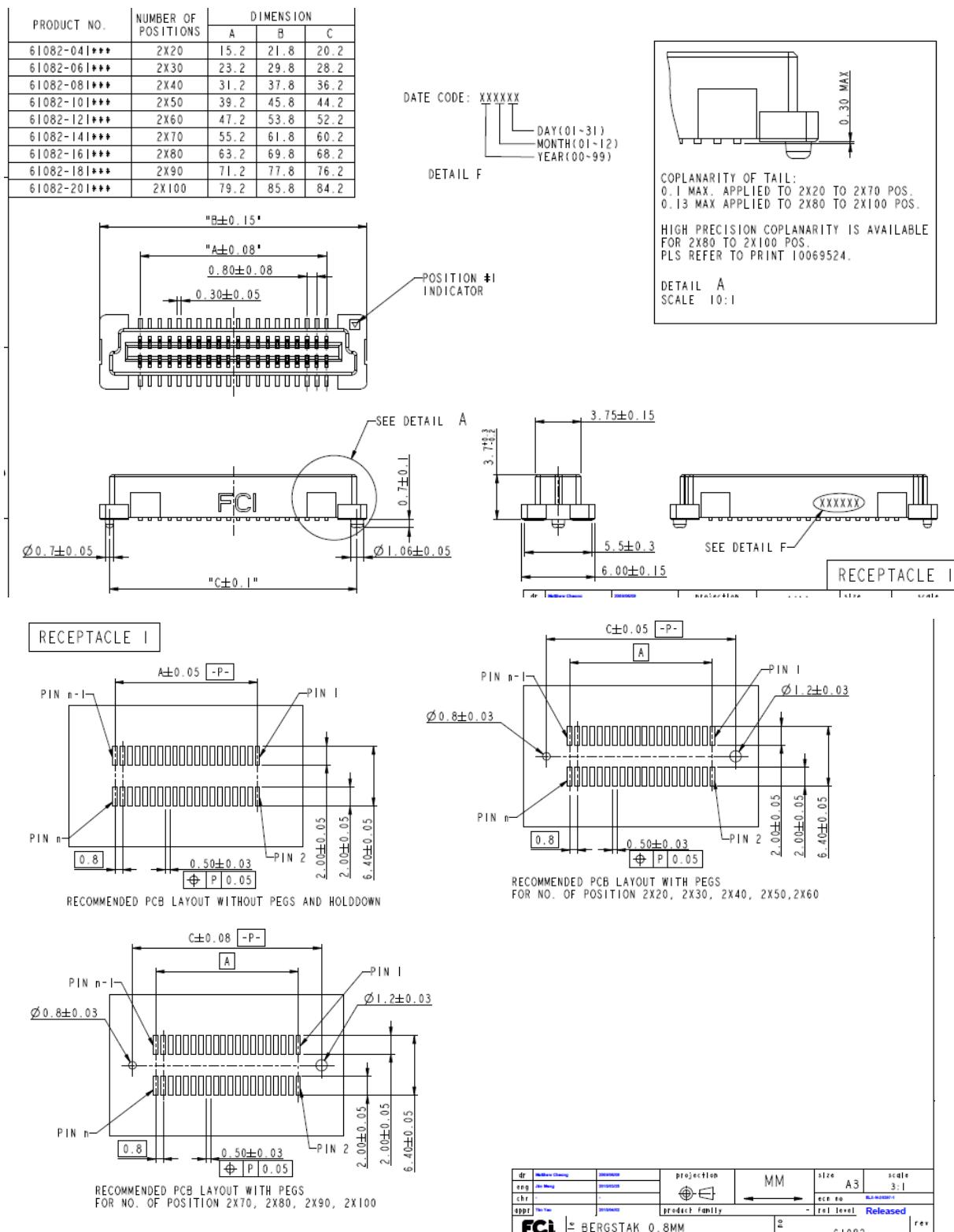


Figure 2-3 Pitch 0.8mm Vertical Double Row 80 PIN PCB Package

2.5 MIPI DPHY DSI TX Extension Connector Information

CON5000 is vertical double-row 30PIN card sockets with 1mm pins and 0.5mm spacing, model: FP05SL_030_V.

The dimensions are as follows:

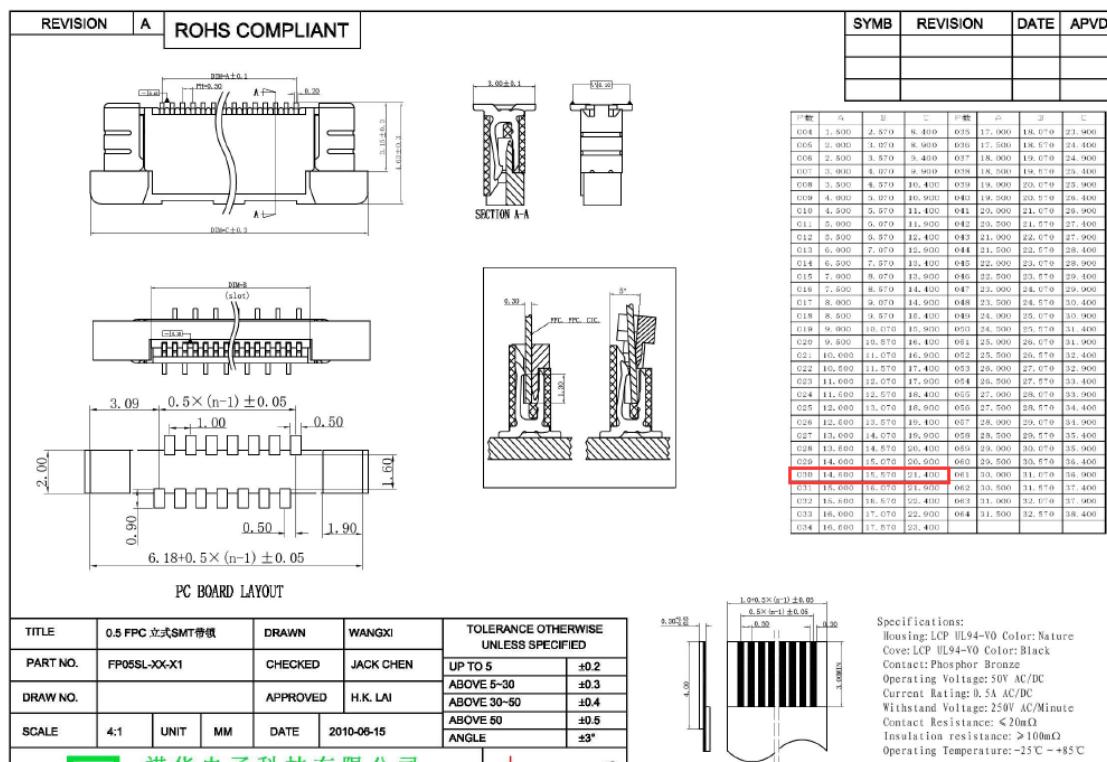


Figure 2-4 Pitch 0.5mm Vertical Double Row 30 PIN PCB Package

2.6 Reference Design

The reference diagram and PCB design information corresponding to the EVB are as follows:

- Reference diagram: RK_EVB1_RK3576_LP4XD200P132SD6_V101_20240321HSW.DSN
- PCB design: RK_EVB1_RK3576_LP4XD200P132SD6_V101_20240321YWQ_final.brd

Note: The reference schematics and PCB silkscreen may not be consistent, and only the BOM information has been updated. The latest schematics have been updated with feedback methods for RK806 BUCK5 GPU and BUCK2 NPU power supplies. The PMU RK806 side filtering capacitor has been removed, and an additional capacitor has been added to the SOC RK3576 side to improve ripple quality.

3 Modules Introduction

3.1 Power Input

Power adapter input 12V/3A power supply, through the front-end buck converter (buck), to get the system power supply VCC5V0_SYS_S5, and then the system voltage is provided to the PMIC power management chip, the output of different voltages for the system to use.

Power adapter input port, front-end Buck converter and PMIC chip:

- Serial number 1 is 12V voltage input
- Serial number 2 is 12V to VCC5V_SYS_S5 voltage buck.
- Serial number 3 is 12V to VCC5V_DEVICE_S0 voltage buck.
- Serial number 4 is the RK806S-5 PMIC chip.

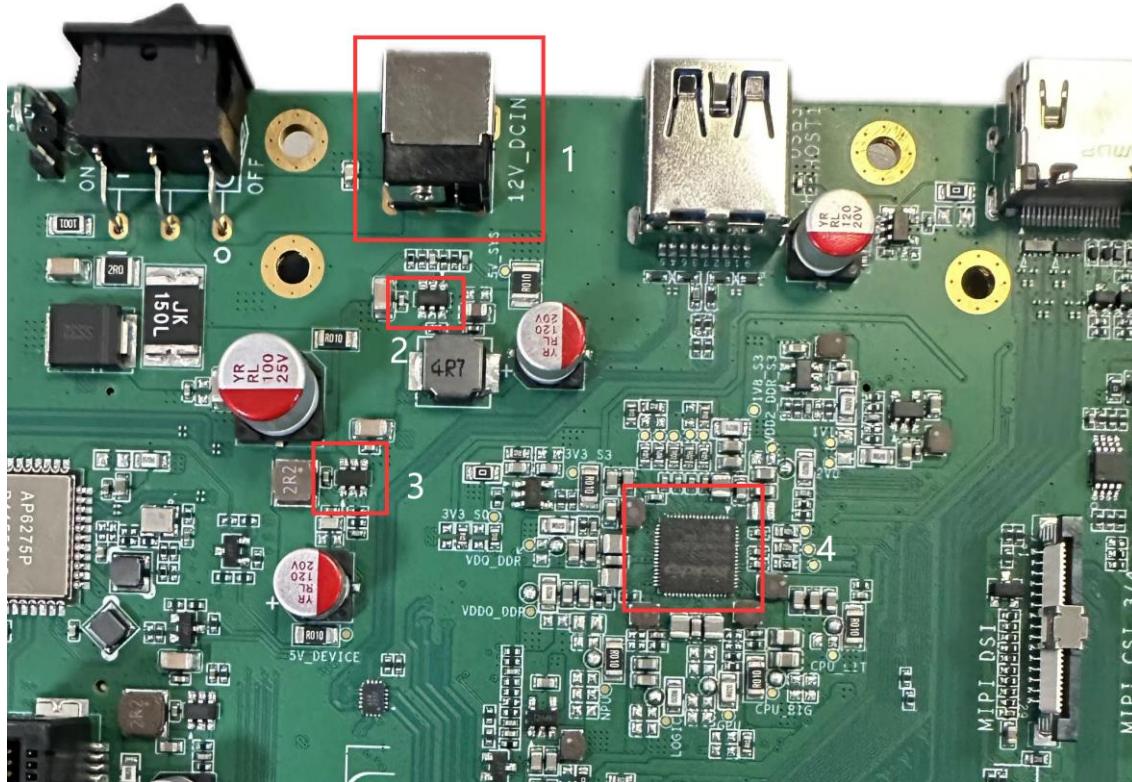


Figure 3-1 DC12V power input, buck convert, PMIC

3.2 Memory

- UFS: The memory type on the development board is UFS, with a default capacity of 128GB, as indicated by number 1 in the following diagram.
- DDR: The development board uses an 8GB LPDDR4x chip for DDR memory, as indicated by number 2 in the following diagram.
- eMMC: The development board reserves a location for an eMMC device, as indicated by number 3 in the following diagram.

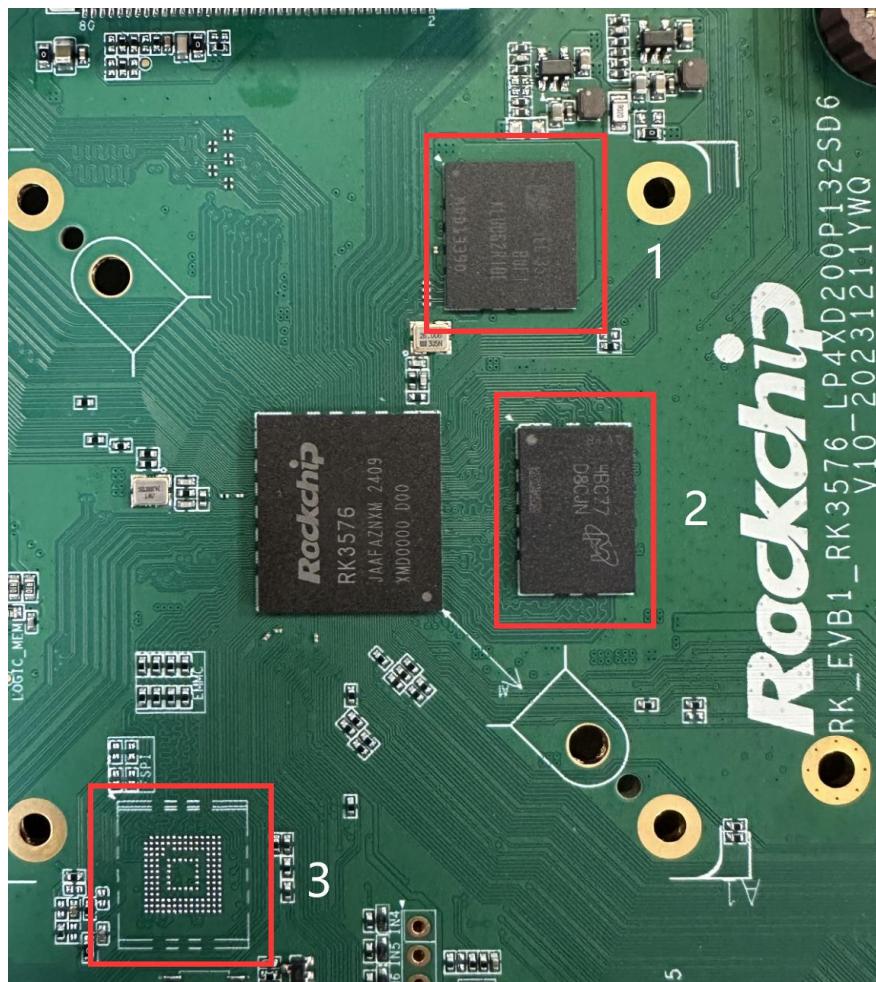


Figure 3-2 RK3576 EVB1 memory

3.3 RTC Circuit

The RTC circuit uses the HYM8563TS chip, which can be powered by the development board or by its coin cell (not by default, it's need to buy your own CR1220-3V coin cell), to ensure that the board can continue to provide accurate time even in the power-off situation, and communicates with the master control via I2C signals.



Figure 3-3 RTC circuit

3.4 TYPEC Interface

The development board supports a full TYPEC interface that supports the following functions:

- USB2_OTG0 of this interface can be used to firmware download
- Supports TYPEC function
- Supports DP1.4 output.

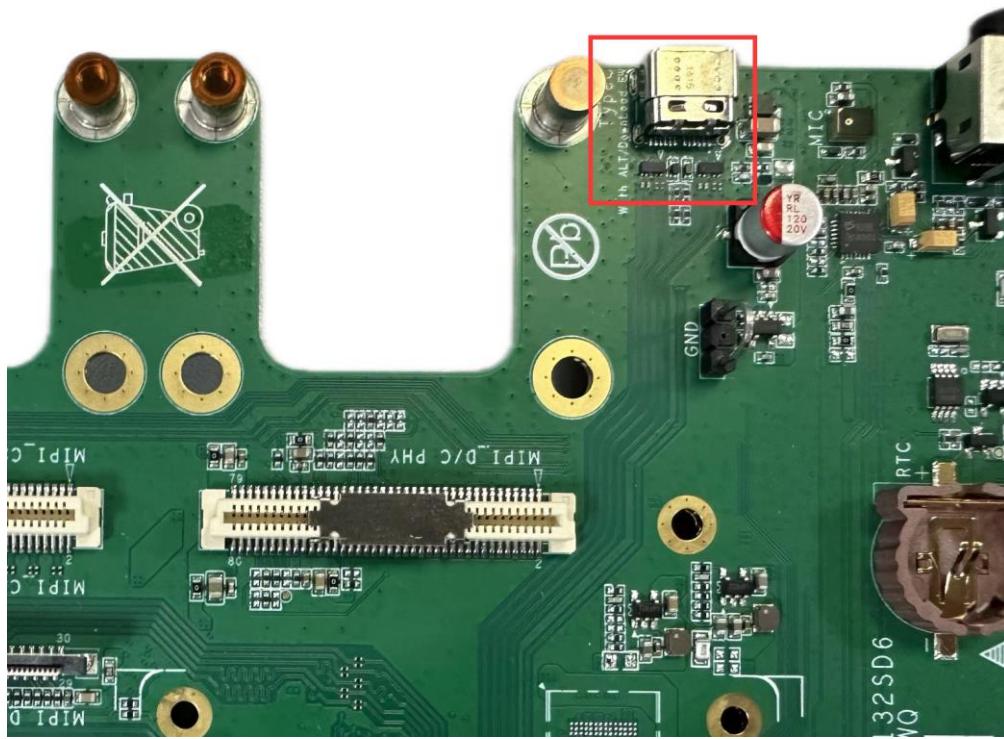


Figure 3-4 TYPEC interface

3.5 USB3.0 Host Interface

Development board supports a USB3.0 Host interface; interface for is the standard A port, easy for developers to

access USB3.0 USB flash drives and other USB3.0 devices. The board is configured for USB3.0 Host by default; however, it shares signals with the PCIe seat, so if you need to use the USB3.0 Host function, you need to hit the dip switch to the off end.

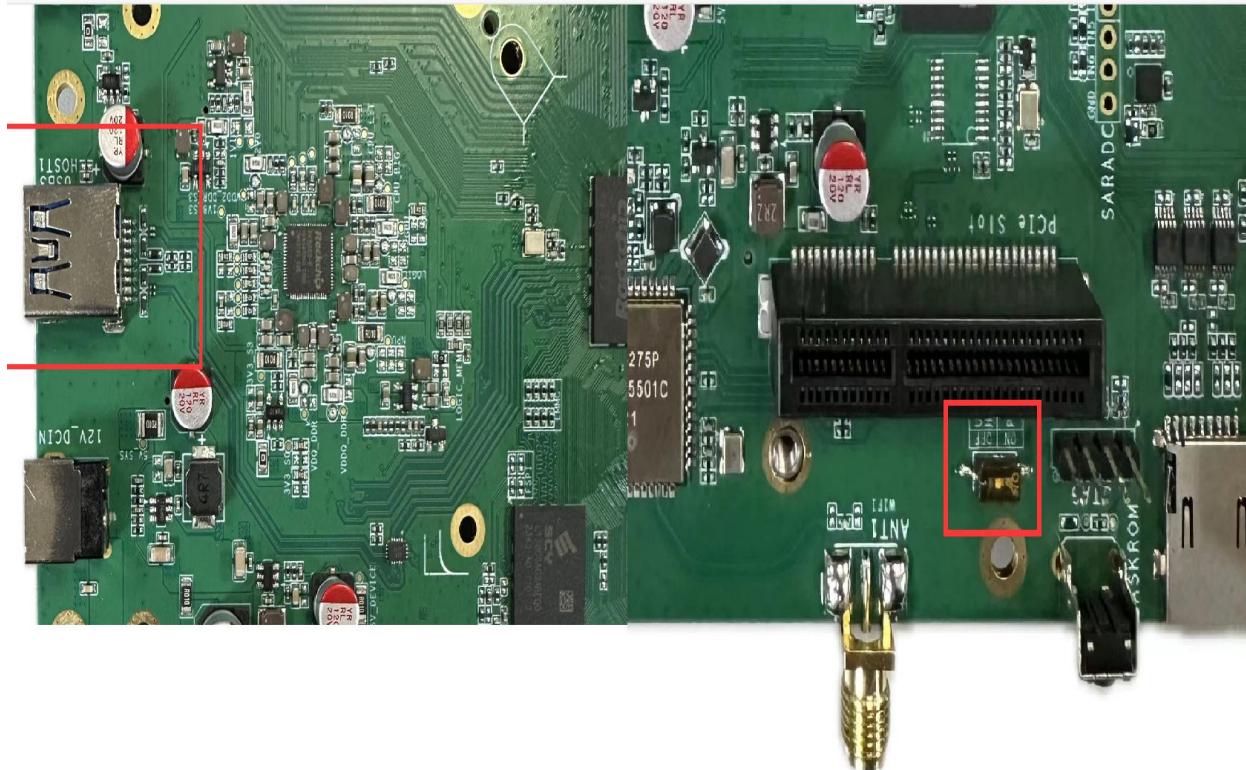


Figure 3-5 USB3.0 Host interface and dipswitch

In addition, the USB3.0 Host interface supports sleep wake up function, users who need this function need to make the following modifications:

Table 3-1 USB3.0 Host supports sleep wake up resistor modify

Net name	Jump resistance	Modify reason
VCC5V0_USB3_HOST1	R2525→R2528	Ensure USB Host interface output 5V when sleep
USB2_OTG_DVDD0V75	R1407→R1408	Ensure USB2.0 PHY be powered when sleep
USB2_OTG_AVDD1V8	R1409→R1410	Ensure USB2.0 PHY be powered when sleep
USB2_OTG_AVDD3V3	R1412→R1411	Ensure USB2.0 PHY be powered when sleep
OSC_1V8	R1119→R1124	Ensure OSC module be powered when sleep

3.6 TF Card Interface

The development board supports one way TF Card interface; it can expand the system memory capacity, the data bus width is 4bits, and supports SD3.0, MMC ver4.51.

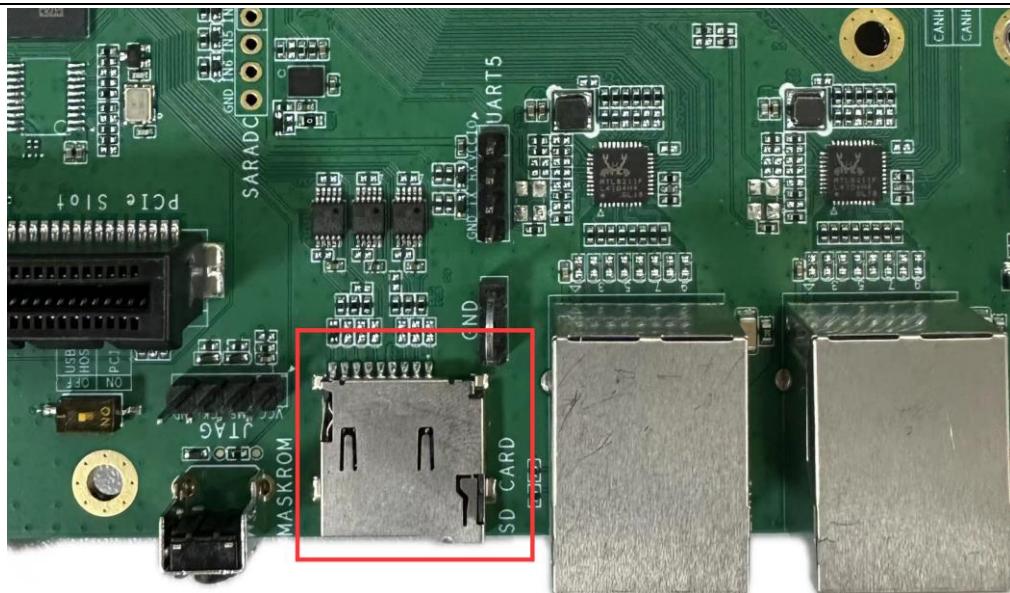


Figure 3-6 TF Card interface

Note: Since the SD card signals are multiplexed with the CAN and JTAG signals, the CAN and JTAG interfaces are not available when the SD card is inserted.

3.7 MIPI DCPHY CSI RX Input Interface

The MIPI DCPHY CSI RX input interface adopts a vertical 80-pin socket with a spacing of 0.8mm (model type: 61082-081402LF, specifications can be found in section 2.4). It supports a single MIPI DCPHY CSI RX interface input. It can accommodate either a single 4-lane DPHY module input or two 3-trios CPHY module inputs. The maximum data rates supported by MIPI DPHY/CPHY are 4.5Gbps/Lane and 5.7Gbps/Trio, respectively. The corresponding receptacle model for this 80-pin socket is 61083-081402LF, and the package dimensions can be referred to in section 2.4. Customers can create expansion boards according to your requirements.

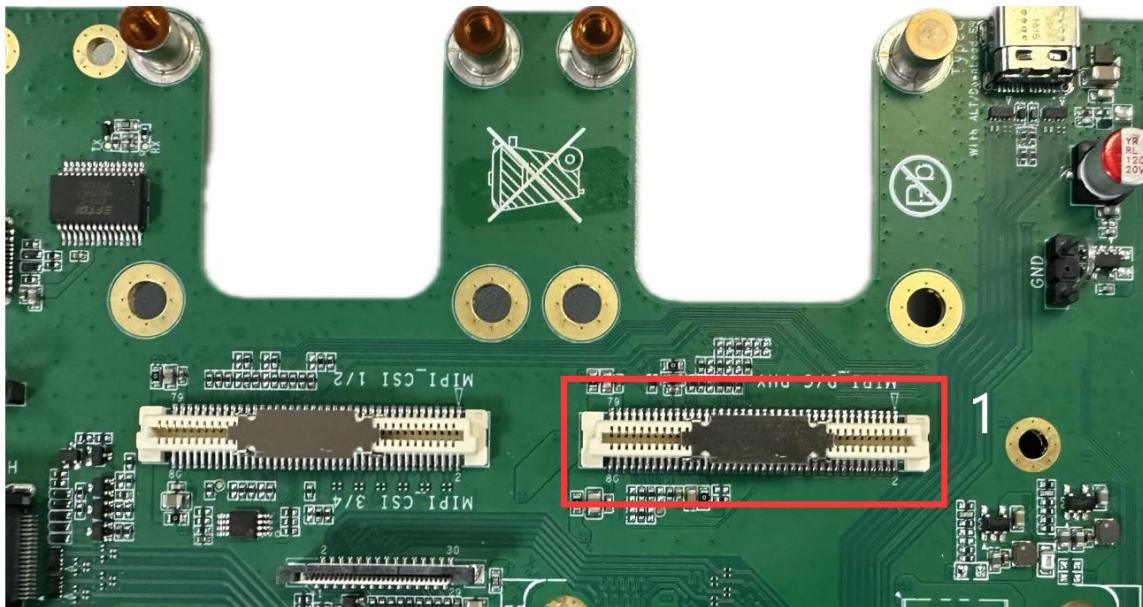


Figure 3-7 MIPI DCPHY CSI RX input interface

MIPI DCPHY CSI RX interface signal sequence:

Table 3-2 MIPI DCPHY CSI RX signal definition

Pin	DPHY (single)	DPHY (dual)	CPHY (single)	Cphy (dual)	Pin
1	GND	GND	GND	GND	2
3	MIPI_DPHY_CSI0_RX_D0N	NC	MIPI_CPHY_CSI_RX_TRIO0_A	NC	4
5	MIPI_DPHY_CSI0_RX_D0P	NC	MIPI_CPHY_CSI_RX_TRIO0_B	NC	6
7	GND	GND	GND	GND	8
9	MIPI_DPHY_CSI0_RX_D1N	NC	MIPI_CPHY_CSI_RX_TRIO0_C	NC	10
11	MIPI_DPHY_CSI0_RX_D1P	NC	MIPI_CPHY_CSI_RX_TRIO1_A	NC	12
13	GND	GND	GND	GND	14
15	MIPI_DPHY_CSI0_RX_CLKN	NC	MIPI_CPHY_CSI_RX_TRIO1_B	NC	16
17	MIPI_DPHY_CSI0_RX_CLKP	NC	MIPI_CPHY_CSI_RX_TRIO1_C	NC	18
19	GND	GND	GND	GND	20
21	MIPI_DPHY_CSI0_RX_D2N	NC	MIPI_CPHY_CSI_RX_TRIO2_A	NC	22
23	MIPI_DPHY_CSI0_RX_D2P	NC	MIPI_CPHY_CSI_RX_TRIO2_B	NC	24
25	GND	GND	GND	GND	26
27	MIPI_DPHY_CSI0_RX_D3N	NC	MIPI_CPHY_CSI_RX_TRIO2_C	NC	28
29	MIPI_DPHY_CSI0_RX_D3P	NC	NO_USE	NC	30
31	GND	GND	GND	GND	32
33	NC	NC	NC	NC	34
35	NC	NC	NC	NC	36
37	GND	GND	GND	GND	38
39	MIPI_DPHY_CSI0_CAM_CLK	NC	MIPI_DPHY_CSI0_CAM_CLK	NC	40
41	NC	NC	NC	NC	42
43	GND	GND	GND	GND	44
45	I2C4_SDA_M3_MIPI_CSI0	NC	I2C4_SDA_M3_MIPI_CSI0	NC	46
47	I2C4_SCL_M3_MIPI_CSI0	NC	I2C4_SCL_M3_MIPI_CSI0	NC	48
49	NC	NC	NC	NC	50
51	MIPI_DPHY_CSI0_PDN_H	VIDEOIN_RESERVE_IO0	MIPI_DPHY_CSI0_PDN_H	VIDEOIN_RESERVE_IO0	52
53	NC	NC	NC	NC	54
55	NC	NC	NC	NC	56
57	MIPI_DPHY_FSYNC	NC	MIPI_DPHY_FSYNC	NC	58
59	MIPI_DPHY_HSYNC	NC	MIPI_DPHY_HSYNC	NC	60
61	VCC_1V8_S0	VCC_3V3_S0	VCC_1V8_S0	VCC_3V3_S0	62
63	NC	NC	NC	NC	64
65	MIPI_DPHY_CSI0_PWREN_H	VIDEOIN_RESERVE_IO1	MIPI_DPHY_CSI0_PWREN_H	VIDEOIN_RESERVE_IO1	66
67	IRC_AIN	NC	IRC_AIN	NC	68

Pin	DPHY (single)	DPHY (dual)	Cphy (single)	Cphy (dual)	Pin
69	IRC_BIN	SAI4_MCLK_M2_DCPHY	IRC_BIN	SAI4_MCLK_M2_DCPHY	70
71	NC	SAI4_SCLK_M2_DCPHY	NC	SAI4_SCLK_M2_DCPHY	72
73	SAI4_LRCK_M2_DCPHY	SAI4_SDI_M2_DCPHY	SAI4_LRCK_M2_DCPHY	SAI4_SDI_M2_DCPHY	74
75	GND	GND	GND	GND	76
77	VCC5V0_DEVICE_S0	GND	VCC5V0_DEVICE_S0	GND	78
79	VCC5V0_DEVICE_S0	VCC12V_DCIN	VCC5V0_DEVICE_S0	VCC12V_DCIN	80

Some pin signal of MIPI DCPHY RX CSI interface is multiplexing with other module as follow:

Table 3-3 MIPI DCPHY CSI RX Supported Extended Function Modification Location Table

Pin	Net name	Default connected function	extended function (HDMI to MIPI IN audio)
67	IRC_AIN	IRC_AIN	NC
69	IRC_BIN	IRC_BIN	NC
70	SAI4_MCLK_M2_DCPHY	NC	SAI4_MCLK_M2_DCPHY
72	SAI4_SCLK_M2_DCPHY	NC	SAI4_SCLK_M2_DCPHY
73	SAI4_LRCK_M2_DCPHY	NC	SAI4_LRCK_M2_DCPHY
74	SAI4_SDI_M2_DCPHY	NC	SAI4_SDI_M2_DCPHY

The extended function is audio function, which can be applied to the audio path of HDMI IN to MIPI IN put. It is necessary to change the SW1800 and SW1801 dip switches (position as below) and jumper resistors R1841→R1840, R1847→R1844, R1852→R1850, R1827→R1828 (this modification affects the function of the HDMI TX module), and the position on the EVB1 board is as below:



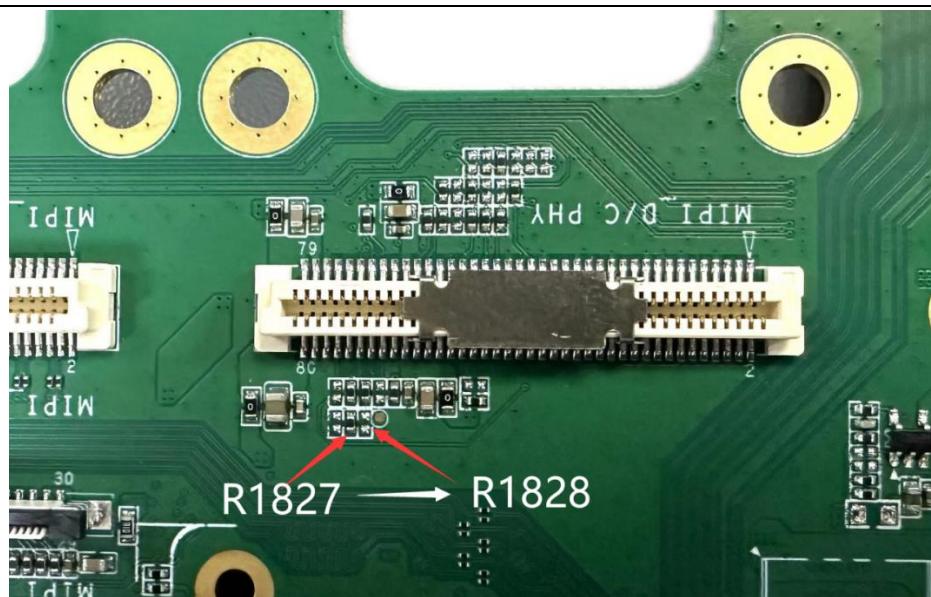


Figure 3-8 MIPI DCPHY CSI RX Extended Function Modification Location

3.8 MIPI DPHY CSI RX Input Interface

The MIPI DPHY CSI RX input interface adopts a vertical 80-pin socket with a spacing of 0.8mm (model number: 61082-081402LF, specifications can be found in section 2.4). It supports either two 4-lane MIPI DPHY module inputs or four 2-lane MIPI DPHY signal inputs. The maximum data rate supported by MIPI DPHY is 2.5Gbps/Lane. Along with MIPI DCPHY, it can support a maximum of 5 module inputs. The corresponding receptacle model for this 80-pin socket is 61083-081402LF, and the package dimensions can be referred to in section 2.4. Customers can create expansion boards according to your requirements.

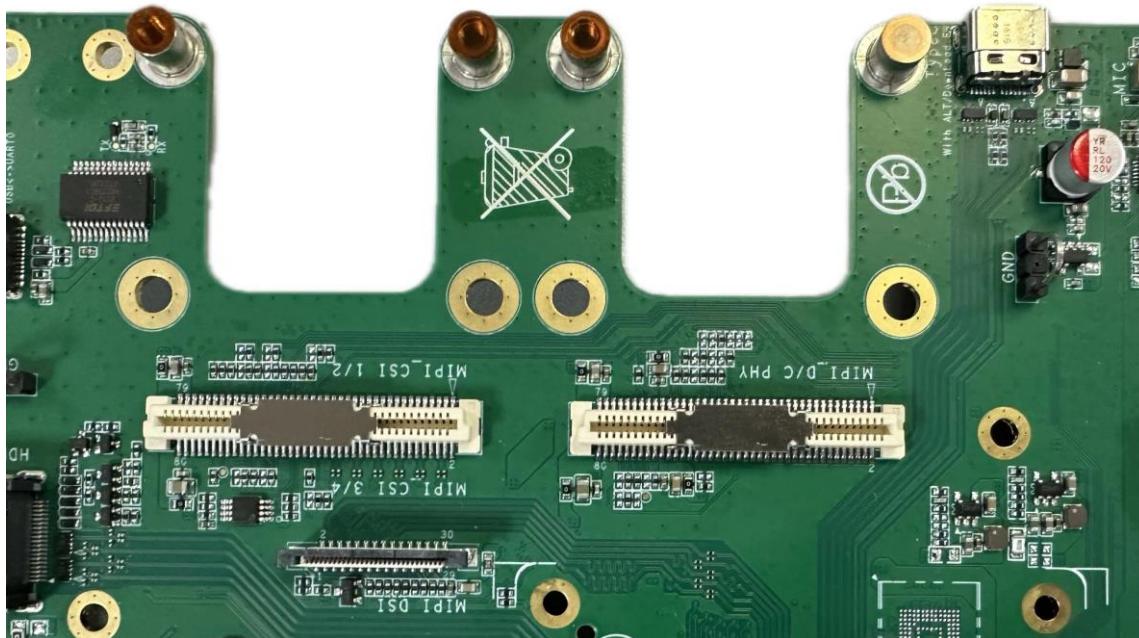


Figure 3-9 MIPI DPHY video input interface

Table 3-4 MIPI DPHY_RX signal definition

Pin	DPHY (single)	DPHY (dual)	Pin
1	GND	GND	2
3	MIPI_DPHY_CSI1_RX_D0N	MIPI_DPHY_CSI3_RX_D0N	4
5	MIPI_DPHY_CSI1_RX_D0P	MIPI_DPHY_CSI3_RX_D0P	6
7	GND	GND	8
9	MIPI_DPHY_CSI1_RX_D1N	MIPI_DPHY_CSI3_RX_D1N	10
11	MIPI_DPHY_CSI1_RX_D1P	MIPI_DPHY_CSI3_RX_D1P	12
13	GND	GND	14
15	MIPI_DPHY_CSI1_RX_CLKN	MIPI_DPHY_CSI3_RX_CLKN	16
17	MIPI_DPHY_CSI1_RX_CLKP	MIPI_DPHY_CSI3_RX_CLKP	18
19	GND	GND	20
21	MIPI_DPHY_CSI1_RX_D2N/	MIPI_DPHY_CSI3_RX_D2N/	
	MIPI_DPHY_CSI2_RX_D0N	MIPI_DPHY_CSI4_RX_D0N	22
23	MIPI_DPHY_CSI1_RX_D2P/	MIPI_DPHY_CSI3_RX_D2P/	
	MIPI_DPHY_CSI2_RX_D0P	MIPI_DPHY_CSI4_RX_D0P	24
25	GND	GND	26
27	MIPI_DPHY_CSI1_RX_D3N/	MIPI_DPHY_CSI3_RX_D3N/	
	MIPI_DPHY_CSI2_RX_D1N	MIPI_DPHY_CSI4_RX_D1N	28
29	MIPI_DPHY_CSI1_RX_D3P/	MIPI_DPHY_CSI3_RX_D3P/	
	MIPI_DPHY_CSI2_RX_D1P	MIPI_DPHY_CSI4_RX_D1P	30
31	GND	GND	32
33	MIPI_DPHY_CSI2_RX_CLKN	MIPI_DPHY_CSI4_RX_CLKN	34
35	MIPI_DPHY_CSI2_RX_CLKP	MIPI_DPHY_CSI4_RX_CLKP	36
37	GND	GND	38
39	MIPI_DPHY_CSI1_CAM_CLKOUT	MIPI_DPHY_CSI3_CAM_CLKOUT	40
41	MIPI_DPHY_CSI2_CAM_CLKOUT_CON	MIPI_DPHY_CSI4_CAM_CLKOUT_CON	42
43	GND	GND	44
45	I2C5_SDA_M3_MIPI_CSI1	I2C_SDA_MIPI_CSI3	46
47	I2C5_SCL_M3_MIPI_CSI1	I2C_SCL_MIPI_CSI3	48
49	NC	NC	50
51	MIPI_DPHY_CSI1_PDN_H	MIPI_DPHY_CSI3_PDN_H	52
53	NC	NC	54
55	MIPI_DPHY_CSI2_PDN_H	MIPI_DPHY_CSI4_PDN_H	56
57	MIPI_CSI1_RX_XVS/MIPI_CSI1_PWM	MIPI_CSI3_RX_XVS/MIPI_CSI3_PWM	58
59	MIPI_CSI1_RX_XHS/MIPI_CSI2_PWM	MIPI_CSI3_RX_XHS/MIPI_CSI4_PWM	60
61	VCC_1V8_S0	VCC_3V3_S0	62

Pin	DPHY (single)	DPHY (dual)	Pin
63	NC	NC	64
65	MIPI_DPHY_CSI1/2_PWREN_H	MIPI_DPHY_CSI3/4_PWREN_H	66
67	IRC_AIN	NC	68
69	IRC_BIN	MIPI_CSI_SAI_MCLK	70
71	MIPI_CSI2_I2C_SDA	MIPI_CSI4_I2C_SDA/SAI_SCLK	72
73	MIPI_CSI2_I2C_SCL/SAI_LRCK	MIPI_CSI4_I2C_SCL/SAI_SDIO/SPDIF_RX	74
75	GND	GND	76
77	VCC5V0_DEVICE_S0	GND	78
79	VCC5V0_DEVICE_S0	VCC12V_DCIN	80

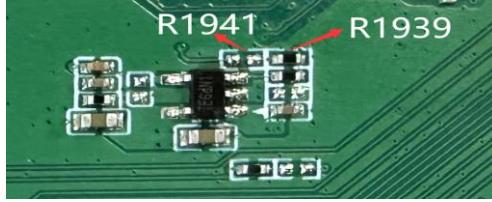
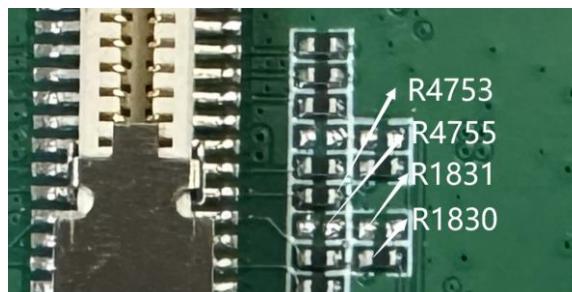
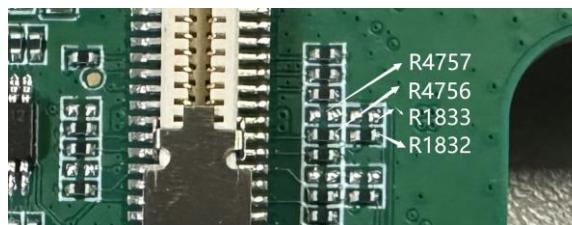
The extended function of the MIPI DPHY CSI RX interface is 5-camera individual control selections, which means that the I2C/MCLK/PWM/PDN signals of each sensor can be controlled separately. The default configuration connects circuit is 2 sensors share a set of I2C/MCLK/PWM/PDN signals. The MIPI DPHY CSI RX interface of the expansion function shares some pin signals with other modules, and customers need to consider the following network signals when design expansion cards:

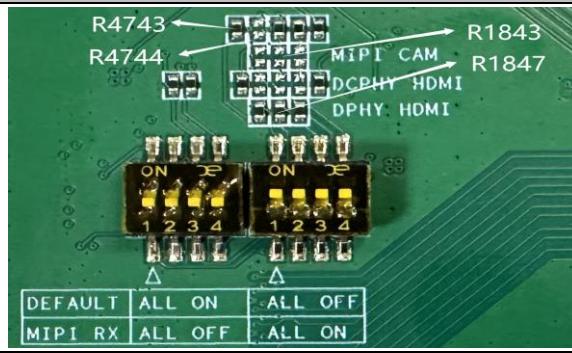
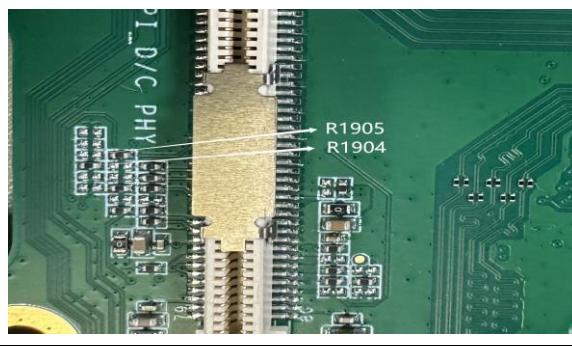
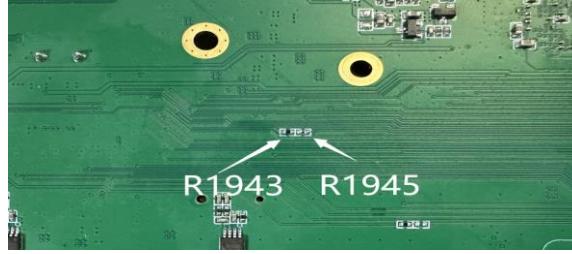
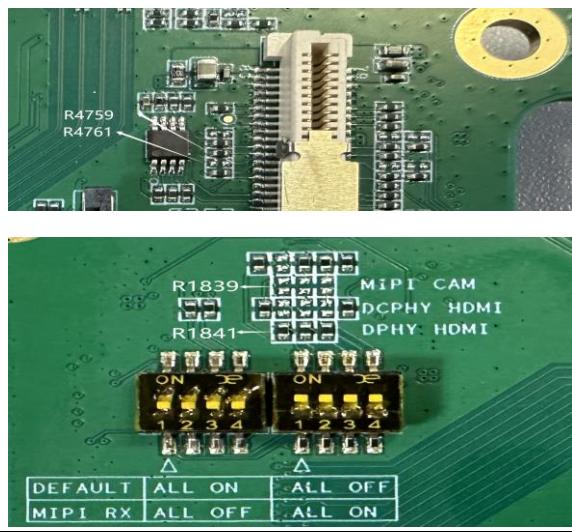
Table 3-5 MIPI DPHY CSI RX Supported Extended Function Modification Location Table

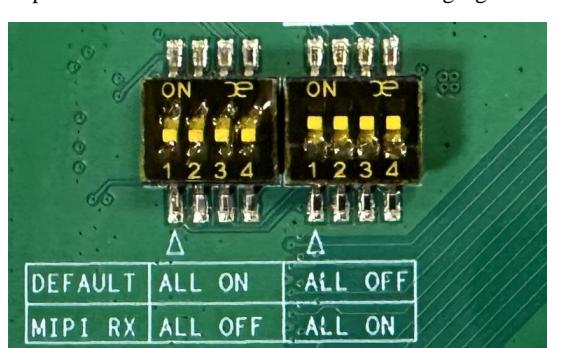
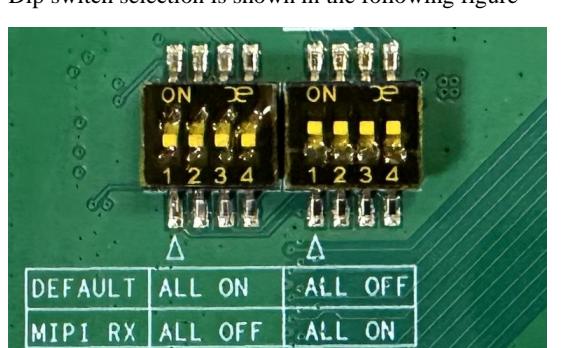
Pin	Net name	Default connected function (5-camera control together)	extended function (5-camera control individual)
41	MIPI_DPHY_CSI2_CAM_CLKOUT_CON	MIPI_DPHY_CSI2_CAM_CLKOUT_CON	NA
55	MIPI_DPHY_CSI2_PDN_H	NC	MIPI_DPHY_CSI2_PDN_H
57	MIPI_CSI1_RX_XVS/MIPI_CSI1_PWM	MIPI_CSI1_RX_XVS	MIPI_CSI1_PWM
59	MIPI_CSI1_RX_XHS/MIPI_CSI2_PWM	MIPI_CSI1_RX_XHS	MIPI_CSI2_PWM
67	IRC_AIN	IRC_AIN	NC
69	IRC_BIN	IRC_BIN	NC
71	MIPI_CSI2_I2C_SDA	NC	MIPI_CSI2_I2C_SDA
73	MIPI_CSI2_I2C_SCL/SAI_LRCK	NC	MIPI_CSI2_I2C_SCL
42	MIPI_DPHY_CSI4_CAM_CLKOUT_CON	NC	MIPI_DPHY_CSI4_CAM_CLKOUT_CON
56	MIPI_DPHY_CSI4_PDN_H	NC	MIPI_DPHY_CSI4_PDN_H
58	MIPI_CSI3_RX_XVS/MIPI_CSI3_PWM	MIPI_CSI3_RX_XVS	MIPI_CSI3_PWM
60	MIPI_CSI3_RX_XHS/MIPI_CSI4_PWM	MIPI_CSI3_RX_XHS	MIPI_CSI4_PWM
70	MIPI_CSI_SAI_MCLK	NC	MIPI_CSI_SAI_MCLK
72	MIPI_CSI4_I2C_SDA/SAI_SCLK	NC	MIPI_CSI4_I2C_SDA/SAI_SCLK
74	MIPI_CSI4_I2C_SCL/SAI_SDIO/SPDIF_RX	NC	MIPI_CSI4_I2C_SCL/SAI_SDIO/SPDIF_RX

There are many items that need to be changed for the extended functions, and the locations of the modifications are given below table

Table 3-6 MIPI DPHY CSI RX Supported Extended Function Modification

Pin	Extended Function	Extended Function (5-camera control individual)																														
41	NA	NA																														
55	MIPI_DPHY_CSI2_PDN_H	R1939→R1941 																														
57	MIPI_CSI1_PWM	R4753→R4755, R1830→R1831 																														
59	MIPI_CSI2_PWM	R4756→R4757, R1832→R1833 																														
67	NC	NC																														
69	NC	NC																														
71	MIPI_CSI2_I2C_SDA	R1852→R1849, Dip switch selection is shown in the following figure  <table border="1"> <tr> <td colspan="3">R1849</td> </tr> <tr> <td colspan="3">R1852</td> </tr> <tr> <td colspan="3">M1PI CAM</td> </tr> <tr> <td colspan="3">DCPHY HDMI</td> </tr> <tr> <td colspan="3">DPHY HDMI</td> </tr> <tr> <td colspan="3">ON ON</td> </tr> <tr> <td>1 2 3 4</td> <td>1 2 3 4</td> <td>1 2 3 4</td> </tr> <tr> <td colspan="3">△ △</td> </tr> <tr> <td colspan="3">DEFAULT ALL ON ALL OFF</td> </tr> <tr> <td colspan="3">MIPI RX ALL OFF ALL ON</td> </tr> </table>	R1849			R1852			M1PI CAM			DCPHY HDMI			DPHY HDMI			ON ON			1 2 3 4	1 2 3 4	1 2 3 4	△ △			DEFAULT ALL ON ALL OFF			MIPI RX ALL OFF ALL ON		
R1849																																
R1852																																
M1PI CAM																																
DCPHY HDMI																																
DPHY HDMI																																
ON ON																																
1 2 3 4	1 2 3 4	1 2 3 4																														
△ △																																
DEFAULT ALL ON ALL OFF																																
MIPI RX ALL OFF ALL ON																																
73	MIPI_CSI2_I2C_SCL	R4744→R4743, R1847→R1843 Dip switch selection is shown in the following figure																														

Pin	Extended Function	Extended Function (5-camera control individual)
		
42	MIPI_DPHY_CSI4_CAM_CLKOUT_CON	<p>R1904→R1905</p> 
56	MIPI_DPHY_CSI4_PDN_H	<p>R1943→R1945</p> 
58	MIPI_CSI3_PWM	<p>R4759→R4761, R1841→R1839, Dip switch selection is shown in the following figure</p> 
60	MIPI_CSI4_PWM	<p>R4763→R4764, R1834→R1835</p>

Pin	Extended Function	Extended Function (5-camera control individual)						
		 						
70	MIPI_CSI_SAI_MCLK	R1827→R1829 						
72	SAI_SCLK	Dip switch selection is shown in the following figure  <table border="1" data-bbox="754 1549 1151 1650"> <tr> <td>DEFAULT</td> <td>ALL ON</td> <td>ALL OFF</td> </tr> <tr> <td>MIPI RX</td> <td>ALL OFF</td> <td>ALL ON</td> </tr> </table>	DEFAULT	ALL ON	ALL OFF	MIPI RX	ALL OFF	ALL ON
DEFAULT	ALL ON	ALL OFF						
MIPI RX	ALL OFF	ALL ON						
74	SAI_SDIO0	Dip switch selection is shown in the following figure  <table border="1" data-bbox="754 1942 1151 2043"> <tr> <td>DEFAULT</td> <td>ALL ON</td> <td>ALL OFF</td> </tr> <tr> <td>MIPI RX</td> <td>ALL OFF</td> <td>ALL ON</td> </tr> </table>	DEFAULT	ALL ON	ALL OFF	MIPI RX	ALL OFF	ALL ON
DEFAULT	ALL ON	ALL OFF						
MIPI RX	ALL OFF	ALL ON						

3.9 MIPI DPHY DSI TX Interface

Development board reserved 1 MIPI DPHY DSI TX interface, default supporting 1080p screen. It can support user to extend the LCD display. Please refer to section 2.5 for interface package.

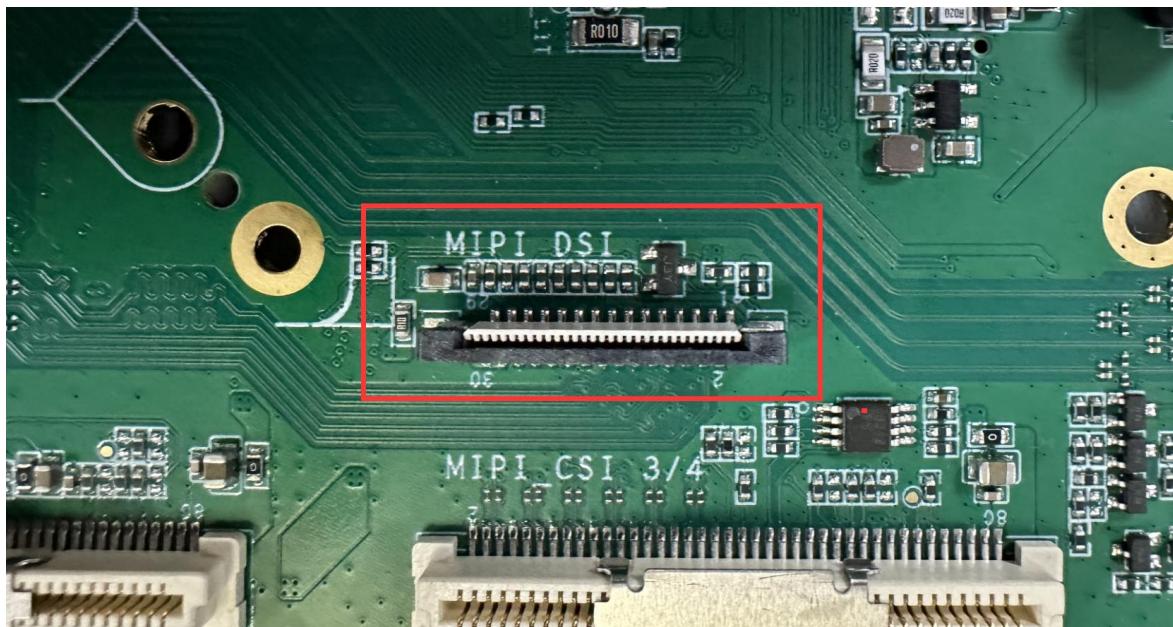


Figure 3-10 MIPI DPHY DSI TX video output interface

MIPI DPHY DSI TX interface signal sequence as follow:

Table 3-7 MIPI DPHY DSI TX interface signal definition

Pin	MIPI DPHY DSI TX (CON5000)		Pin
1	GND	MIPI_DPHY_DSI_TX_D0N	2
3	MIPI_DPHY_DSI_TX_D0P	GND	4
5	MIPI_DPHY_DSI_TX_D1N	MIPI_DPHY_DSI_TX_D1P	6
7	GND	MIPI_DPHY_DSI_TX_CLKN	8
9	MIPI_DPHY_DSI_TX_CLKP	GND	10
11	MIPI_DPHY_DSI_TX_D2N	MIPI_DPHY_DSI_TX_D2P	12
13	GND	MIPI_DPHY_DSI_TX_D3N	14
15	MIPI_DPHY_DSI_TX_D3P	GND	16
17	LCD_BL_PWM1_CH1_M0	MIPI_TE	18
19	VCC3V3_LCD_S0	LCD_RESET_L	20
21	SARADC_VIN7_LCD_ID	LCD_PWR_EN	22
23	I2C0_SCL_M1_TP	I2C0_SDA_M1_TP	24
25	TP_INT_L	TP_RST_L	26
27	GND	VCC5V0_DEVICE_S0	28
29	CON0_VCC5V0_LCD	VCC5V0_DEVICE_S0	30

3.10 HDMI Output Interface

The development board supports one HDMI standard A output interface, the supports HDMI2.1, the support up to 4K120 video output.

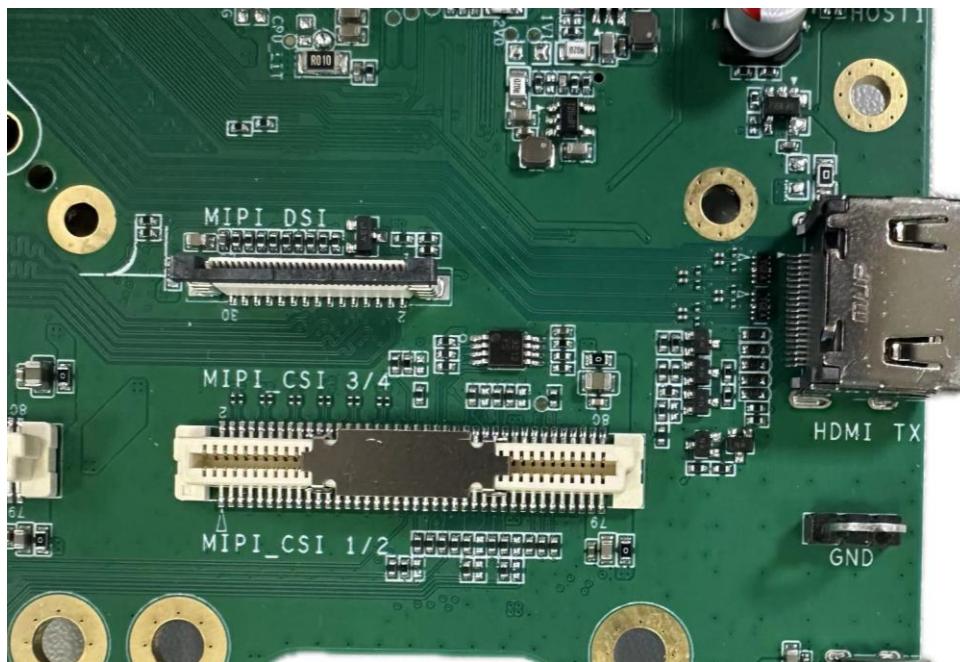


Figure 3-11 MIPI DPHY DSI TX video output interface

3.11 WI-FI/BT Interface

The development board uses the Ampak AP6275P WiFi+ Bluetooth module (as shown in Figure). Its features are as follows:

- Supports 2x2 WiFi 6 (2.4GHz and 5GHz, 802.11 a/b/g/n/ac/ax) and Bluetooth 5.0.
- It has two external SMA interface connectors for antennas (as shown in Figure No.2 and No.3).
- Bluetooth data communication is done through UART.
- Bluetooth voice is connected to the main control via the SAI interface.
- WiFi data communication utilizes the PCIe data bus.

The RK3576 EVB1 development board comes with a dual-mode antenna for 2.4GHz and 5GHz bands by default.

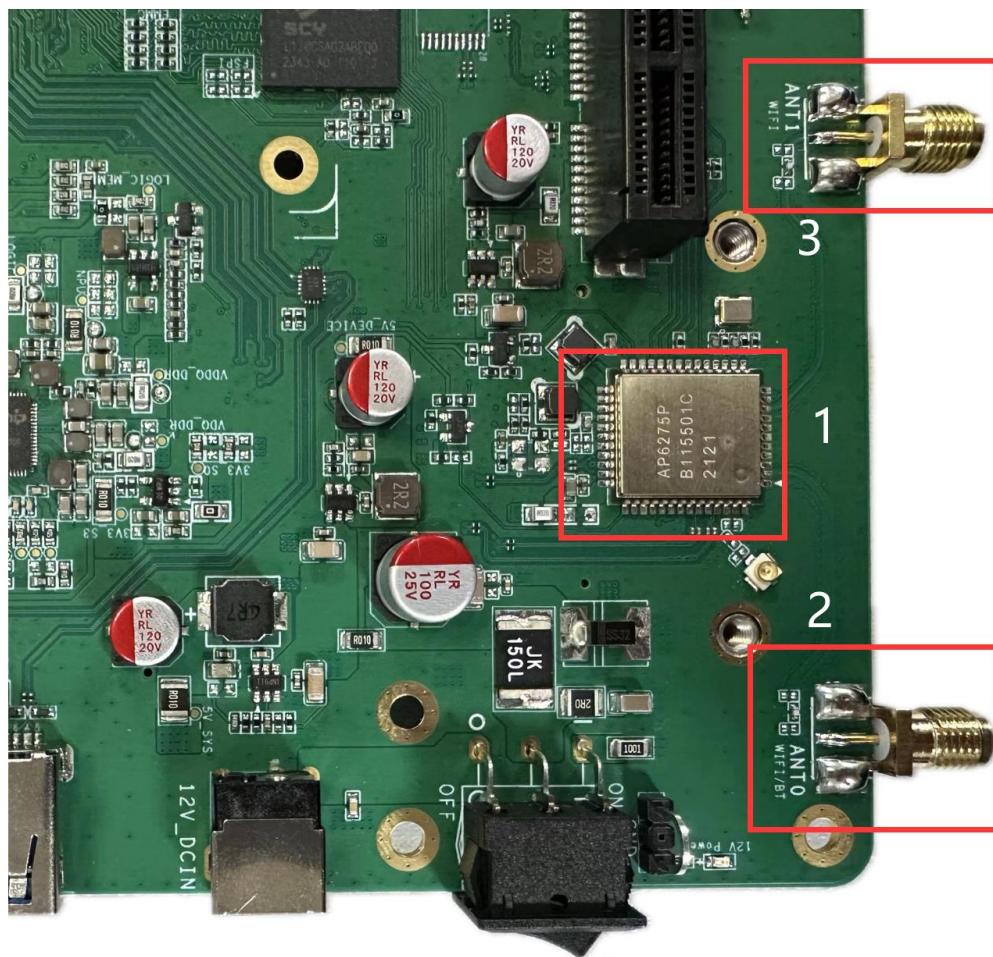


Figure 3-12 WI-FI/BT module dual SMA interface

3.12 SDIO/PCIe WIFI EXT Interface

The development board supports WIFI extend board, which is convenient for customers to debug the WIFI chips and modules required.



Figure 3-13 WI-FI/BT module dual-SMA interface

Table 3-8 SDIO/PCIe WIFI EXT signal definition

Pin	SDIO/PCIe WIFI EXT (single)	SDIO/PCIe WIFI EXT (dual)	Pin
1	GND	VCC12V_DCIN	2
3	VCC_3V3_S3	VCC12V_DCIN	4
5	VCC_3V3_S3	VCC12V_DCIN	6
7	GND	GND	8
9	VCCIO_WL	5V_1	10
11	GND	5V_2	12
13	RSV	GND	14
15	GND	RSV	16
17	USB_DM	GND	18
19	USB_DP	CON_PCIE_WAKEn_L	20
21	GND	CON_PCIE_PERSTn_L	22
23	CLK_32KHz	CON_PCIE_CLKREQn_L	24
25	GND	GND	26
27	HOST_WAKE_WIFI	SDMMC1_CMD_M0	28
29	CON_HOST_WAKE_BT_H	SDMMC1_CLK_M0	30
31	CON_BT_WAKE_HOST	GND	32
33	CON_WIFI_WAKE_HOST	SDMMC1_D3_M0	34
35	CON_BT_REG_ON_H	SDMMC1_D2_M0	36
37	CON_WIFI_REG_ON_H	SDMMC1_D0_M0	38
39	GND	SDMMC1_D1_M0	40
41	UART4_RX_M1	GND	42
43	UART4_TX_M1	CON_PCIE0_REFCLKN	44
45	UART4_CTSN_M1	CON_PCIE0_REFCLKP	46
47	UART4_RTSN_M1	GND	48
49	GND	CON_PCIE0_RXN	50
51	SAI2_SCLK_M0_CON	CON_PCIE0_RXP	52
53	SAI2_LRCK_M0_CON	GND	54
55	SAI2_SDO_M0_CON	CON_PCIE0_TXN	56
57	SAI2_SDI_M0_CON	CON_PCIE0_TXP	58
59	GND	GND	60

Note: This interface shares some pins with the WIFI6 module and cannot be used at the same time. The following table describes the relevant jumper resistors and shared pins.

Table 3-9 SDIO/PCIe WIFI EXT functional resistor

PIN	Net name	Jumper resistors and shared relation
29	CON_HOST_WAKE_BT_H	Share with WIFI6 module AP6275P
31	CON_BT_WAKE_HOST	Share with WIFI6 module AP6275P
33	CON_WIFI_WAKE_HOST	Share with WIFI6 module AP6275P
35	CON_BT_REG_ON_H	Share with WIFI6 module AP6275P
37	CON_WIFI_REG_ON_H	Share with WIFI6 module AP6275P
41	UART4_RX_M1	Share with WIFI6 module AP6275P
43	UART4_TX_M1	Share with WIFI6 module AP6275P
45	UART4_CTSN_M1	Share with WIFI6 module AP6275P
47	UART4_RTSN_M1	Share with WIFI6 module AP6275P
51	SAI2_SCLK_M0_CON	R1821→R1854
53	SAI2_LRCK_M0_CON	R1822→R1855
55	SAI2_SDO_M0_CON	R1820→R1853
57	SAI2_SDI_M0_CON	R1842→R1856
20	CON_PCIE_WAKEn_L	Share with WIFI6 module AP6275P
22	CON_PCIE_PERSTn_L	Share with WIFI6 module AP6275P
24	CON_PCIE_CLKREQn_L	Share with WIFI6 module AP6275P
44	CON_PCIE0_REFCLKN	R1714→R1713
46	CON_PCIE0_REFCLKP	R1716→R1715
50	CON_PCIE0_RXN	R1709→R1708
52	CON_PCIE0_RXP	R1711→R1710
56	CON_PCIE0_TXN	R1706→R1705
58	CON_PCIE0_TXP	R1704→R1703

3.13 Ethernet

The development board supports two RJ45 interfaces, providing dual Gigabit Ethernet connectivity. It utilizes the integrated Gigabit Ethernet MAC within the RK3576 chip, which is connected to an external PHY chip, the RTL8211F-CG. The features of the PHY chip are as follows:

- It is compatible with the IEEE 802.3 standard and supports both full duplex and half duplex operations.
- It supports auto-negotiation and cross-detection.
- The PHY chip supports data rates of 10/100/1000 Mbps.
- The interfaces are equipped with RJ45 connectors that include isolation transformers and indicator lights.

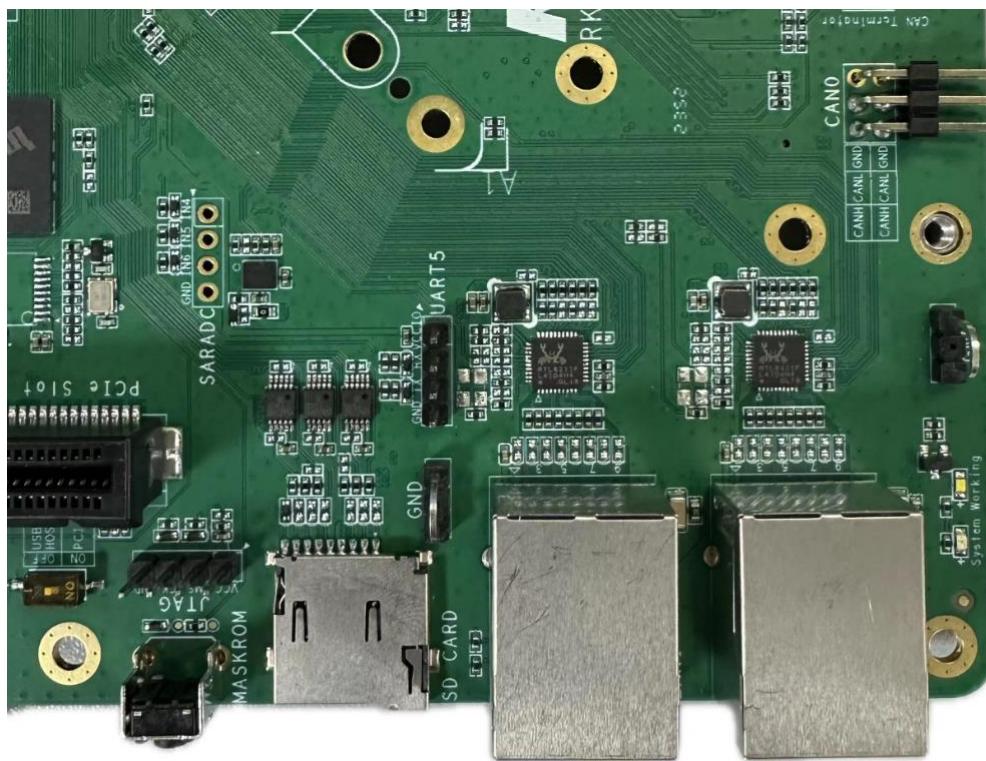
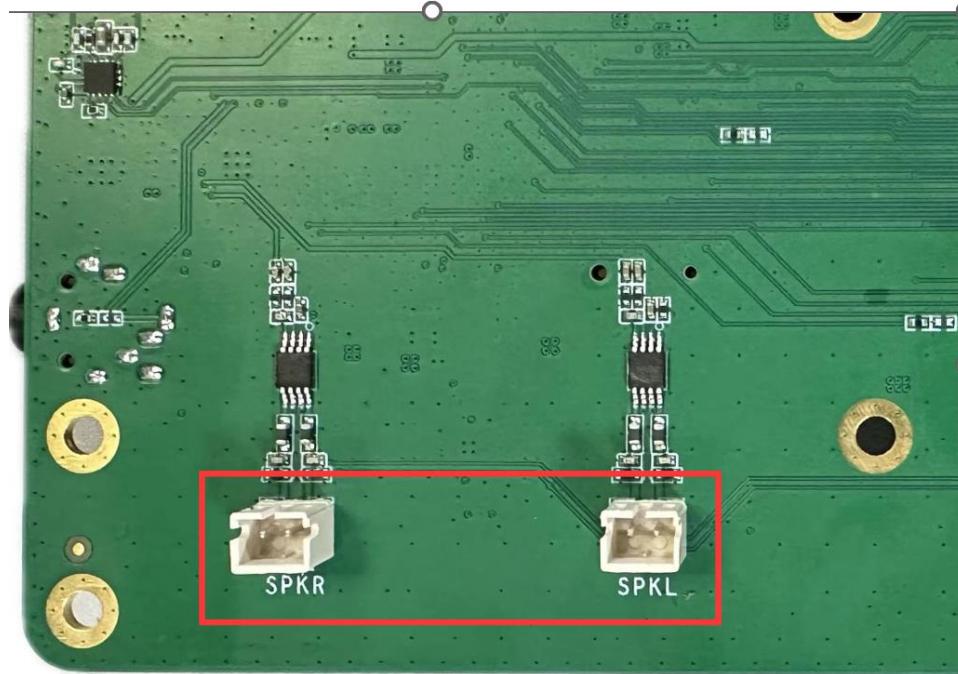


Figure 3-14 Dual Gigabit Ethernet port

3.14 Audio Interface

The development board supports two speaker interfaces, one earphone interface, and one microphone interface. These interfaces enable basic network video calling functionality.



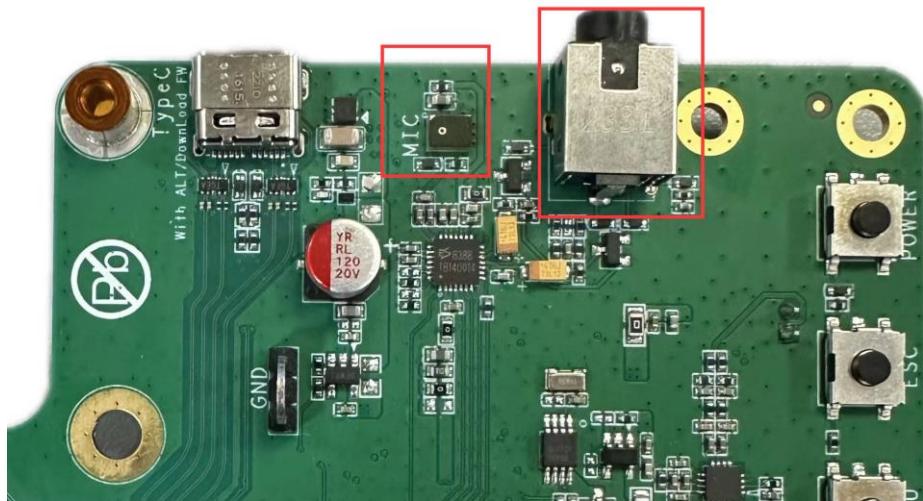


Figure 3-15 SPEAKER/MIC/Earphone interface

3.15 AUDIO MicArray Interface

The board supports MicArray audio board extensions and customised Audio board extensions.



Figure 3-16 AUDIO MicArray extend interface

Table 3-10 AUDIO MicArray signal definition

Pin	AUDIO MicArray (single)	AUDIO MicArray (dual)	Pin
1	VCC_3V3_S0	VCC5V0_DEVICE_S0	2
3	VCC_3V3_S0	VCC5V0_DEVICE_S0	4
5	GND	GND	6
7	AUD_I2C_SDA	VCCIO2	8
9	AUD_I2C_SCL	GND	10
11	GND	NC	12
13	NC	NC	14

Pin	AUDIO MicArray (single)	AUDIO MicArray (dual)	Pin
15	GND	GND	16
17	NC	NC	18
19	GND	GND	20
21	NC	NC	22
23	GND	GND	24
25	NC	NC	26
27	GND	GND	28
29	PDM1_CLK0_M1	PDM1_CLK1_M1	30
31	GND	GND	32
33	PDM1_SDI0_M1	PDM1_SDI1_M1	34
35	PDM1_SDI2_M1	PDM1_SDI3_M1	36
37	GND	GND	38
39	NC	NC	40

Note: This interface shares some pin pins with the speaker loopback chip ES7202 and cannot be used at the same time. The following table describes the relevant jumper resistors and shared pins.

Table 3-11 AUDIO MicArray interface signal modification

PIN	Net name	Jumper resistors and shared relation
29	PDM1_CLK0_M1	R1807→R1809
33	PDM1_SDI0_M1	R1810→R1811
36	PDM1_SDI3_M1	R1804→R1805

3.16 PCIe Connector

The development board uses the standard PCIe connector (as shown in Figure below), allowing for external PCIe expansion cards to be connected for communication.

- The working mode is Root Complex (RC).
- The link supports PCIe 2.1 with a 1-lane data interface.
- The PCIe clock is provided by the main controller, with a reserved position for an external clock chip RS2CG5705BLE (as indicated by Figure 2).

Note: The PCIe functionality is not connected by default. To enable PCIe functionality, switch the DIP switch (as indicated 3 show the below Figure) to the ON position.

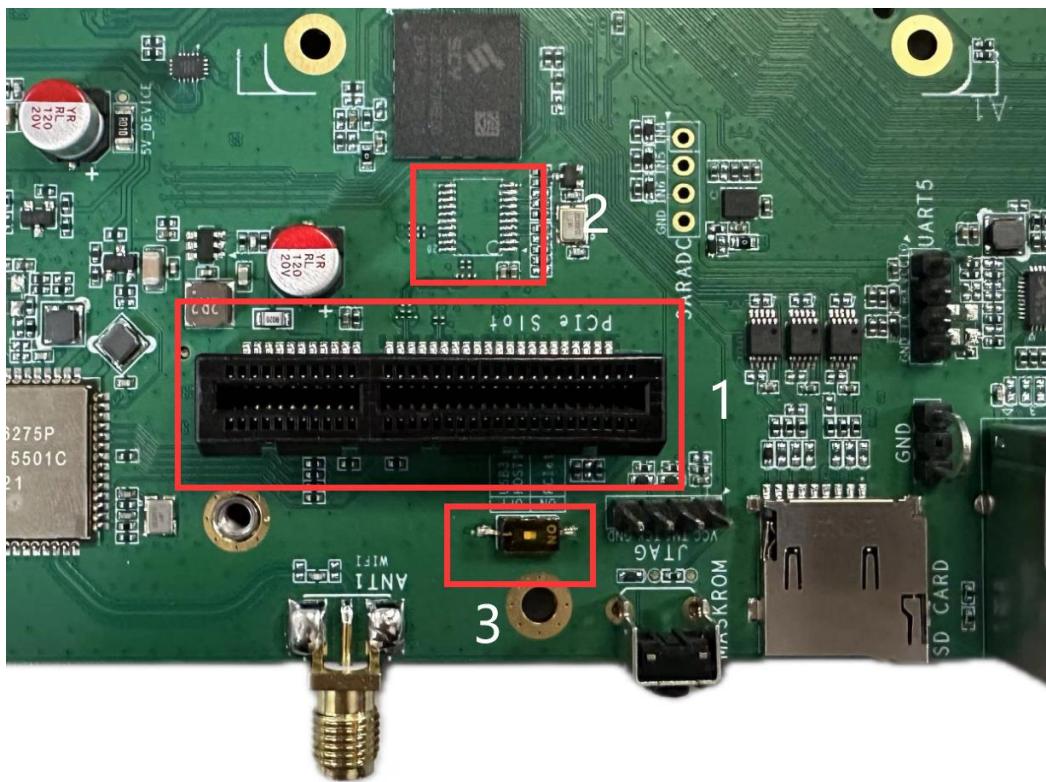


Figure 3-17 PCIe connector

3.17 Button Input

The development board uses SARADC_IN1 as the input for RECOVERY detection, supporting a 12-bit resolution. By pressing the V+/REC button, you can enter the LOADER burning mode. Additionally, the board also has a RESET button for hardware reset and machine reboot. There are several other commonly used buttons: Volume+ (RECOVERY), Volume-, MENU, ESC, and POWER.

The button positions are as follows: [Please provide the button positions for an accurate translation.]

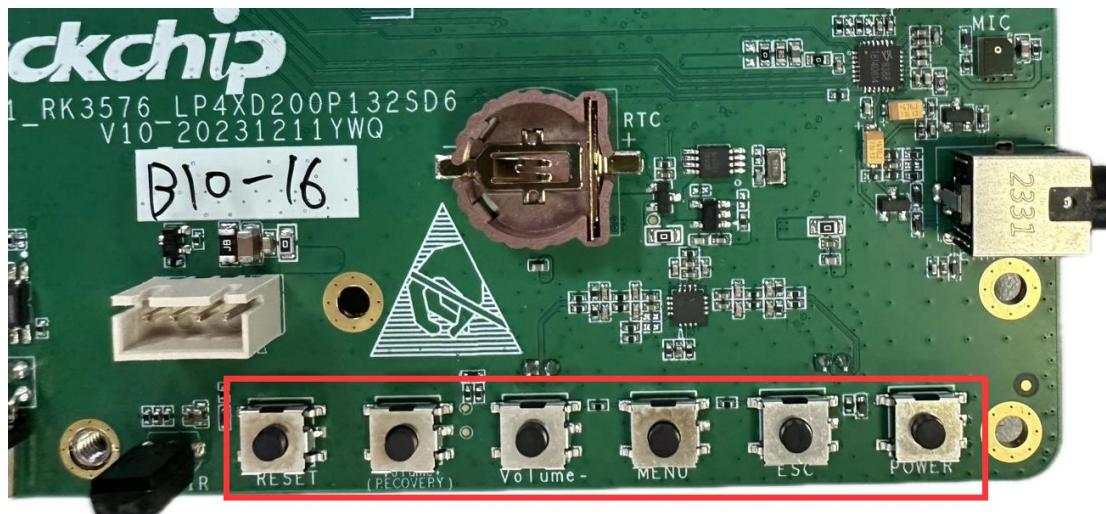


Figure 3-18 Button Input

3.18 Sensor Module Expansion

3.18 Sensor Module Expansion

The development board is equipped with an IMX415 module, which can support a maximum of 800W pixels.

- Supports automatic white balance, 3D noise reduction, and HDR.
- Supports RAW10/RAW12 data output.
- Integrated with an IRCUT switching circuit, capable of controlling the day/night mode of the sensor module.

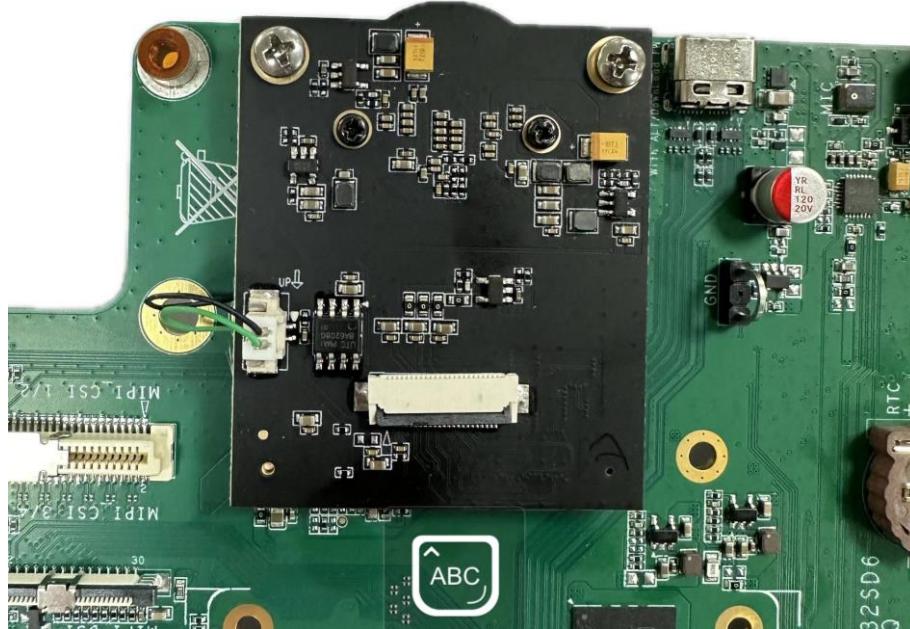


Figure 3-19 IMX415 module extend board

3.19 Gyroscope+G-Sensor

The development board is equipped with a Gyroscope+G-Sensor chip, which is convenient for users to debug related applications.

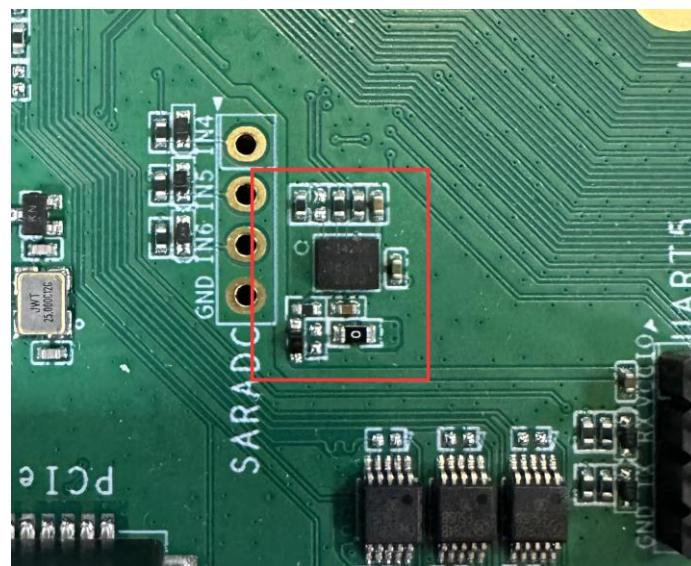


Figure 3-20 Gyroscope+G-Sensor chip

3.20 IR Interface

The development board supports IR function



Figure 3-21 IR interface

3.21 MASKROM

You can enter the MASKROM state by pressing the MASKROM button, and then use it to upgrade the board according to the method described in Section 1.6.

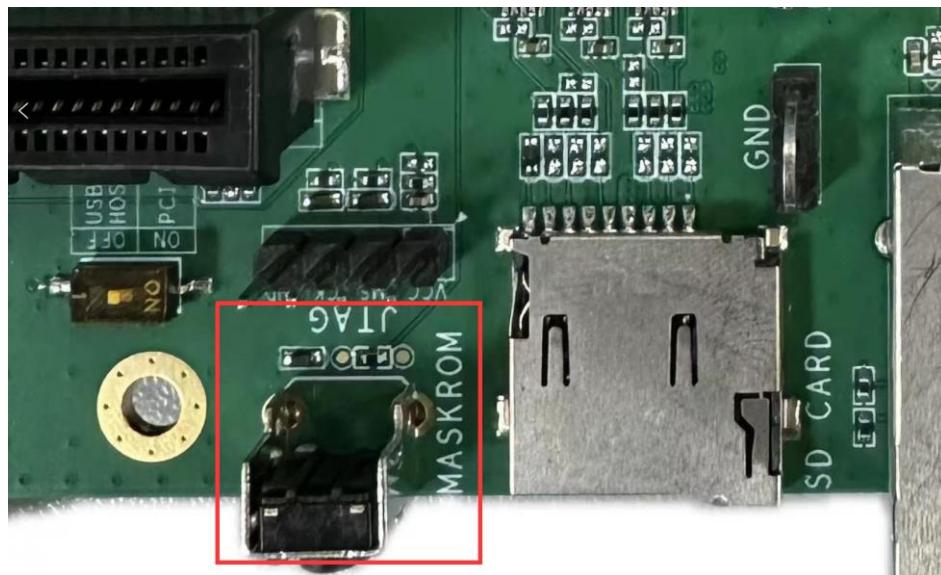


Figure 3-22 MASKROM button

3.22 CAN Interface

The development board has a reserved CAN interface, which is a 2.54mm interface for convenient user expansion. The CAN interface has a reserved position for a 120Ω pin header. If you need to connect it, you can insert a jumper

cap.

Note: The CAN interface cannot be used if an SD card is inserted.

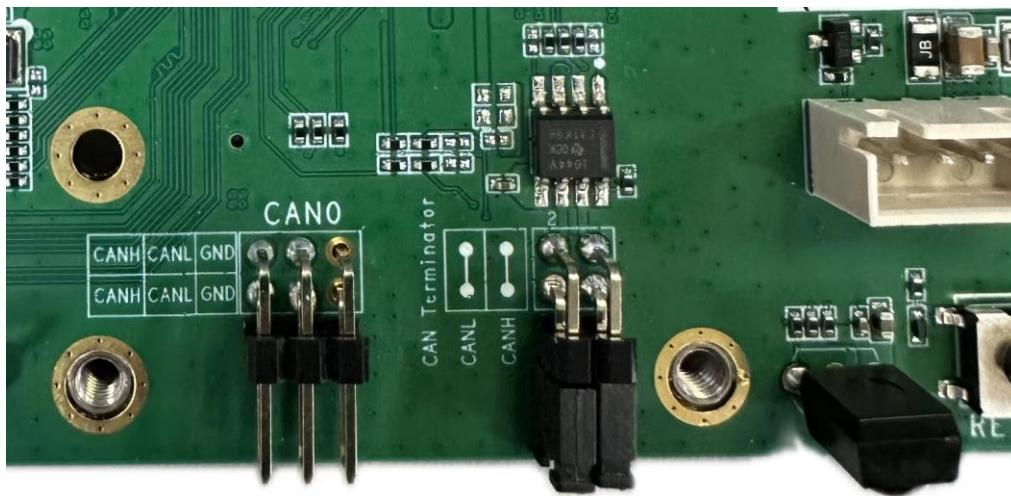


Figure 3-23 CAN interface

3.23 Fan Power Interface

The development board has a reserved fan interface, which supports 12V/5V fans and adjustable speed. The default configuration for the development board is a 12V fan.

The interface pinout, from left to right, is as follows: CONTROL, SENSOR, 12V, GND. Currently, EVB1 does not support sensor-based speed control functionality.

(The pinout order is as follows: PIN4: CONTROL, PIN3: SENSOR, PIN2: 12V, PIN1: GND)



Figure 3-24 fan power interface

3.24 Debug Interface

The development board supports a USB<->UART Debug debugging interface. It is accessible through a TYPE-C socket, making it convenient for debugging.

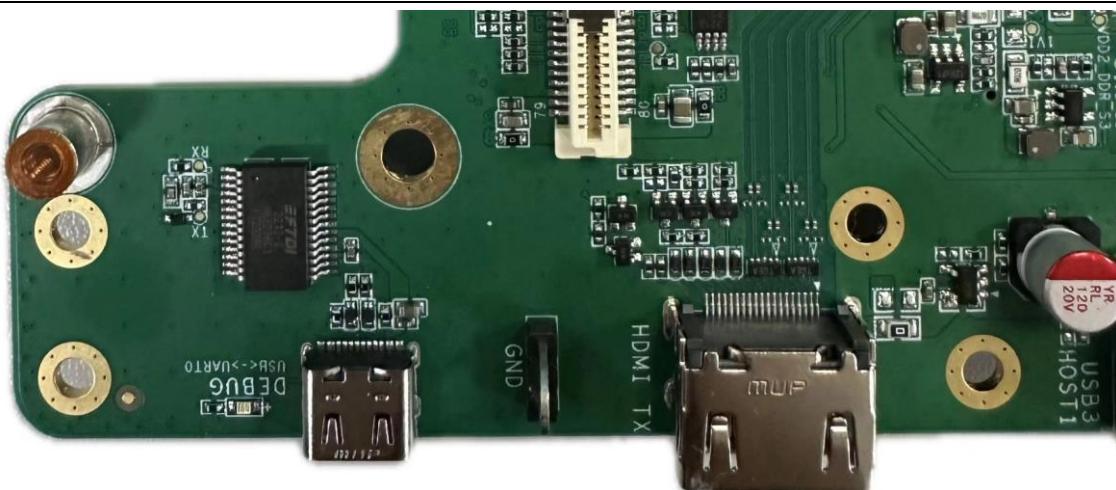


Figure 3-25 Debug Interface

3.25 JTAG Interface

The development board has a reserved JTAG interface, which is designed for pin header connections.

The pin definitions are as follows: PIN1: VCC, PIN2: TMS, PIN3: TCK, PIN4: GND.

Note: JTAG functionality cannot be used if an SD card is inserted.

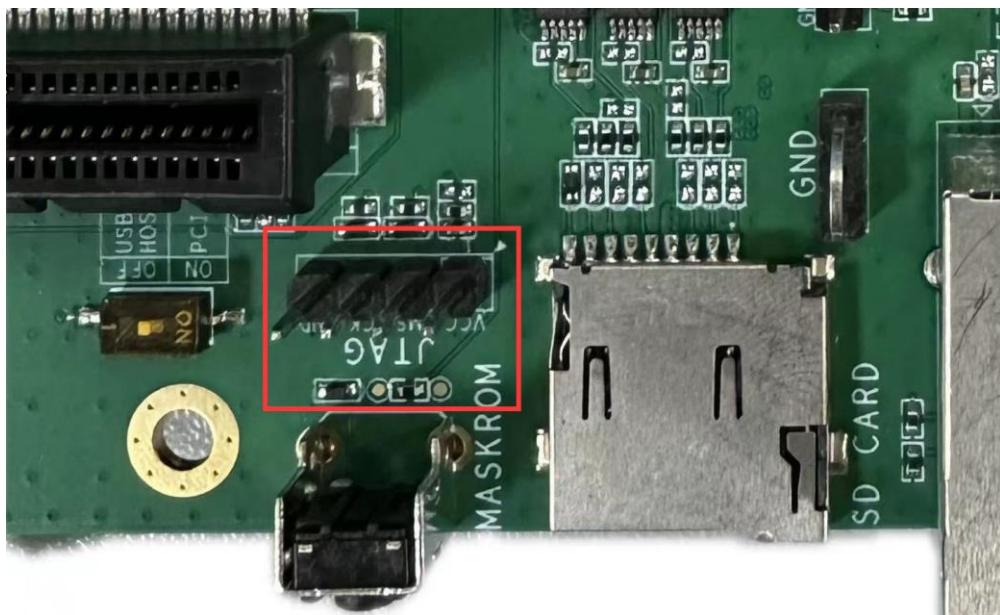


Figure 3-26 JTAG interface

4 Precautions

RK3576 EVB1 is designed for laboratory or engineering environments. Before starting operations, please read the following precautions:

- To prevent electrostatic discharge (ESD) from damaging the development board hardware, take necessary anti-static measures before unpacking the board packaging and during installation.
- When handling the development board, hold it by the edges and avoid touching exposed metal parts to prevent static electricity from damaging the components.
- Please place the development board on a dry and flat surface, away from heat sources, electromagnetic interference sources, radiation sources, and electromagnetic radiation-sensitive devices (e.g., medical equipment).