Pre-Lab 4

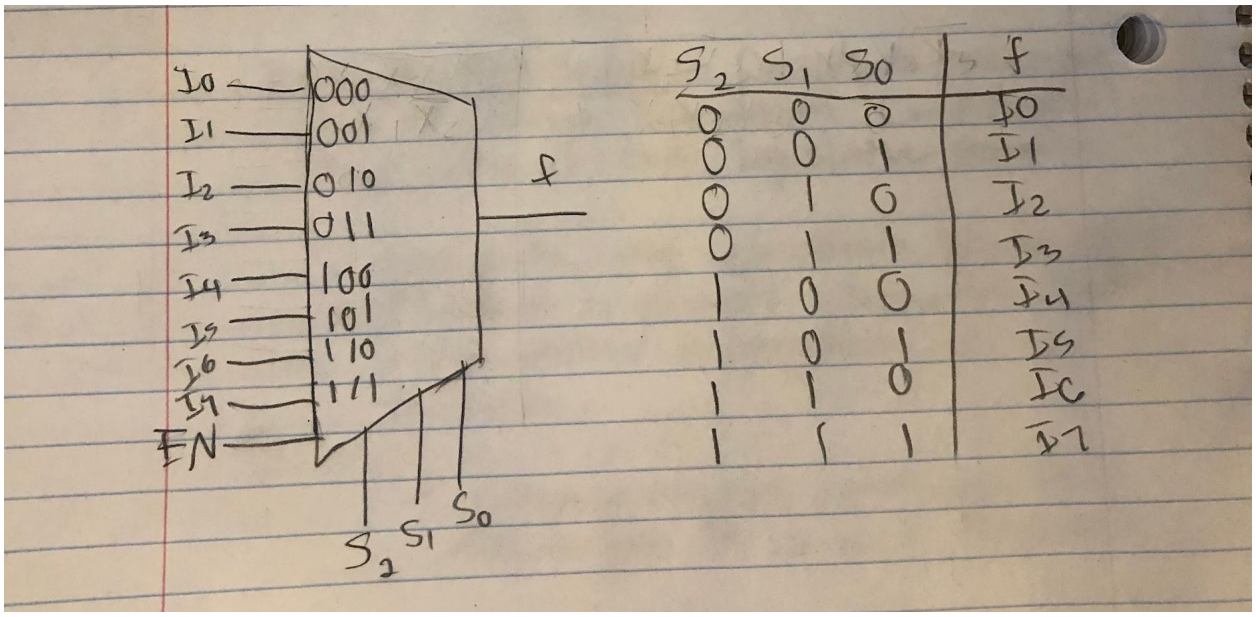
Problem Summary:

The purpose of this lab is to represent an 8 by 1 multiplexer in vivado. The 8 by 1 multiplexer should have eight inputs and one output, and three select lines with an active high enable and output.

Design Approach:

The approach for this lab is to create a mux8to1.sv file that has the 8 by 1 multiplexer, and the mux8to1_tb.sv test bench file to apply values to each input. After creating the 8 by 1 multiplexer, it is implemented with a boolean function using components to connect and pass values with the expression and the multiplexer.

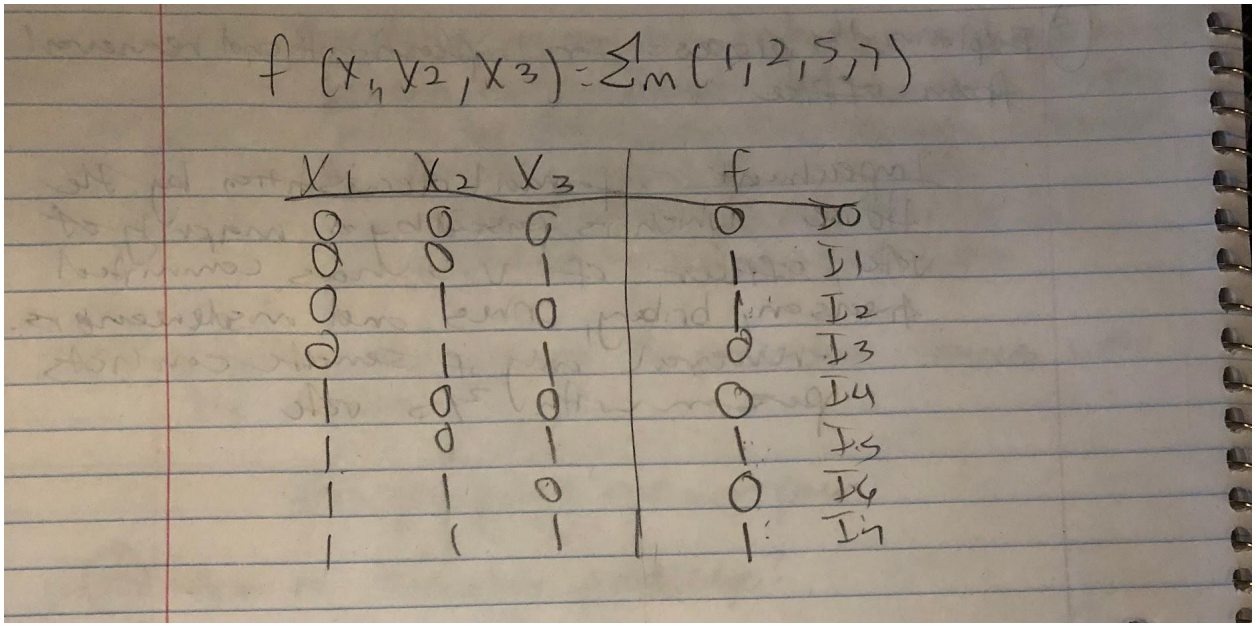
8:1 Multiplexer with Truth Table



The select lines will be s0, s1, and s2, represented in system verilog using the command *input logic [2:0]sel;* to be three bits. The select lines, the three inputs i0 to i7, and the enabler EN, are all inputs. F is the only output where it is equal to one of the inputs i0 to i7.

Next is implementing the boolean expression f(x1,x2,x3) = sum(1,2,5,7).

Boolean Function Truth Table



In vivado, the function is to be passed to the multiplexer, with x1, x2, and x3, as the select lines, and the output of f as the inputs from i0 to i7.