STM32MP15XXAC_1LPDDR2x32

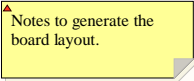# Schematics not complete, only for layout example

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U_STM32MP15XXAC_1LPDDR2x32-Top
STM32MP15XXAC_1LPDDR2x32-Top.SchDoc

Legend

General comment such as function title, configuration, ...

Text to be added to silkscreen.

Warning text.

Notes to generate the board layout.

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Title:	STM32MP15XXAC_1LPDDR2x32-Project	
Project:	STM32MP15XXAC_1LPDDR2x32	
Variant:	Example	
Revision:	A-01	Reference:
Size: A4	Date: 06-JUN-19	Sheet: 1 of 7

life.augmented

U_STM32_MPU_IOs
STM32_MPU_IOs.SchDoc

U_Power_MPU
Power_MPU.SchDoc

U_1LPDDR2_32bits
1LPDDR2_32bits .SchDoc

DDR_A_C
DDR_BYTE0&1
DDR_BYTE2&3

DDR_A_C
DDR_BYTE0&1
DDR_BYTE2&3

PWR_ON

PA0_WKUP

I2C4_SCL
I2C4_SDA
NRST

U_Power_PMIC
Power_PMIC.SchDoc

PWR_ON

PA0_WKUP

I2C4_SCL
I2C4_SDA
NRST

U_eMMC
eMMC.SchDoc

SDMMC2_D[0..7]
SDMMC2_CK
SDMMC2_CMD

eMMC_SDIO2_D[0..7]
eMMC_SDIO2_CK
eMMC_SDIO2_CMD

U1A — STM32MP157CAC3

Pin	Signal		Signal	Pin
AB3	PA0		PC0	AB5
AA4	PA1		PC1	AA6
AC3	PA2		PC2	Y2
U2	PA3		PC3	W2
V4	PA4		PC4	AC7
V3	PA5		PC5	AB7
AC8	PA6		PC6	B14
AB8	PA7		PC7	B11
A13	PA8		PC8	D18
A8	PA9		PC9	D17
Y17	PA10		PC10	D15
AA18	PA11		PC11	D16
AB19	PA12		PC12	D13
N2	PA13		PC13	K2
T2	PA14	PC14-OSC32_IN		L2
C19	PA15	PC15-OSC32_OUT		L1
AB6	PB0		PD0	B8
AA7	PB1		PD1	B9
Y16	PB2		PD2	D12
A11	PB3		PD3	D14
B13	PB4		PD4	B6
Y8	PB5		PD5	A7
Y14	PB6		PD6	D2
D11	PB7		PD7	D10
AB10	PB8		PD8	K3
B10	PB9		PD9	K1
Y3	PB10		PD10	B5
AB1	PB11		PD11	AC10
AC5	PB12		PD12	Y18
AA10	PB13		PD13	AA19
C13	PB14		PD14	L3
B12	PB15		PD15	J2
AC19	OTG_VBUS	JTMS-SWDIO		C20
AB17	USB_DM1	JTCK-SWCLK		B20
AC17	USB_DP1	JTDI		A20
AB16	USB_DM2	JTDO-TRACESWO		A19
AC16	USB_DP2	NJTRST		B19
AB18	USB_RREF			

SDMMC2_D4 (A13/PA8), SDMMC2_D7 (B11/PC7)
SDMMC2_D2 (A11/PB3), SDMMC2_D3 (B13/PB4), SDMMC2_D5 (B10/PB9)
SDMMC2_D0 (C13/PB13), SDMMC2_D1 (B12/PB14)
PA0_WKUP (AB3/PA0)
I2C4_SCL, I2C4_SDA — R37 1K5, R38 1K5 — VDD

U1B — STM32MP157CAC3

Pin	Signal		Signal	Pin
D6	PE0		PG0	AC2
C8	PE1		PG1	W1
Y1	PE2		PG2	V2
C9	PE3		PG3	T4
D19	PE4		PG4	AB2
C11	PE5		PG5	Y6
C10	PE6		PG6	A10
AA11	PE7		PG7	AC14
AC13	PE8		PG8	AB9
AA9	PE9		PG9	Y13
Y15	PE10		PG10	AB11
A4	PE11		PG11	Y7
B4	PE12		PG12	K4
A3	PE13		PG13	AA2
C6	PE14		PG14	AA1
D3	PE15		PG15	B7
D8	PF0	PH0-OSC_IN		P1
A5	PF1	PH1-OSC_OUT		P2
A14	PF2		PH2	AB4
U1	PF3		PH3	AA3
D9	PF4		PH4	B3
D7	PF5		PH5	A2
AA13	PF6		PH6	Y11
AB12	PF7		PH7	W4
AC11	PF8		PH8	D5
AA14	PF9		PH9	C5
Y12	PF10		PH10	C2
Y10	PF11		PH11	C4
Y9	PF12		PH12	B2
Y5	PF13		PH13	D1
AC4	PF14		PH14	C3
Y4	PF15		PH15	B1

SDMMC2_CK (D19/PE4), SDMMC2_D6 (C11/PE5), SDMMC2_CMD (A10/PG6)

U1C — STM32MP157CAC3

Pin	Signal		Signal	Pin
C1	PI0		DSI_D0P	C15
E3	PI1		DSI_D0N	B15
E2	PI2		DSI_D1P	B17
E1	PI3		DSI_D1N	A17
E4	PI4		DSI_CKP	B16
F3	PI5		DSI_CKN	A16
F4	PI6			
L4	PI7			
H4	PI8			
T1	PI9			
P4	PI10			
	PI11			
G3	PZ0		ANA0	U3
G1	PZ1		ANA1	U4
J4	PZ2			
G4	PZ3		PWR_ON	R2
G2	PZ4		NRST	M3
H2	PZ5			
H1	PZ6		PWR_LP	N3
J3	PZ7		PDR_ON	R3
			PDR_ON_CORE	T3
N1	BOOT0		NRST_CORE	M4
N4	BOOT1			
M2	BOOT2		BYPASS_REG1V8	AB13

PWR_ON, NRST

DDR_BYTE_0&1 / U1E — STM32MP157CAC3

DDR_DQ0 (E22), DDR_DQ1 (F22), DDR_DQ2 (H21), DDR_DQ3 (E21), DDR_DQ4 (J21), DDR_DQ5 (J22), DDR_DQ6 (H22), DDR_DQ7 (G21), DDR_DQS0_P (G22), DDR_DQS0_N (G23), DDR_DQM0 (H23)
DDR_DQ8 (T21), DDR_DQ9 (U21), DDR_DQ10 (T22), DDR_DQ11 (W21), DDR_DQ12 (W23), DDR_DQ13 (T23), DDR_DQ14 (W22), DDR_DQ15 (Y21), DDR_DQS1_P (U22), DDR_DQS1_N (U23), DDR_DQM1 (V22)

DDR_CLKP (N22) DDR_CLK_P, DDR_CLKN (N23) DDR_CLK_N
DDR_A0 (L20), DDR_A1 (P22), DDR_A2 (J20), DDR_A3 (K22), DDR_A4 (V20), DDR_A5 (H20), DDR_A6 (W20), DDR_A7 (E20), DDR_A8 (Y20), DDR_A9 (G20)
DDR_A10 (R22), DDR_A11 (R20), DDR_A12 (P23), DDR_A13 (F20), DDR_A14 (R21), DDR_A15 (P20)
DDR_BA0 (L23), DDR_BA1 (U20), DDR_BA2 (M21)

DDR_RASN (N21), DDR_CASN (N20), DDR_CSN (M22), DDR_CKE (T20), DDR_WEN (M20), DDR_ODT (L22), DDR_RESETN (D20)
DDR_VREF (AC20) — C17 100nF — VREF_DDR
DDR_ZQ (K23) — R27 240R 1%
DDR_ATO (Y19), DDR_DTO0 (K20), DDR_DTO1 (L21)

DDR_BYTE_2&3

DDR_DQ16 (B22), DDR_DQ17 (D22), DDR_DQ18 (D23), DDR_DQ19 (B21), DDR_DQ20 (A21), DDR_DQ21 (E23), DDR_DQ22 (D21), DDR_DQ23 (A22), DDR_DQS2_P (C22), DDR_DQS2_N (B23), DDR_DQM2 (C23)
DDR_DQ24 (Y23), DDR_DQ25 (Y22), DDR_DQ26 (AB21), DDR_DQ27 (AB20), DDR_DQ28 (AC22), DDR_DQ29 (AC21), DDR_DQ30 (AA23), DDR_DQ31 (AA22), DDR_DQS3_P (AB22), DDR_DQS3_N (AB23), DDR_DQM3 (AA20)

DDR_A_C, DDR_BYTE0&1, DDR_BYTE2&3

eMMC

SDMMC2_D[0..7]	SDMMC2_D[0..7]
SDMMC2_CMD	SDMMC2_CMD
SDMMC2_CK	SDMMC2_CK

POWER - PMIC

PWR_ON	PWR_ON
NRST	NRST
PA0_WKUP	PA0_WKUP
I2C4_SDA	I2C4_SDA
I2C4_SCL	I2C4_SCL

U1D   STM32MP157CAC3

VDD_CORE

Pin	Signal		Signal	Pin
1A2	VDDCORE	VSS		1A3
1A4	VDDCORE	VSS		1A5
1A6	VDDCORE	VSS		1A7
1B1	VDDCORE	VSS		1B2
1B3	VDDCORE	VSS		1B4
1B5	VDDCORE	VSS		1B6
1C2	VDDCORE	VSS		1B8
1C4	VDDCORE	VSS		1C1
1C6	VDDCORE	VSS		1C3
1D1	VDDCORE	VSS		1C5
1D3	VDDCORE	VSS		1C7
1D5	VDDCORE	VSS		1C9
1D7	VDDCORE	VSS		1D2
1E2	VDDCORE	VSS		1D4
1E4	VDDCORE	VSS		1D6
1E6	VDDCORE	VSS		1D8
1F5	VDDCORE	VSS		1E1
1F7	VDDCORE	VSS		1E3
1G6	VDDCORE	VSS		1E5
1H7	VDDCORE	VSS		1E7
		VSS		1E9
1F3	VDD	VSS		1F2
1G4	VDD	VSS		1F4
1H3	VDD	VSS		1F6
1H5	VDD	VSS		1F8
1J4	VDD	VSS		1G3
1J6	VDD	VSS		1G5
		VSS		1G7
1A8	VDDQ_DDR	VSS		1G9
1B7	VDDQ_DDR	VSS		1H4
1B9	VDDQ_DDR	VSS		1H6
1C8	VDDQ_DDR	VSS		1H8
1D9	VDDQ_DDR	VSS		1J3
1E8	VDDQ_DDR	VSS		1J5
1F9	VDDQ_DDR	VSS		1J7
1G8	VDDQ_DDR	VSS		A1
1H9	VDDQ_DDR	VSS		A23
1J8	VDDQ_DDR	VSS		C7
		VSS		C12
1F1	VBAT	VSS		C21
1J2	VDD_OTP	VSS		D4
		VSS		D4
1H1	VDDA	VSS		F21
R4	VREF+	VSS		H3
		VSS		K21
		VSS		P3
1H2	VSSA	VSS		P21
1G2	VDD_ANA	VSS		V21
B18	VDD_DSI	VSS		W3
		VSS		AA5
AB15	VDDA1V1_REG	VSS		AA8
AB14	VDDA1V8_REG	VSS		AA12
C14	VDDA1V8_DSI	VSS		AA21
C17	VDD1V2_DSI_PHY	VSS		AC1
C18	VDD1V2_DSI_REG	VSS		AC23
		VSS_ANA		1G1
		VSS_DSI		C16
AA15	VDD3V3_USBHS			
AA17	VDD3V3_USBFS	VSS_USBHS		AA16

VDD_CORE: C30 1uF, C75 1uF, C76 1uF, C77 1uF, C35 1uF, C36 1uF, C37 1uF — GND

VDD: C95 1uF, C96 1uF, C47 1uF, C48 1uF, C92 1uF, C94 1uF — GND

VDD2_DDR: C45 1uF, C53 1uF, C54 1uF, C55 1uF, C56 820pF, C57 820pF — GND

VDD2_DDR

C61 100nF

VDD

VDDA — R41 0R — VREF+ — C70 1uF, C50 1uF, C58 10nF

VDD

VDDA_1V8 — C69 2.2uF, C66 100nF, C67 2.2uF, C68 2.2uF

VDD_USB — C71 100nF

U4 — STPMU1A

Signal	Pin
5V_VIN	
BUCK1IN	8
C33 10uF	
PGND1	6

BUCK1 → VOUT1 (5), VLX1 (7)
- L1 1uH
- C34 22uF → VDD_CORE

BUCK2 → VOUT2 (9), VLX2 (11)
- 5V_VIN — BUCK2IN (12), C18 10uF, PGND2 (10)
- L2 1uH
- C29 22uF → VDD2_DDR

BUCK3 → VOUT3 (31), VLX3 (29)
- 5V_VIN — BUCK3IN (28), C31 10uF, PGND3 (30)
- L3 1uH
- C38 22uF → VDD

BUCK4 → VOUT4 (27), VLX4 (25)
- 5V_VIN — BUCK4IN (24), C39 10uF, PGND4 (26)
- L4 1uH
- C40 22uF → 3V3

BOOST
- 5V_VIN — R43 47K — VLXBST (33)
- BYPASS (VIN)
- PGND5 (32)
- BSTOUT (34)
- PWR_USB_SW → VBUSOTG (35)

PWR_SW
- 5V_VIN — SWIN (37)
- SWOUT (38)

VREF = VOUT2 / 2
- GNDLDO (15)
- VREF (16) → VREF_DDR
- C84 1uF

LDO3
- VDD — LDO3IN (13), C42 10uF
- LDO3OUT (14) → VDD1_DDR
- C46 10uF

LDO16IN
- 3V3 — LDO16IN (22), C32 1uF
- LDO1 → LDO1OUT (23)
- LDO6 → LDO6OUT (21)

LDO25IN
- 5V_VIN — LDO25IN (19), C41 1uF
- LDO2 → LDO2OUT (18)
- LDO5 → LDO5OUT (20) → VDDA
- C49 4.7uF

INTLDO / LDO4
- 5V_VIN — VIN (36), C51 4.7uF
- PWR MUX (BSTOUT, VBUSOTG, vin_mux)
- INTLDO → AGND (41), INTLDO (40)
- C43 4.7uF
- LDO4 → LDO4OUT (39) → VDD_USB
- C52 4.7uF
- VDD — VIN

Logic / Control
- VIO (42)
- I2C4_SDA — PZ5 — SDA (3)
- I2C4_SCL — PZ4 — SCL (4)
- PWR_ON — PWRCTRL (44)
- NRST — RSTn (1)
- WAKEUP (2)
- PONKEYn (17)
- NVM
- INTn (43) — PA0 → PA0_WKUP
- EPGND (ep)

B1 SW-PUSH-TS-02H-Blue
- pins 1, 2, 3, 4
- C44 10nF

STPMU1A

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eMMC_SDIO2_D[0..7] eMMC_SDIO2_D[0..7]

3V3

U5

| | | eMMC_SDIO2_D0 | A3 | DAT0 | VCC | E6 |
eMMC_SDIO2_D1 A4 DAT1 VCC F5
eMMC_SDIO2_D2 A5 DAT2 VCC J10
eMMC_SDIO2_D3 B2 DAT3 VCC K9
eMMC_SDIO2_D4 B3 DAT4
eMMC_SDIO2_D5 B4 DAT5 VCCQ N4
eMMC_SDIO2_D6 B5 DAT6 VCCQ C6
eMMC_SDIO2_D7 B6 DAT7 VCCQ M4
VCCQ P3
VCCQ P5

VDD

C78   C79
100nF 2.2uF

VDD

C80   C81
100nF 2.2uF

VDDI C2

C82   C83
100nF 2.2uF

VDD

R40
10K

K5 RSTn

VSSQ C4
VSSQ N2
VSSQ N5
VSSQ P4
VSSQ P6

eMMC_SDIO2_CK   M6 CLK

eMMC_SDIO2_CMD   M5 CMD

VSS A6
VSS E7
VSS G5
VSS H10
VSS J5
VSS K8

H5 DS

THGBMDG5D1LBAIL

DDR_BYTE_0&1

VDD1_DDR (1v8)

VDD2_DDR (1v2)

U2

Signal	Pin	DQ	VDD

DDR_DQ0 N8 DQ0 VDD1 B6
DDR_DQ1 M8 DQ1 VDD1 C1
DDR_DQ2 M7 DQ2 VDD1 R1
DDR_DQ3 M9 DQ3 VDD1 T6
DDR_DQ4 M6 DQ4
DDR_DQ5 L7 DQ5 VDD2 B5
DDR_DQ6 L8 DQ6 VDD2 D2
DDR_DQ7 L9 DQ7 VDD2 G1
DDR_DQS0_P L6 DQS0 VDD2 J7
DDR_DQS0_N L5 DQS0# VDD2 P2
DDR_DQM0 K5 DM0 VDD2 T5

DDR_BYTE0&1

DDR_DQ11 G9 DQ8 VDDCA F1
DDR_DQ9 G8 DQ9 VDDCA H1
DDR_DQ10 G7 DQ10 VDDCA N2
DDR_DQ8 F6 DQ11
DDR_DQ14 F9 DQ12 VDDQ C7
DDR_DQ13 F7 DQ13 VDDQ C10
DDR_DQ12 E8 DQ14 VDDQ D5
DDR_DQ15 E8 DQ15 VDDQ E9
DDR_DQS1_P G6 DQS1 VDDQ F10
DDR_DQS1_N G5 DQS1# VDDQ H6
DDR_DQM1 H5 DM1 VDDQ J6
                   VDDQ K6
                   VDDQ M10
DDR_BYTE_2&3   VDDQ N9
DDR_DQ17 T7 DQ16 VDDQ P5
DDR_DQ23 P6 DQ17 VDDQ R7
DDR_DQ18 T8 DQ18 VDDQ R10
DDR_DQ19 N5 DQ19
DDR_DQ16 P7 DQ20
DDR_DQ21 T9 DQ21 VSS C2
DDR_DQ22 R8 DQ22 VSS C5
DDR_DQ20 N6 DQ23 VSS D1
DDR_DQS2_P P8 DQS2 VSS H2
DDR_DQS2_N P9 DQS2# VSS J8
DDR_DQM2 N7 DM2 VSS P1
                   VSS R2
DDR_DQ29 E6 DQ24 VSS R5
DDR_DQ25 C8 DQ25
DDR_DQ24 B9 DQ26 VSSCA E1
DDR_DQ28 D7 DQ27 VSSCA J1
DDR_DQ27 E5 DQ28 VSSCA N1
DDR_DQ30 B8 DQ29
DDR_DQ26 D6 DQ30 VSSQ C6
DDR_DQ31 B7 DQ31 VSSQ C9
DDR_DQS3_P D8 DQS3 VSSQ D10
DDR_DQS3_N D9 DQS3# VSSQ E10
DDR_DQM3 E7 DM3 VSSQ F5
                   VSSQ G10
DDR_A_C   VSSQ J5
DDR_CLK_P J3 CK VSSQ L10
DDR_CLK_N H3 CK# VSSQ M5
                   VSSQ N10
DDR_A0 P3 CA0 VSSQ P10
DDR_A1 N3 CA1 VSSQ R6
DDR_A2 M3 CA2 VSSQ R9
DDR_A3 M2 CA3
DDR_A4 M1 CA4
DDR_A5 G2 CA5 NC B2
DDR_A6 F2 CA6 NC B3
DDR_A7 F3 CA7 NC J2
DDR_A8 E3 CA8 NC R3
DDR_A9 E2 CA9 NC T2
                   NC T3
DDR_CKE K1 CKE0
         K2 RFU DNU A1
                   DNU A2
DDR_CSN L1 CS0# DNU A9
         L2 RFU DNU A10
                   DNU B1
         D3 ZQ0 DNU B10
         C3 RFU DNU T1
VREF_DDR   DNU T10
         G3 VREFCA DNU U1
         J9 VREFDQ DNU U2
                   DNU U9
         K3 RFU DNU U10
         L3 RFU

EDB4432BBBJ-1D-F-R

R29 240R 1%
C26 100nF C25 100nF
GND GND GND GND

VDD1_DDR
C16 10uF C1 100nF C2 100nF C3 100nF
GND

VDD2_DDR
C15 10uF C4 100nF C5 100nF C6 100nF C7 100nF C8 100nF C9 100nF C10 100nF C11 100nF C12 100nF
GND
To connect to VDD2_DDR power plane

DDR_CLK_P
DDR_CLK_N
R14 100R

DDR_CKE
R26 10K

GND