STM32MP15XXAC_1DDR3Lx16

Schematics not complete, only for layout example

Table of contents

U_STM32MP15XXAC_1DDR3Lx16-Top
STM32MP15XXAC_1DDR3Lx16-Top.SchDoc

Legend

General comment such as function title, configuration, ...

Text to be added to silkscreen.

Warning text.

Notes to generate the
board layout.

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Title:	STM32MP15XXAC_1DDR3Lx16-Project
Project:	STM32MP15XXAC_1DDR3Lx16
Variant:	Example
Revision: A-01	Reference:
Size: A4	Date: 06-JUN-19	Sheet: 1 of 7

life.augmented

U_1DDR3L_16bits
1DDR3L_16bits .SchDoc

DDR_A_C
DDR_BYTE0&1

U_STM32_MPU_IOs
STM32_MPU_IOs.SchDoc

DDR_A_C
DDR_BYTE0&1

PWR_ON
PA0_WKUP
I2C4_SCL
I2C4_SDA
NRST

SDMMC2_D[0..7]
SDMMC2_CK
SDMMC2_CMD

U_Power_MPU
Power_MPU.SchDoc

U_Power_PMIC
Power_PMIC.SchDoc

PWR_ON
PA0_WKUP
I2C4_SCL
I2C4_SDA
NRST

U_eMMC
eMMC.SchDoc

eMMC_SDIO2_D[0..7]
eMMC_SDIO2_CK
eMMC_SDIO2_CMD

U1A — STM32MP157CAC3

Pin	Signal		Signal	Pin
AB3	PA0	PC0	AB5	PA0_WKUP
AA4	PA1	PC1	AA6	
AC3	PA2	PC2	Y2	
U2	PA3	PC3	W2	
V4	PA4	PC4	AC7	
V3	PA5	PC5	AB7	
AC8	PA6	PC6	B14	
AB8	PA7	PC7	B11	SDMMC2_D7
A13	PA8	PC8	D18	SDMMC2_D4
A8	PA9	PC9	D17	
Y17	PA10	PC10	D15	
AA18	PA11	PC11	D16	
AB19	PA12	PC12	D13	
N2	PA13	PC13	K2	
T2	PA14	PC14-OSC32_IN	L2	
C19	PA15	PC15-OSC32_OUT	L1	
AB6	PB0	PD0	B8	
AA7	PB1	PD1	B9	
Y16	PB2	PD2	D12	
A11	PB3	PD3	D14	SDMMC2_D2
B13	PB4	PD4	B6	SDMMC2_D3
Y8	PB5	PD5	A7	
Y14	PB6	PD6	D2	
D11	PB7	PD7	D10	
AB10	PB8	PD8	K3	
B10	PB9	PD9	K1	SDMMC2_D5
Y3	PB10	PD10	B5	
AB1	PB11	PD11	AC10	I2C4_SCL
AC5	PB12	PD12	Y18	I2C4_SDA
AA10	PB13	PD13	AA19	
C13	PB14	PD14	L3	SDMMC2_D0
B12	PB15	PD15	J2	SDMMC2_D1
AC19	OTG_VBUS	JTMS-SWDIO	C20	
AB17	USB_DM1	JTCK-SWCLK	B20	
AC17	USB_DP1	JTDI	A20	
AB16	USB_DM2	JTDO-TRACESWO	A19	
AC16	USB_DP2	NJTRST	B19	
AB18	USB_RREF			

U1B — STM32MP157CAC3

Pin	Signal		Signal	Pin
D6	PE0	PG0	AC2	
C8	PE1	PG1	W1	
Y1	PE2	PG2	V2	
C9	PE3	PG3	T4	SDMMC2_CK
D19	PE4	PG4	AB2	SDMMC2_D6
C11	PE5	PG5	Y6	
C10	PE6	PG6	A10	SDMMC2_CMD
AA11	PE7	PG7	AC14	
AC13	PE8	PG8	AB9	
AA9	PE9	PG9	Y13	
Y15	PE10	PG10	AB11	
A4	PE11	PG11	Y7	
B4	PE12	PG12	K4	
A3	PE13	PG13	AA2	
C6	PE14	PG14	AA1	
D3	PE15	PG15	B7	
D8	PF0	PH0-OSC_IN	P1	
A5	PF1	PH1-OSC_OUT	P2	
A14	PF2	PH2	AB4	
U1	PF3	PH3	AA3	
D9	PF4	PH4	B3	
D7	PF5	PH5	A2	
AA13	PF6	PH6	Y11	
AB12	PF7	PH7	W4	
AC11	PF8	PH8	D5	
AA14	PF9	PH9	C5	
Y12	PF10	PH10	C2	
Y10	PF11	PH11	C4	
Y9	PF12	PH12	B2	
Y5	PF13	PH13	D1	
AC4	PF14	PH14	C3	
Y4	PF15	PH15	B1	

U1C — STM32MP157CAC3

Pin	Signal		Signal	Pin
C1	PI0	DSI_D0P	C15	
E3	PI1	DSI_D0N	B15	
E2	PI2	DSI_D1P	B17	
E1	PI3	DSI_D1N	A17	
E4	PI4	DSI_CKP	B16	
F3	PI5	DSI_CKN	A16	
F2	PI6			
L4	PI7			
H4	PI8			
T1	PI9			
P4	PI10			
	PI11	ANA0	U3	
G3	PZ0	ANA1	U4	
G1	PZ1			
J4	PZ2	PWR_ON	R2	PWR_ON
G4	PZ3	NRST	M3	NRST
G2	PZ4			
H2	PZ5	PWR_LP	N3	
H1	PZ6	PDR_ON	R3	
J3	PZ7	PDR_ON_CORE	T3	
		NRST_CORE	M4	
N1	BOOT0			
N4	BOOT1	BYPASS_REG1V8	AB13	
M2	BOOT2			

U1E — STM32MP157CAC3

DDR_BYTE_0&1

Pin	Signal		Signal	Pin
E22	DDR_DQ0	DDR_CLKP	N22	DDR_CLK_P
F22	DDR_DQ1	DDR_CLKN	N23	DDR_CLK_N
H21	DDR_DQ2	DDR_A0	L20	DDR_A0
E21	DDR_DQ3	DDR_A1	P22	DDR_A1
J21	DDR_DQ4	DDR_A2	J20	DDR_A2
J22	DDR_DQ5	DDR_A3	K22	DDR_A3
H22	DDR_DQ6	DDR_A4	V20	DDR_A4
G21	DDR_DQ7	DDR_A5	H20	DDR_A5
G22	DDR_DQS0P	DDR_A6	W20	DDR_A6
G23	DDR_DQS0N	DDR_A7	E20	DDR_A7
H23	DDR_DQM0	DDR_A8	Y20	DDR_A8
T21	DDR_DQ8	DDR_A9	G20	DDR_A9
U21	DDR_DQ9	DDR_A10	R22	DDR_A10
T22	DDR_DQ10	DDR_A11	R20	DDR_A11
W21	DDR_DQ11	DDR_A12	P23	DDR_A12
W23	DDR_DQ12	DDR_A13	F20	DDR_A13
T23	DDR_DQ13	DDR_A14	R21	DDR_A14
Y21	DDR_DQ14	DDR_A15	P20	
U22	DDR_DQ15	DDR_BA0	L23	DDR_BA0
U23	DDR_DQS1P	DDR_BA1	U20	DDR_BA1
V22	DDR_DQS1N	DDR_BA2	M21	DDR_BA2
B22	DDR_DQM1	DDR_RASN	N21	DDR_RASN
D22	DDR_DQ16	DDR_CASN	N20	DDR_CASN
D23	DDR_DQ17	DDR_CSN	M22	DDR_CSN
B21	DDR_DQ18	DDR_CKE	T20	DDR_CKE
A21	DDR_DQ19	DDR_WEN	M20	DDR_WEN
E23	DDR_DQ20	DDR_ODT	L22	DDR_ODT
D21	DDR_DQ21			
A22	DDR_DQ22	DDR_RESETN	D20	DDR_RESETN
C22	DDR_DQ23			
B23	DDR_DQS2P			
C23	DDR_DQS2N	DDR_VREF	AC20	
	DDR_DQM2			
Y23	DDR_DQ24			
Y22	DDR_DQ25			
AB21	DDR_DQ26			
AB20	DDR_DQ27	DDR_ZQ	K23	
AC22	DDR_DQ28			
AC21	DDR_DQ29			
AA23	DDR_DQ30	DDR_ATO	Y19	
AA22	DDR_DQ31	DDR_DTO0	K20	
AB22	DDR_DQS3P	DDR_DTO1	L21	
AB23	DDR_DQS3N			
AA20	DDR_DQM3			

DDR_A_C

VDD
R37 1K5 R38 1K5
I2C4_SCL
I2C4_SDA

VDD_DDR
R31 1K
R32 1K
C88 100nF
C72 100nF
R27 240R

eMMC

SDMMC2_D[0..7]	SDMMC2_D[0..7]
SDMMC2_CMD	SDMMC2_CMD
SDMMC2_CK	SDMMC2_CK

POWER - PMIC

PWR_ON	PWR_ON
NRST	NRST
PA0_WKUP	PA0_WKUP
I2C4_SDA	I2C4_SDA
I2C4_SCL	I2C4_SCL

VDD_CORE

| C30 | C75 | C76 | C77 | C35 | C36 | C37 |
| 1uF | 1uF | 1uF | 1uF | 1uF | 1uF | 1uF |

GND

VDD

| C95 | C96 | C47 | C48 | C92 | C94 |
| 1uF | 1uF | 1uF | 1uF | 1uF | 1uF |

GND

VDD_DDR

| C45 | C53 | C54 | C55 | C57 | C56 |
| 1uF | 1uF | 1uF | 1uF | 1nF | 1nF |

GND

U1D   STM32MP157CAC3

VDD_CORE

1A2	VDDCORE	VSS	1A3
1A4	VDDCORE	VSS	1A5
1A6	VDDCORE	VSS	1A7
1B1	VDDCORE	VSS	1B2
1B3	VDDCORE	VSS	1B4
1B5	VDDCORE	VSS	1B6
1C2	VDDCORE	VSS	1B8
1C4	VDDCORE	VSS	1C1
1C6	VDDCORE	VSS	1C3
1D1	VDDCORE	VSS	1C5
1D3	VDDCORE	VSS	1C7
1D5	VDDCORE	VSS	1C9
1D7	VDDCORE	VSS	1D2
1E2	VDDCORE	VSS	1D4
1E4	VDDCORE	VSS	1D6
1E6	VDDCORE	VSS	1D8
1F5	VDDCORE	VSS	1E1
1F7	VDDCORE	VSS	1E3
1G6	VDDCORE	VSS	1E5
1H7	VDDCORE	VSS	1E7
		VSS	1E9

VDD

1F3	VDD	VSS	1F2
1G4	VDD	VSS	1F4
1H3	VDD	VSS	1F6
1H5	VDD	VSS	1F8
1J4	VDD	VSS	1G3
1J6	VDD	VSS	1G5
		VSS	1G7

VDD_DDR

1A8	VDDQ_DDR	VSS	1G9
1B7	VDDQ_DDR	VSS	1H4
1B9	VDDQ_DDR	VSS	1H6
1C8	VDDQ_DDR	VSS	1H8
1D9	VDDQ_DDR	VSS	1J3
1E8	VDDQ_DDR	VSS	1J5
1F9	VDDQ_DDR	VSS	1J7
1G8	VDDQ_DDR	VSS	A1
1H9	VDDQ_DDR	VSS	A23
1J8	VDDQ_DDR	VSS	C7
		VSS	C12

| 1F1 | VBAT | VSS | C21 |
| | | VSS | D4 |

VDD

| 1J2 | VDD_OTP | VSS | D21 |
| | | VSS | F21 |

VDDA

| 1H1 | VDDA | VSS | H3 |
| | | VSS | K21 |

VREF+

| R4 | VREF+ | VSS | P3 |
| | | VSS | P21 |

C50 1uF   C97 10nF

C70 1uF

| 1H2 | VSSA | VSS | V21 |
| | | VSS | W3 |

R41 0R

| 1G2 | VDD_ANA | VSS | AA5 |
| | | VSS | AA8 |

VDD

| B18 | VDD_DSI | VSS | AA12 |
| | | VSS | AA21 |

| AB15 | VDDA1V1_REG | VSS | AC1 |
| AB14 | VDDA1V8_REG | VSS | AC23 |

VDDA_1V8

| C14 | VDDA1V8_DSI | VSS_ANA | 1G1 |

C69 2.2uF

| C17 | VDD1V2_DSI_PHY | VSS_DSI | C16 |
| C18 | VDD1V2_DSI_REG |

C66 100nF   C67 2.2uF   C68 2.2uF

VDD_USB

| AA15 | VDD3V3_USBHS | VSS_USBHS | AA16 |
| AA17 | VDD3V3_USBFS |

C71 100nF

C61 100nF

Title: **Power_PMIC**
Project: **STM32MP15XXAC_1DDR3Lx16**
Variant: Example
Revision: A-01
Reference:
Size: A3
Date: 06-JUN-19
Sheet: 5 of 7

eMMC_SDIO2_D[0..7]   eMMC_SDIO2_D[0..7]
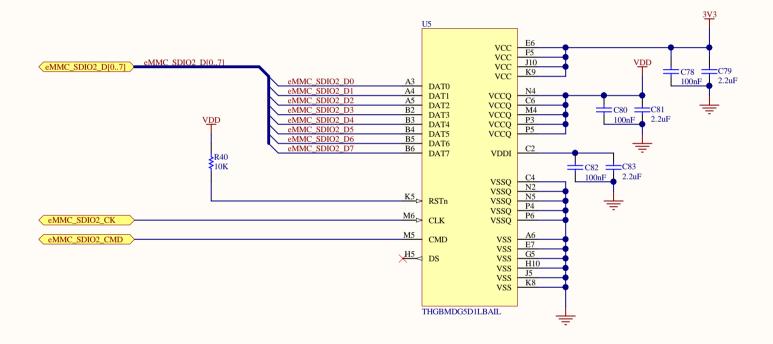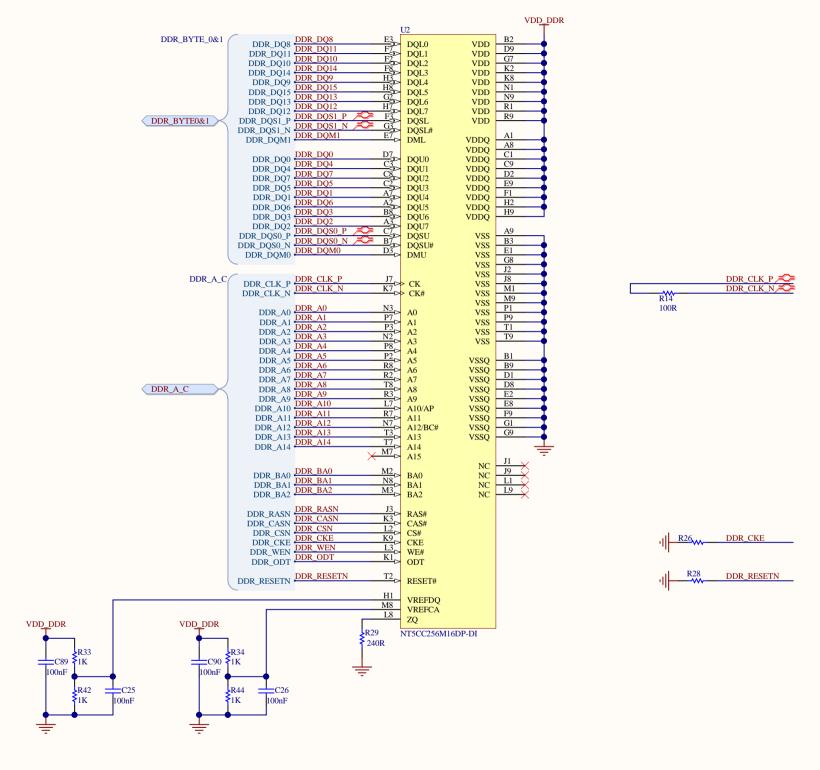
eMMC_SDIO2_D0   A3
eMMC_SDIO2_D1   A4
eMMC_SDIO2_D2   A5
eMMC_SDIO2_D3   B2
eMMC_SDIO2_D4   B3
eMMC_SDIO2_D5   B4
eMMC_SDIO2_D6   B5
eMMC_SDIO2_D7   B6

U5

VCC   E6
VCC   F5
VCC   J10
VCC   K9

DAT0
DAT1
DAT2
DAT3
DAT4
DAT5
DAT6
DAT7

VCCQ   N4
VCCQ   C6
VCCQ   M4
VCCQ   P3
VCCQ   P5

VDDI   C2

VSSQ   C4
VSSQ   N2
VSSQ   N5
VSSQ   P4
VSSQ   P6

VDD

R40
10K

K5   RSTn

eMMC_SDIO2_CK   M6   CLK
eMMC_SDIO2_CMD   M5   CMD
                 H5   DS

VSS   A6
VSS   E7
VSS   G5
VSS   H10
VSS   J5
VSS   K8

THGBMDG5D1LBAIL

3V3

VDD

C78   C79
100nF 2.2uF

C80   C81
100nF 2.2uF

C82   C83
100nF 2.2uF

U2

DDR_BYTE_0&1

Net	Pin	Signal		Signal	Pin

DDR_DQ8 — DDR_DQ8 — E3 — DQL0 — VDD — B2 — VDD_DDR
DDR_DQ11 — DDR_DQ11 — F7 — DQL1 — VDD — D9
DDR_DQ10 — DDR_DQ10 — F2 — DQL2 — VDD — G7
DDR_DQ14 — DDR_DQ14 — F8 — DQL3 — VDD — K2
DDR_DQ9 — DDR_DQ9 — H3 — DQL4 — VDD — K8
DDR_DQ15 — DDR_DQ15 — H8 — DQL5 — VDD — N1
DDR_DQ13 — DDR_DQ13 — G2 — DQL6 — VDD — N9
DDR_DQ12 — DDR_DQ12 — H7 — DQL7 — VDD — R1
DDR_DQS1_P — DDR_DQS1_P — F3 — DQSL — VDD — R9
DDR_DQS1_N — DDR_DQS1_N — G3 — DQSL#
DDR_DQM1 — DDR_DQM1 — E7 — DML — VDDQ — A1

DDR_DQ0 — DDR_DQ0 — D7 — DQU0 — VDDQ — A8
DDR_DQ4 — DDR_DQ4 — C3 — DQU1 — VDDQ — C1
DDR_DQ7 — DDR_DQ7 — C8 — DQU2 — VDDQ — C9
DDR_DQ5 — DDR_DQ5 — C2 — DQU3 — VDDQ — D2
DDR_DQ1 — DDR_DQ1 — A7 — DQU4 — VDDQ — E9
DDR_DQ6 — DDR_DQ6 — A2 — DQU5 — VDDQ — F1
DDR_DQ3 — DDR_DQ3 — B8 — DQU6 — VDDQ — H2
DDR_DQ2 — DDR_DQ2 — A3 — DQU7 — VDDQ — H9
DDR_DQS0_P — DDR_DQS0_P — C7 — DQSU — VSS — A9
DDR_DQS0_N — DDR_DQS0_N — B7 — DQSU# — VSS — B3
DDR_DQM0 — DDR_DQM0 — D3 — DMU — VSS — E1
— VSS — G8
— VSS — J2
DDR_A_C — VSS — J8
DDR_CLK_P — DDR_CLK_P — J7 — CK — VSS — M1
DDR_CLK_N — DDR_CLK_N — K7 — CK# — VSS — M9
— VSS — P1
DDR_A0 — DDR_A0 — N3 — A0 — VSS — P9
DDR_A1 — DDR_A1 — P7 — A1 — VSS — T1
DDR_A2 — DDR_A2 — P3 — A2 — VSS — T9
DDR_A3 — DDR_A3 — N2 — A3
DDR_A4 — DDR_A4 — P8 — A4 — VSSQ — B1
DDR_A5 — DDR_A5 — P2 — A5 — VSSQ — B9
DDR_A6 — DDR_A6 — R8 — A6 — VSSQ — D1
DDR_A7 — DDR_A7 — R2 — A7 — VSSQ — D8
DDR_A8 — DDR_A8 — T8 — A8 — VSSQ — E2
DDR_A9 — DDR_A9 — R3 — A9 — VSSQ — E8
DDR_A10 — DDR_A10 — L7 — A10/AP — VSSQ — F9
DDR_A11 — DDR_A11 — R7 — A11 — VSSQ — G1
DDR_A12 — DDR_A12 — N7 — A12/BC# — VSSQ — G9
DDR_A13 — DDR_A13 — T3 — A13
DDR_A14 — DDR_A14 — T7 — A14
— M7 — A15

DDR_BA0 — DDR_BA0 — M2 — BA0 — NC — J1
DDR_BA1 — DDR_BA1 — N8 — BA1 — NC — J9
DDR_BA2 — DDR_BA2 — M3 — BA2 — NC — L1
— NC — L9

DDR_RASN — DDR_RASN — J3 — RAS#
DDR_CASN — DDR_CASN — K3 — CAS#
DDR_CSN — DDR_CSN — L2 — CS#
DDR_CKE — DDR_CKE — K9 — CKE
DDR_WEN — DDR_WEN — L3 — WE#
DDR_ODT — DDR_ODT — K1 — ODT

DDR_RESETN — DDR_RESETN — T2 — RESET#

H1 — VREFDQ
M8 — VREFCA
L8 — ZQ

R29 240R

NT5CC256M16DP-DI

VDD_DDR
C89 100nF R33 1K R42 1K C25 100nF

VDD_DDR
C90 100nF R34 1K R44 1K C26 100nF

VDD_DDR
C84 100nF C85 100nF C86 100nF C87 100nF
To connect to VDD_DDR power plane

VTT_DDR

DDR_A0 — R1 56R — C1 100nF C2 100nF C3 100nF C4 100nF
DDR_A1 — R2 56R
DDR_A2 — R3 56R
DDR_A3 — R4 56R
DDR_A4 — R5 56R
DDR_A5 — R6 56R
DDR_A6 — R7 56R
DDR_A7 — R8 56R — C5 100nF C6 100nF C7 100nF C8 100nF
DDR_A8 — R9 56R
DDR_A9 — R10 56R
DDR_A10 — R11 56R
DDR_A11 — R12 56R
DDR_A12 — R13 56R
DDR_A13 — R15 56R
DDR_A14 — R16 56R — C9 100nF C10 100nF C11 100nF C12 100nF
DDR_BA0 — R17 56R
DDR_BA1 — R18 56R
DDR_BA2 — R19 56R
DDR_RASN — R20
DDR_CASN — R21 56R
DDR_CSN — R22 56R — C13 22uF C14 22uF
DDR_CKE — R23 56R
DDR_WEN — R24 56R
DDR_ODT — R25 56R

VDD_DDR
C15 10uF C16 10uF C17 100nF C19 100nF C20 100nF C21 100nF C22 100nF C23 100nF C24 100nF

DDR_CLK_P
DDR_CLK_N
R14 100R

R26 — DDR_CKE
R28 — DDR_RESETN