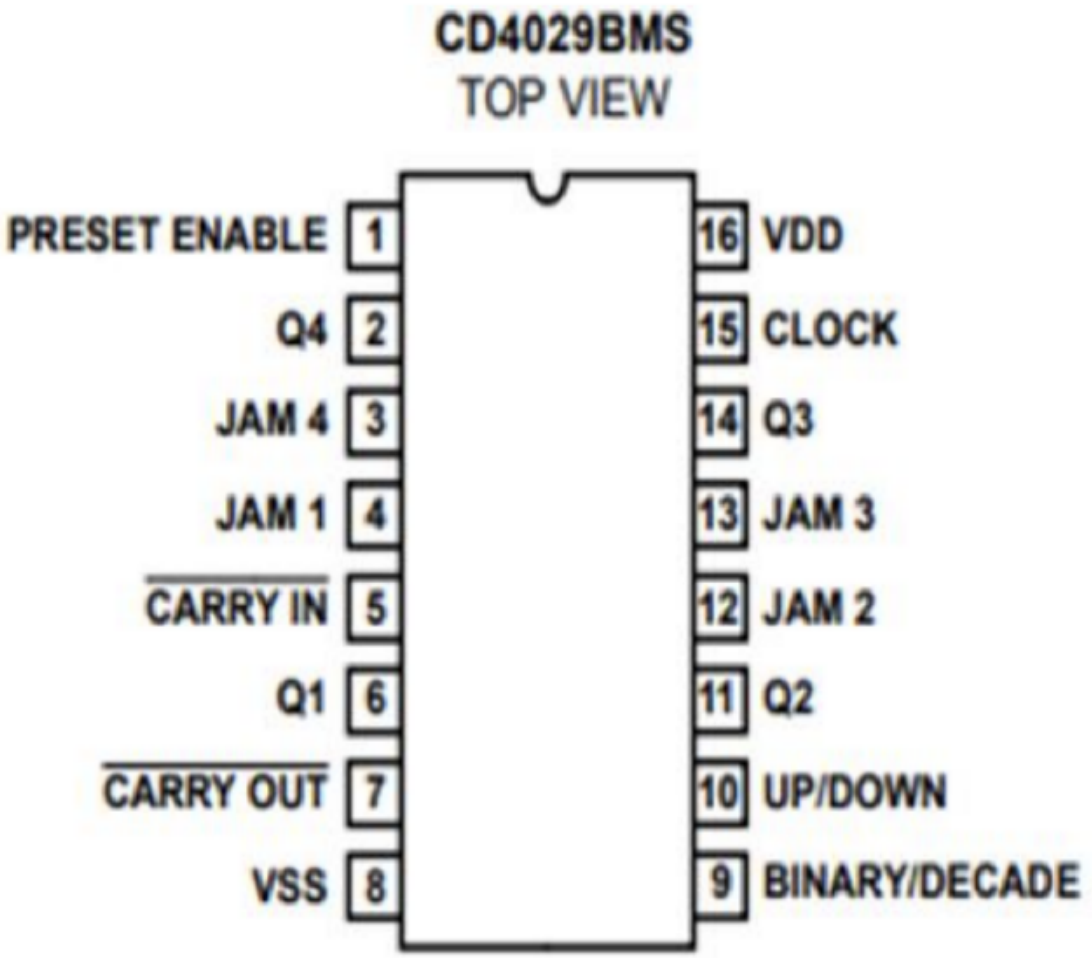
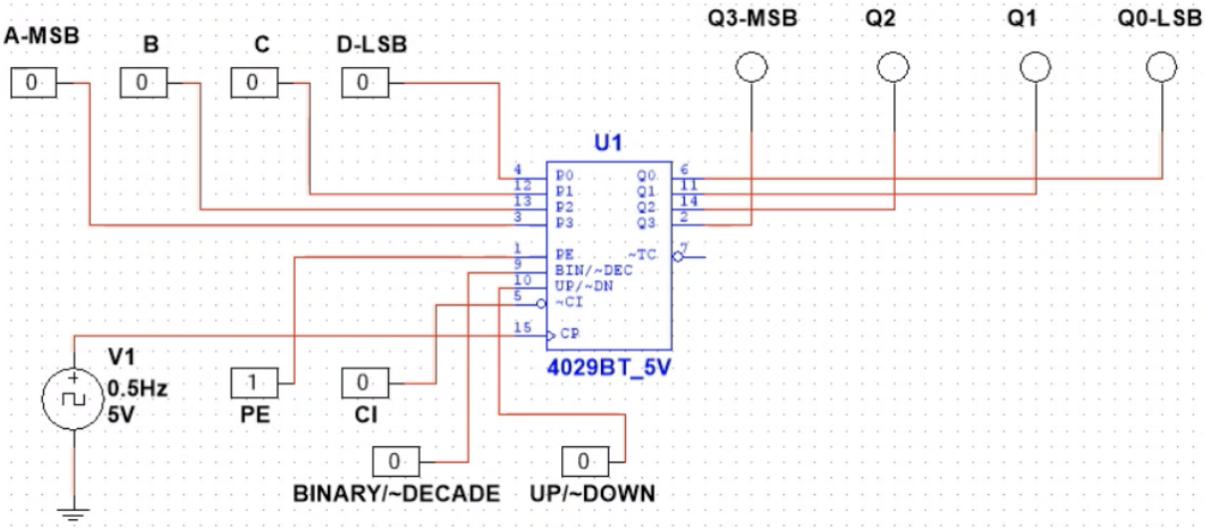
# Experiment 11 :

- ***Aim*** : Design a ROM(8x4) using a decoder, gates and diodes.
- ***Software Used*** : NI Multism 14.2 software.

## PIN Diagram :




## Circuit Diagram :




# Theory :

***Up-Down Counter :***

Counters are used in many different applications. Some count up from zero and provide a change in state of output upon reaching a predetermined value; others count down from a pre-set value to zero to provide an output state change. The counters are synchronous, but they are asynchronously pre settable. In this experiment we will use IC CD 4029 and implement following counter configurations.

1. 4 bit Binary UP Counter
2. 4 bit Binary DOWN Counter
3. 4 bit Binary UP Counter with pre-set value
4. 4 bit Binary Down Counter with pre-set value

# Result :

1. Binary Up Counter (Pin 9 and 10 are connected to 5V)

| Clock | Present Values | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | JAM1 | JAM2 | JAM3 | JAM4 | Cout | Q4 | Q3 | Q2 | Q1 |
| 1 | 0 | 0 | 0 | 1 | 2 | 0 | 0 | 1 | 0 |
| 2 | 0 | 0 | 1 | 0 | 3 | 0 | 0 | 1 | 1 |
| 3 | 0 | 0 | 1 | 1 | 4 | 0 | 1 | 0 | 0 |
| 4 | 0 | 1 | 0 | 0 | 5 | 0 | 1 | 0 | 1 |
| 5 | 0 | 1 | 0 | 1 | 6 | 0 | 1 | 1 | 0 |
| 6 | 0 | 1 | 1 | 0 | 7 | 0 | 1 | 1 | 1 |
| 7 | 0 | 1 | 1 | 1 | 8 | 1 | 0 | 0 | 0 |
| 8 | 1 | 0 | 0 | 0 | 9 | 1 | 0 | 0 | 1 |
| 9 | 1 | 0 | 0 | 1 | 10 | 1 | 0 | 1 | 0 |
| 10 | 1 | 0 | 1 | 0 | 11 | 1 | 0 | 1 | 1 |
| 11 | 1 | 0 | 1 | 1 | 12 | 1 | 1 | 0 | 0 |
| 12 | 1 | 1 | 0 | 0 | 13 | 1 | 1 | 0 | 1 |
| 13 | 1 | 1 | 0 | 1 | 14 | 1 | 1 | 1 | 0 |
| 14 | 1 | 1 | 1 | 0 | 15 | 1 | 1 | 1 | 1 |

2. Binary Down Counter (Pin 9 and 10 are connected to 5V)

| Clock | Present Values | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | JAM1 | JAM2 | JAM3 | JAM4 | Cout | Q4 | Q3 | Q2 | Q1 |
| 1 | 0 | 0 | 0 | 1 | 14 | 1 | 1 | 1 | 0 |
| 2 | 0 | 0 | 1 | 0 | 13 | 1 | 1 | 0 | 1 |
| 3 | 0 | 0 | 1 | 1 | 12 | 1 | 1 | 0 | 0 |
| 4 | 0 | 1 | 0 | 0 | 11 | 1 | 0 | 1 | 1 |
| 5 | 0 | 1 | 0 | 1 | 10 | 1 | 0 | 1 | 0 |
| 6 | 0 | 1 | 1 | 0 | 9 | 1 | 0 | 0 | 1 |
| 7 | 0 | 1 | 1 | 1 | 8 | 1 | 0 | 0 | 0 |
| 8 | 1 | 0 | 0 | 0 | 7 | 0 | 1 | 1 | 1 |
| 9 | 1 | 0 | 0 | 1 | 6 | 0 | 1 | 1 | 0 |
| 10 | 1 | 0 | 1 | 0 | 5 | 0 | 1 | 0 | 1 |
| 11 | 1 | 0 | 1 | 1 | 4 | 0 | 1 | 0 | 0 |
| 12 | 1 | 1 | 0 | 0 | 3 | 0 | 0 | 1 | 1 |
| 13 | 1 | 1 | 0 | 1 | 2 | 0 | 0 | 1 | 0 |
| 14 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |

## Conclusion :

A pre settable up and down counter has been designed successfully.