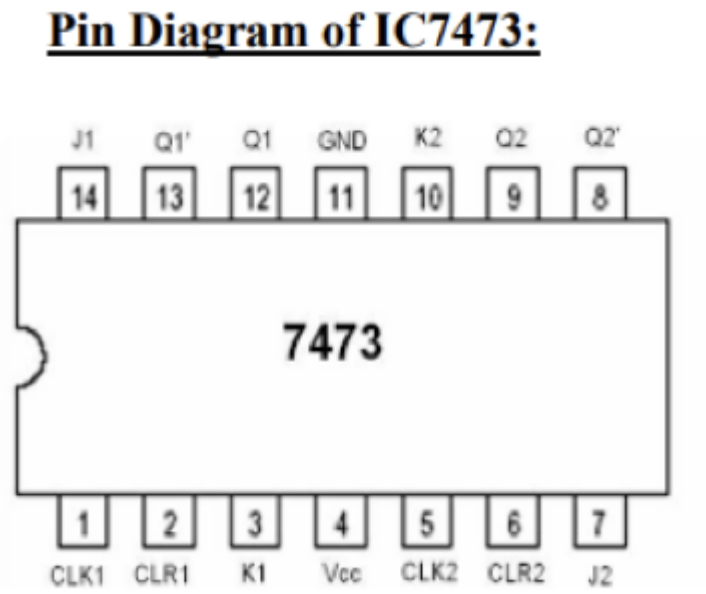
Experiment 9 :

- ***Aim*** : Design and verify the Decade counter
- ***Apparatus Required*** : 1. Trainer Kit (Micro LABORATORY Kit -II) or Wish board, Power supply
- ***Software Used*** : NI Multism 14.2 software.

Pin Diagram :

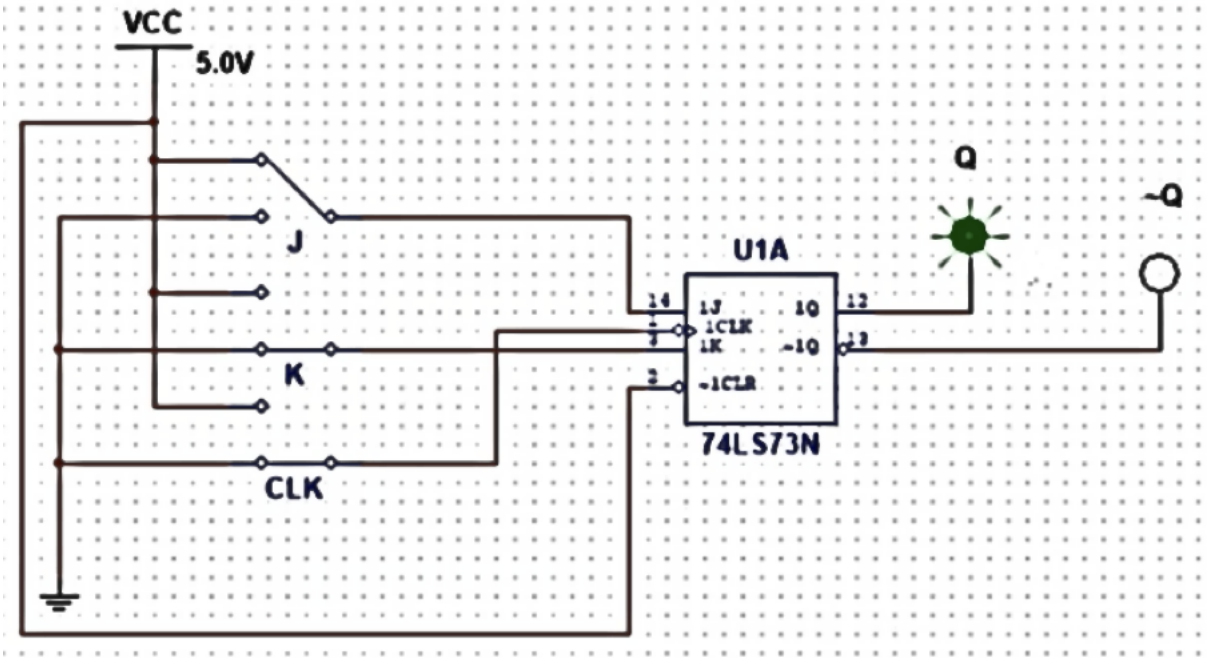


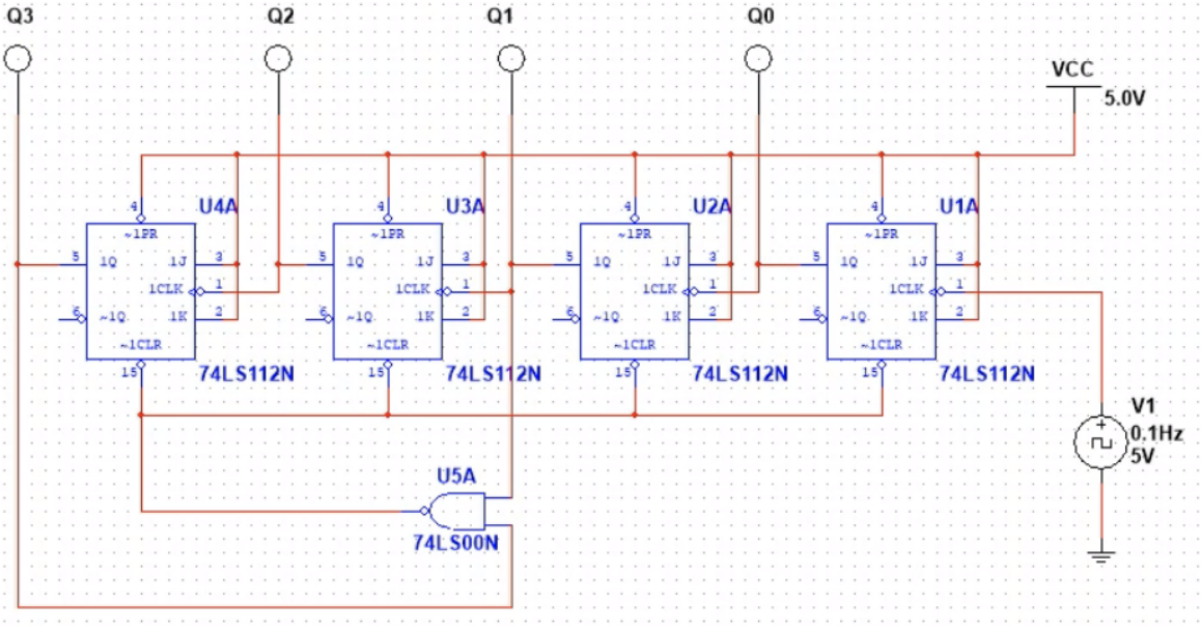
Theory :

J-K flip-flop : A J-K flip-flop has very similar characteristics to an S-R flip-flop. The only difference is that the undefined condition for an S-R flip-flop, i.e., S = R = 1 condition, is also included in this case. Inputs J and K behave like inputs S and R to set and reset the flip-flop respectively. When J = K = 1, the flip-flop is said to be in a toggle state, which means the output switches to its complementary state every time a clock pass. The inherent difficulty of an S-R flip-flop (i.e., S = R = 1) is eliminated by using the feedback connections from the outputs to the inputs of gate 1 and gate 2 as discussed in JK flip-flop. Truth tables JK flip-flop were formed with the assumption that the inputs do not change during the clock pulse (CLK = 1).

Synchronous and asynchronous counter : Counters are circuits made using flip-flops. Synchronous counter, as the name suggests, have all the flip-flops working in sync with clock pulse as well as each other. Here clock pulse is applied to every flip flop. Whereas in Asynchronous counter clock pulse is applied only to the initial flip flop whose value would be considered as LSB. Instead of the clock pulse, the output of first flip-flop acts as a clock pulse to the next flip flop, whose output is used as a clock to the next in line flip-flop and so on. Thus, in Asynchronous counter after the transition of the previous flip flop, the transition of the next flip flop takes place, not at the same time as seen in Synchronous counter.

Circuit Diagram :





Result :

Truth Table of J-K flip flop –

Flip Flop Inputs		Present Output	Next Output
J	K	Q	-Q
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Truth Table of Synchronous and Asynchronous Counter –

Clock Count	Q_D	Q_C	Q_B	Q_A	Decimal Value
1	0	0	0	0	0
2	0	0	0	1	1
3	0	0	1	0	2
4	0	0	1	1	3
5	0	1	0	0	4
6	0	1	0	1	5
7	0	1	1	0	6
8	0	1	1	1	7
9	1	0	0	0	8
10	1	0	0	1	9
11	Counter Resets its Outputs back to Zero				

Conclusion :

Decade counter has been designed and verified successfully.