Weekly Report: Mar. 22 – Mar. 28

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Weekly Report

- Functional correctness of design verified for both batch and stream based processing
- Bugs identified and removed in test bench giving false successful running
- Two versions of testbench each using
  - Randomly generated data in SystemVerilog testbench
  - HLS generated data and comparison against HLS output
- Automatic document generation integration with Travis complete
- Next
  - Integration of HLS simulation with RTL Simulation with automatic data generation for all cases