Weekly Report: Apr. 05 – Apr. 11

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Weekly Report

- All individual tests complete and design functionally correct
- MVAU Stream and Batch Units synthesized to check. No timing violations
- All hold violations removed
- New HLS test benches created to test for special cases of XNOR and 1-bit weight based SIMD processing
- Declaration of signed/unsigned weights generalized in `config.h` through `gen_weigths.py`
- Test flow established for running HLS and RTL simulation/synthesis and comparison of performance. Data extracted and written to a CSV file
- Work on regression testing in progress using the test flow established