# Weekly Report: Mar. 15 – Mar. 21

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# Weekly Report

- Design modified to include input and output valid signals
- Modified design verified (steam based only)
- Automatic documentation generated using **Natural Docs**
- Documentation documents the following:
  - Module/testbench name
  - Inputs/outputs and parameters
  - Internal signals
  - Combinatorial and sequential always blocks
  - Initial blocks
  - Brief description of all
- Integration of document generation with Travis in progress
- Testing of streaming block using data generated by HLS testbench in progress, need more clarification about interpretation of data dumped by HLS testbench needed.