ECSE 323
LAB REPORT 4
Group No.- 20

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g20_YMD_Counter

Objective

To make a circuit (g20_YMD_Counter) that counts up Day, Month and Year for Earth and resets according to specification.

The circuit is required to count up for days, months and years on Earth. It is expected to do so as per regular calendar counting- which necessitated the number of days in a month and the leap year considerations to be made during the circuit implementation. The circuit implements process block with the asynchronous clock and reset signals passed to the sensitivity list. Before implementing the process block, explicit cases for special situations have been outlined. This includes consideration of months with 30 and 31 days, and also leap year. Cases have also been defined for day, month and year reset. The circuit is required to count up to the year 4000.

The main logic of the circuit is implemented in the process block. The block contains asynchronous clock and reset signals passed to its sensitivity list. The circuit is rising edge triggered, implying that changes will only take place during the rising edge of the clock transitions. Following the explicit case definitions made before the declaration of the process block and the commenting made all throughout, the vhdl logic implementation within the block is self-explanatory.

The g20_YMD_Counter circuit has inputs and outputs defined as follows:

- 1-bit asynchronous clock input, specified as ‘clock’
- 1-bit asynchronous reset input, specified as ‘reset’
- Two 1-bit enable inputs, specified as ‘day_count_en’ and ‘load_enable’
- Three load inputs named ‘Y_Set’= 12-bit, ‘M_Set’= 4-bit and ‘D_Set’= 5-bit
- Three outputs named ‘Years’= 12-bit, ‘Months’= 4-bit and ‘Days’= 5-bit

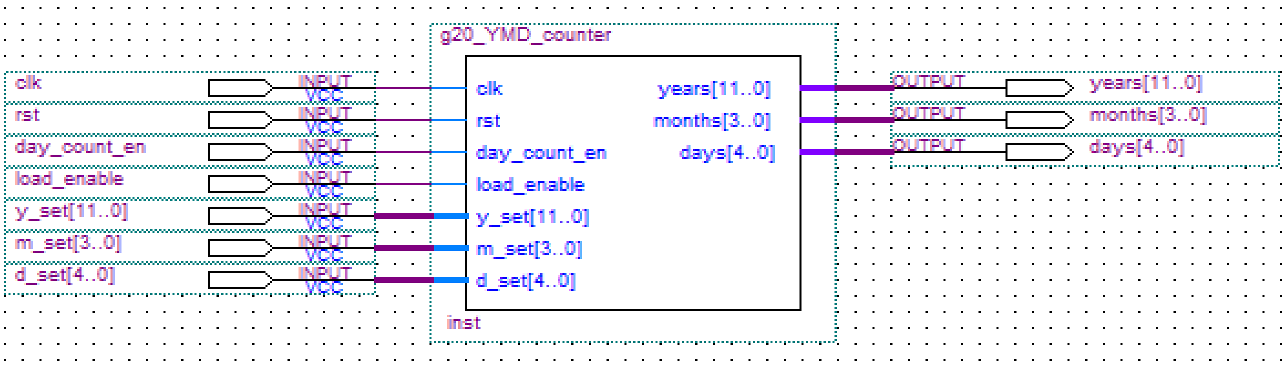


Fig: Higher abstraction for the counter circuit

VHDL description

The VHDL description of the circuit has been attached as a separate file in the zipped folder. The VHDL has been aptly commented to aid the reader in understanding the code.

Circuit testing

A functional simulation has been performed on the counter circuit to validate its operation. Snapshots of its operation for different cases are included in the following.

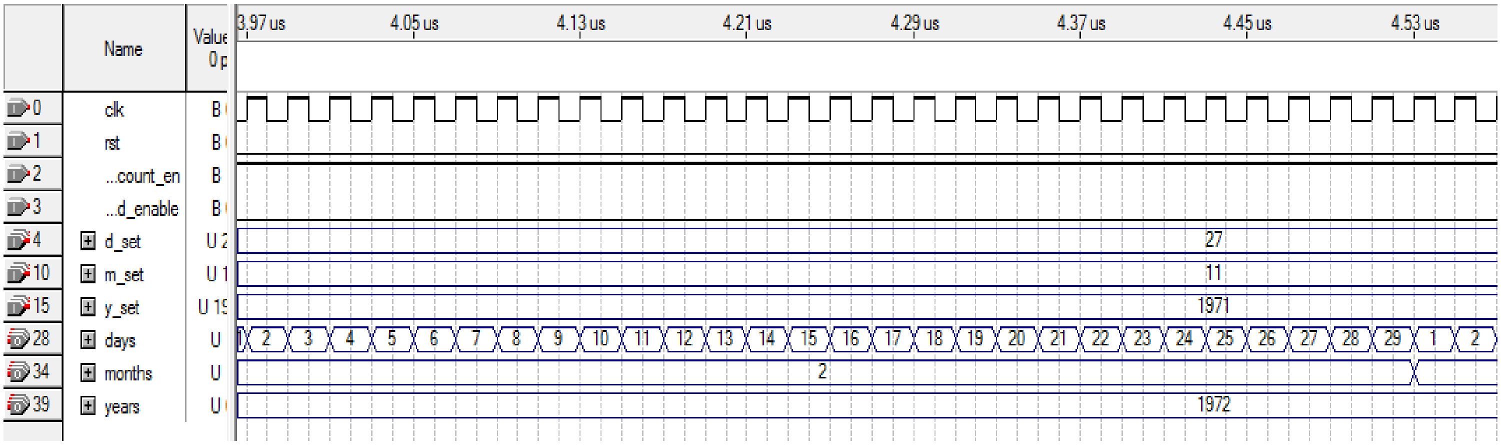


Fig: Waveform showing proper assertion of 29th-day of the 2nd month during a leap year

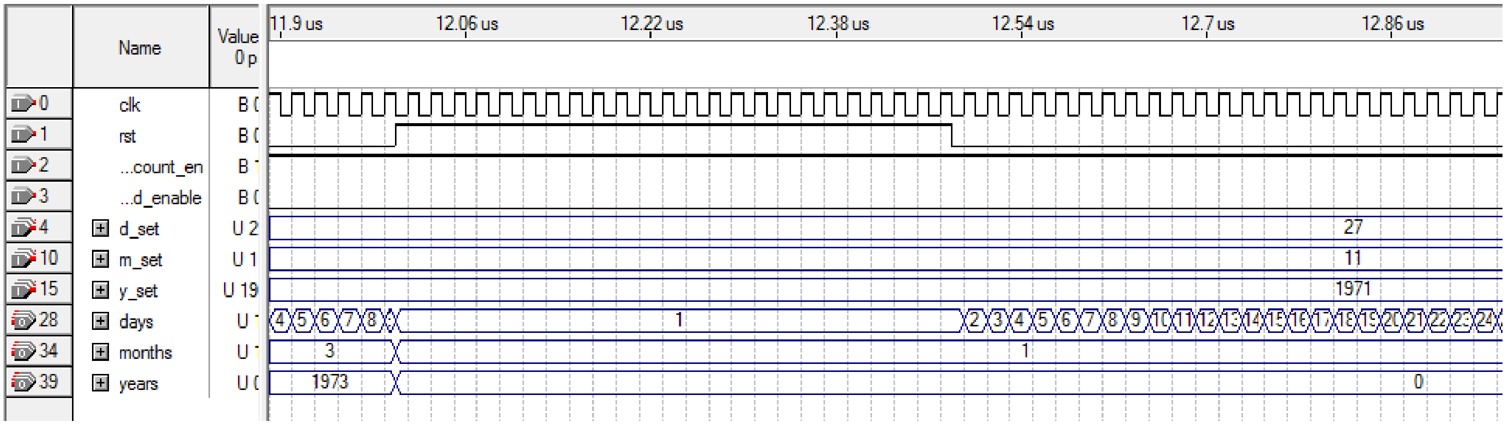


Fig: Waveform showing the respective signals being reset when the input reset signal is asserted

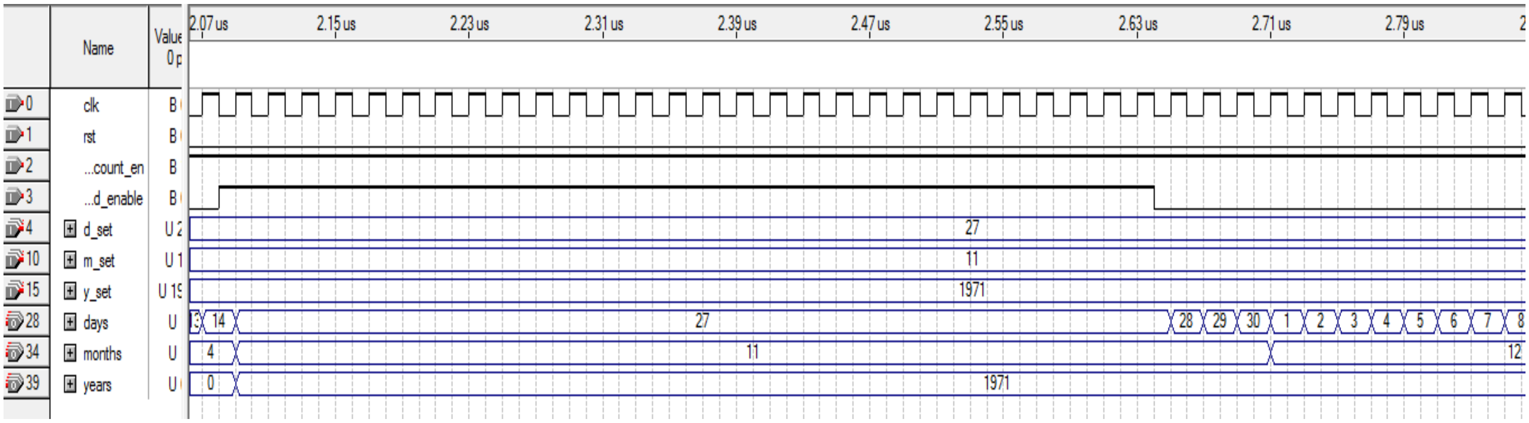


Fig: Waveform showing respective signals loading and holding the corresponding load value for the entire duration when the input load enable signal is asserted

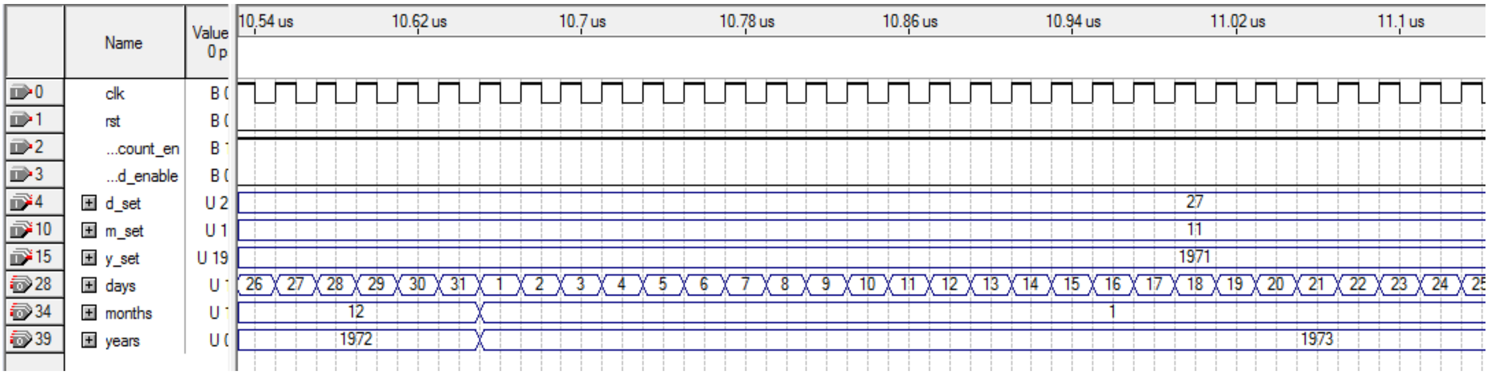


Fig: Waveform showing apt transition between years and both the days and months being reset

For the sake of verifying the validity and the robustness of the counter circuit, a test bed circuit has been implemented. A pin out symbol for the test bed circuit is included in the following to emphasise on the approach taken into testing.

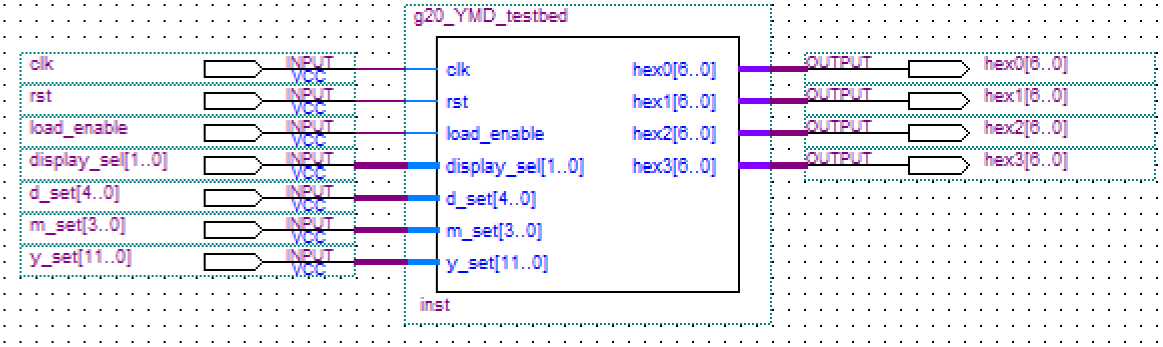


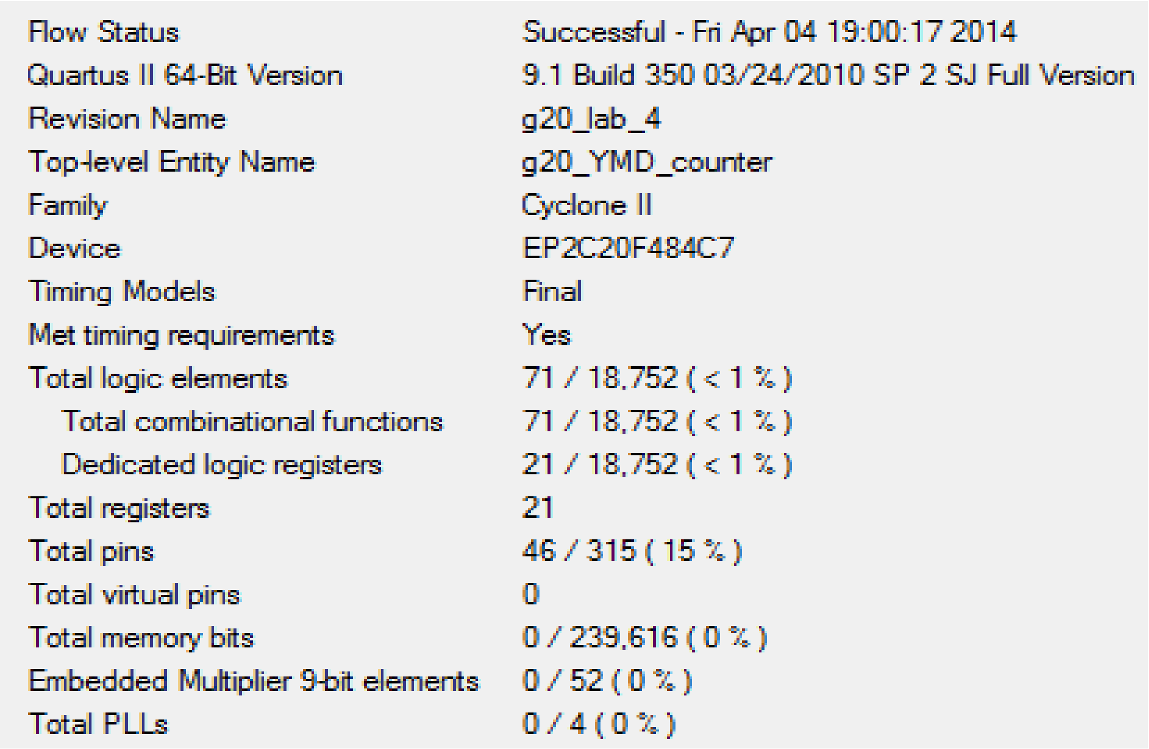
Fig: Higher abstraction for the counter test bed circuit

The inputs to the test bed circuit are the same as the inputs to the basic timer circuit. Besides the test bed circuit also contains a 2-bit input ‘display_sel’ which decides the parameter (year, month or day) to be displayed on the Altera board. The test bed circuit implements

- g20_Basic_Timer: frequency divider circuit that generates unit pulse for day count
- g20_YMD_Counter: counter circuit that counts up day, month and year
- g20_lab2_7_segment_decoder: circuit that enables display on the Altera board

Besides all the regular packages, a custom package has also been imported that implements a conversion method for binary to BCD. Instead of implementing the method in LUT approach using LPM modules, the logic has been explicitly defined in the method.

FPGA Resource Utilization Summary



Flow Status	Successful - Fri Apr 04 19:00:17 2014
Quartus II 64-Bit Version	9.1 Build 350 03/24/2010 SP 2 SJ Full Version
Revision Name	g20_lab_4
Top-level Entity Name	g20_YMD_counter
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Met timing requirements	Yes
Total logic elements	71 / 18,752 (< 1 %)
Total combinational functions	71 / 18,752 (< 1 %)
Dedicated logic registers	21 / 18,752 (< 1 %)
Total registers	21
Total pins	46 / 315 (15 %)
Total virtual pins	0
Total memory bits	0 / 239,616 (0 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)