ECSE 323
LAB REPORT 4
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g20_UTC_to_MTC

Objective

To make a circuit (g20_UTC_to_MTC) that takes in Earth time and date and generates the corresponding Mars time of day.

The circuit is required to calculate the time of day in Mars, given time and date parameters on Earth. The motive behind this circuit implementation is to synchronize both the Earth and Mars clock, i.e. set the Mars clock following the Earth parameters. The implementation of this circuit largely relies on the standardisation discussions and conversion methods stated in the lab slides. The computation of the Mars time involves other modular computations in the process. Notably using the formula given in the lab slides, 'NDays' is computed in a process block that takes asynchronous clock and reset signals in the sensitivity list. This variable represents the number of times the YMD counter gets incremented. Another variable 'day_frac' which is the day-fraction representation of seconds is computed using one of the previously built lab modules (g20_Seconds_to_Days). Following computation of each of these variables the corresponding Julian Date is evaluated. The circuit finally implements LPM multiplication and add-sub module to extract the hours, minutes and seconds components of MTC, followed by a process block implementation to latch the extracted outputs. The computation primarily employs concepts of fixed point arithmetic. A 1-bit output 'done' is asserted when the operation completes.

The g20_UTC_to_MTC circuit has inputs and outputs defined as follows:

- 1-bit asynchronous clock input, specified as 'clock'
- 1-bit asynchronous reset input, specified as 'reset'
- Three load inputs named 'earth_year'= 12-bit, 'earth_month'= 4-bit and 'earth_day'= 5-bit
- Three load inputs named 'earth_hour'= 5-bit, 'earth_min'= 6-bit and 'earth_sec'= 6-bit
- Three load outputs named 'mars_hour'= 5-bit, 'mars _min'= 6-bit and 'mars _sec'= 6-bit
- 1-bit output named 'done'

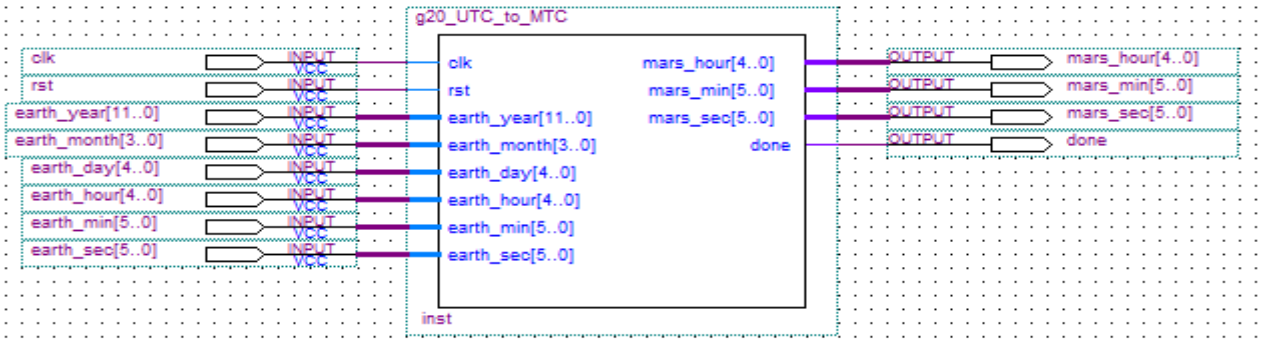

Fig: Higher abstraction for the converter circuit

The previous lab and lpm modules implemented in this circuit are given in the following:

- g20_HMS_Counter
- g20_YMD_Counter
- g20_HMS_to_sec
- g20_Seconds_to_Days
- lpm_mult and lpm_add_sub

VHDL description

The VHDL description of the circuit has been attached as a separate file in the zipped folder. The VHDL has been aptly commented to aid the reader in understanding the code.

Relevant formula

The formula used in calculation has mostly been taken from the lab slides. Notably, the formula have been modified to involve multiplication processes, since division operations are costlier in terms of implementation overhead.

Computing the Julian Date: $JD_{2000} = NDays.Dayfrac$

Computing the MTC: $MTC = 24 * Frac\left[JD_{2000} * 0.973244297 - 0.00072\right]$

Where:

- NDays- number of times the YMD counter gets incremented
- Dayfrac- day fraction representation of 'Nsecs' which represents the number of times HMS is incremented

Circuit testing

A functional circuit has been performed on the counter circuit to validate its operation. A snapshot of its operation is included in the following. Sample values used for testing purpose are Y:M:D:H:M:S = 2000:1:6:0:4:33. The result obtained has been compared with an online converter app and also computed by hand to validate the operation of the circuit. As previously mentioned, the signal 'done' is duly asserted once the circuit operation completes and an output value is extracted.

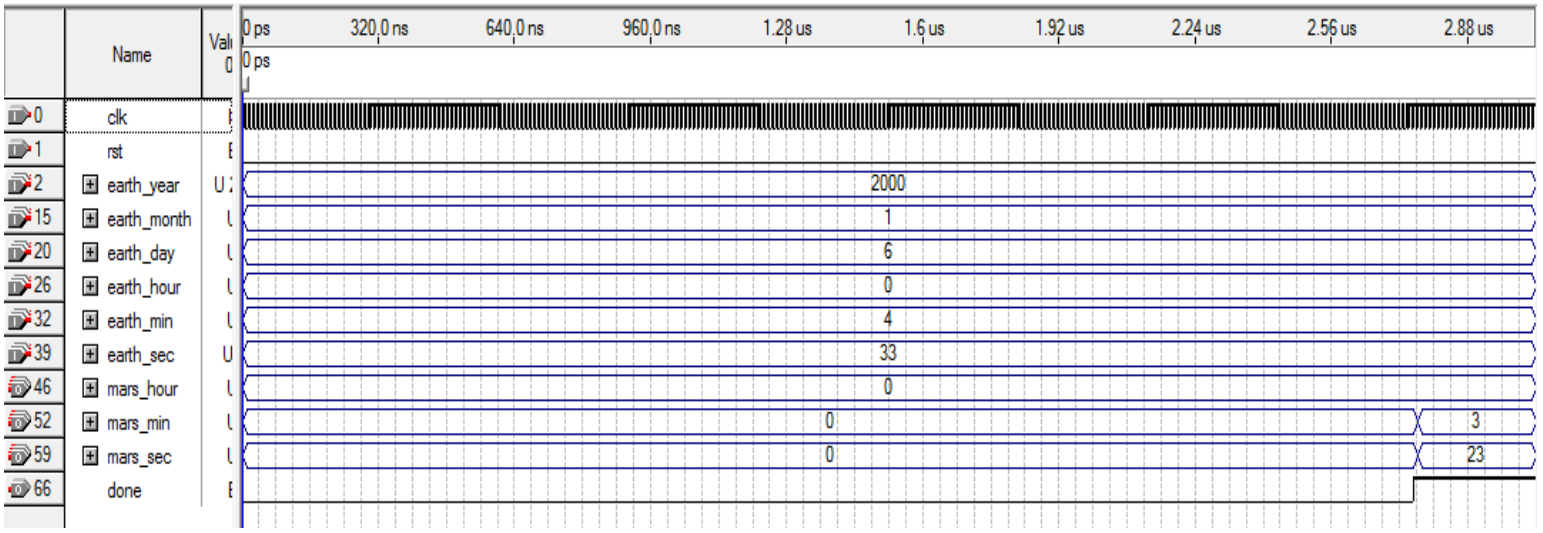

Fig: Waveform showing outputs aptly changing in response to the input Y:M:D:H:M:S parameters

FPGA Resource Utilization Summary

Flow Status	Successful - Fri Apr 04 21:32:16 2014
Quartus II 64-Bit Version	9.1 Build 350 03/24/2010 SP 2 SJ Full Version
Revision Name	g20_lab_4
Top-level Entity Name	g20_UTC_to_MTC
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Met timing requirements	Yes
Total logic elements	0 / 18,752 (0 %)
Total combinational functions	0 / 18,752 (0 %)
Dedicated logic registers	0 / 18,752 (0 %)
Total registers	0
Total pins	58 / 315 (18 %)
Total virtual pins	0
Total memory bits	0 / 239,616 (0 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)