ECSE 323
LAB REPORT 3
Group No.- 20
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g20_Basic_Timer

Objective

To make a circuit (g20_Basic_Timer) that acts as a frequency divider and provides an output pulse at each second.

The circuit is implemented following the schematic provided in the lab slides. An LPM down counter module is used to count down from a constant value and set the counter output signal high once the count reaches 0. The circuit is sequential, hence the output has been fed back to the input in order to reset the counter (start over counting down to 0). Hence, counter reset is asserted by implementing OR operation of the 'reset' input signal with the counter output/feedback signal. An LPM constant module has been used to feed in a constant value (of specific bits) to the circuit (the constant value to count down from). The calculation for the constant value is given below.

The g20_Basic_Timer has three inputs and two outputs:

- 1-bit clock input, specified as 'clock'
- 1-bit counter reset input, specified as 'reset'
- 1-bit counter enable input, specified as 'enable'
- Two 1-bit outputs named EPULSE and MPULSE

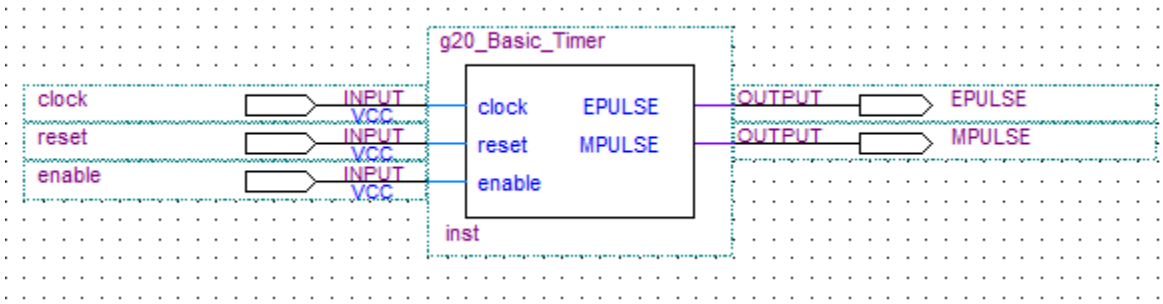


Fig: Higher abstraction for the timer circuit

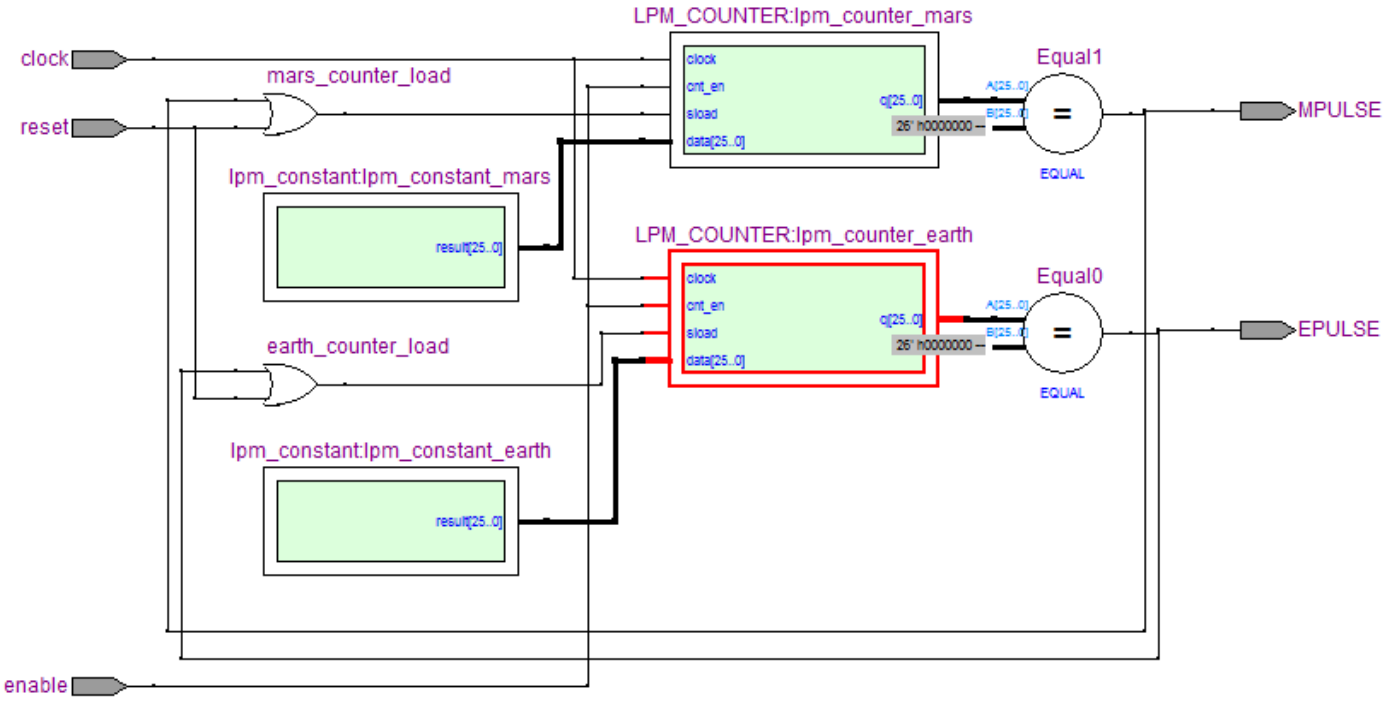


Fig: Schematic for the timer circuit

Constant calculation

$$Period = (N + 1) * Tc$$

For earth: Period = 1, Tc = 20ns [=(50 MHz)$^{-1}$] => N = 49, 999, 999 => 26 bits

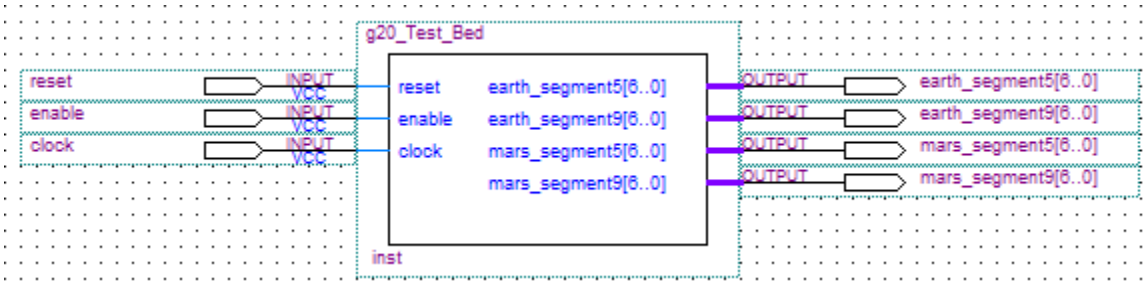
For mars: Period = 1.027 491 252, Tc = 20ns [=(50 MHz)$^{-1}$] => N = 51, 374, 562 => 26 bits

VHDL description

The VHDL description of the circuit has been attached as a separate file in the zipped folder. The LPM module declarations have been initially implemented using the megafunction wizard. However, for later purposes module declarations have been done directly using the LPM documentation found online. The VHDL has been aptly commented to aid the reader in understanding the code.

Circuit testing

For the sake of verifying the validity and the robustness of the timer circuit, a test bed circuit has been implemented. A pinout symbol for the circuit is included in the following to aid the approach taken into testing.



The inputs to the test bed circuit are the same as the inputs to the basic timer circuit. Besides the basic timer circuit, the test bed circuit also implements the 7 segment decoder module prepared in one of the previous labs. The output produced by the basic timer circuit is passed to a cascade of 0-9 and 0-5 counters. Each of the output of the counter is fed as input to the decoder circuit for purpose of LED display on the Altera board.

Initially, a timing simulation of the basic timer circuit has been carried out to output a single pulse. The diagram clearly shows the value of MPULSE being greater than that of EPULSE (by 1.027 times). For the purpose of carrying out the simulation, the LPM constant value and the corresponding bit resolution have been decreased to shorten the testing time.

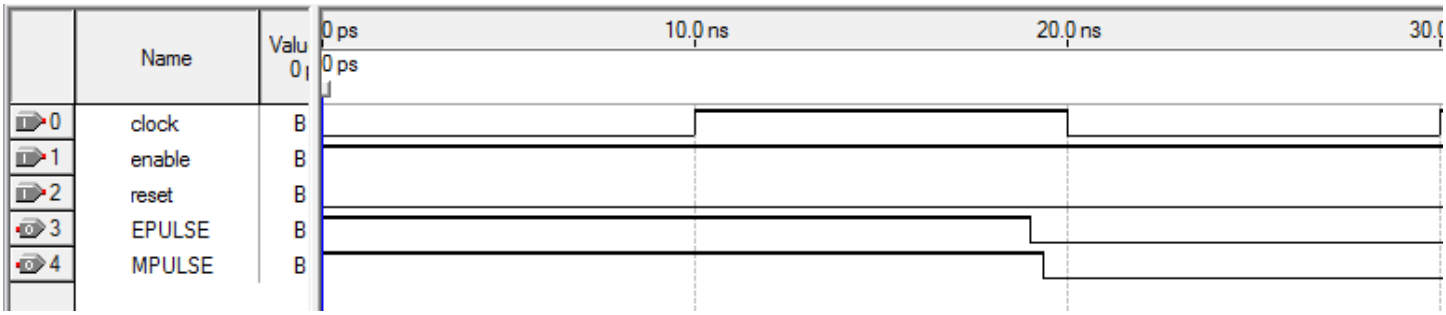


Fig: Waveform for the basic timer circuit

Following the implementation of the timer test bed circuit, another timing simulation has been carried out. Again the constant value and the corresponding bit resolution have been decreased for the same reason as before. The reset signal has been intentionally asserted at places to check whether the clock resets duly.

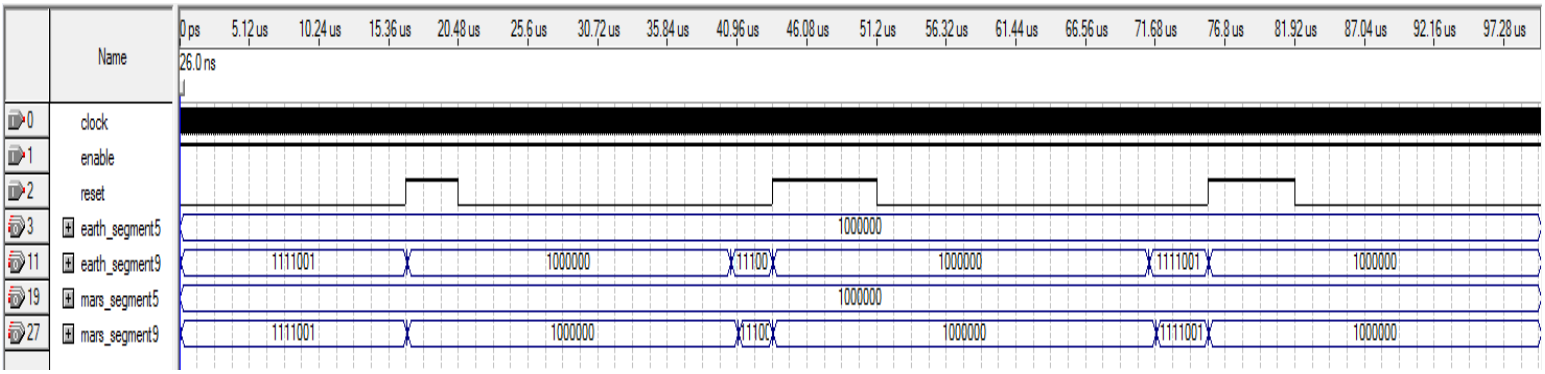


Fig: Waveform for the timer test bed circuit

Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From	To	From Clock	To Clock	Failed Paths
1	Worst-case tsu	N/A	None	2.300 ns	reset	lpm_counter:lpm_counter_earth|cntr_1rk:auto_generated|s...	--	clock	0
2	Worst-case tco	N/A	None	12.575 ns	lpm_counter:lpm_counter_earth|...	EPULSE	clock	--	0
3	Worst-case tpd	N/A	None	2.810 ns	altera_internal_jtag~TDO	altera_reserved_tdo	--	--	0
4	Worst-case th	N/A	None	1.753 ns	altera_internal_jtag~TDIUTAP	sld_hub:auto_hub|irsr_reg[8]	--	altera_internal_jtag~TCKUTAP	0
5	Clock Setup: 'altera_internal_jtag~TCKUTAP'	N/A	None	123.95 MHz (period = 8.068 ns)	sld_hub:auto_hub|irf_reg[1][1]	sld_hub:auto_hub|tdo	altera_internal_jtag~TCKUTAP	altera_internal_jtag~TCKUTAP	0
6	Clock Setup: 'clock'	N/A	None	Restricted to 195.01 MHz (period = 5.128 ns)	sld_signaltap:auto_signaltap_0|s...	sld_signaltap:auto_signaltap_0|sld_signaltap_impl:sld_signa...	clock	clock	0
7	Total number of failed paths								0

Fig: Timing analyzer summary for the basic timer circuit

Flow Status	Successful - Fri Mar 21 19:19:11 2014
Quartus II 64-Bit Version	9.1 Build 350 03/24/2010 SP 2 SJ Full Version
Revision Name	g20_lab3
Top-level Entity Name	g20_Basic_Timer
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Met timing requirements	Yes
Total logic elements	733 / 18,752 (4 %)
Total combinational functions	452 / 18,752 (2 %)
Dedicated logic registers	600 / 18,752 (3 %)
Total registers	600
Total pins	5 / 315 (2 %)
Total virtual pins	0
Total memory bits	2,816 / 239,616 (1 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)

Fig: Flow summary for the basic timer circuit

Analysis & Synthesis Status	Successful - Fri Mar 21 19:18:55 2014
Quartus II 64-Bit Version	9.1 Build 350 03/24/2010 SP 2 SJ Full Version
Revision Name	g20_lab3
Top-level Entity Name	g20_Basic_Timer
Family	Cyclone II
Total logic elements	768
Total combinational functions	450
Dedicated logic registers	600
Total registers	600
Total pins	5
Total virtual pins	0
Total memory bits	2,816
Embedded Multiplier 9-bit elements	0
Total PLLs	0

Fig: Analysis and synthesis summary for the basic timer circuit

Propagation delay of EPULSE = 19.05ns – 10ns = 9.05ns

Propagation delay of MPULSE = 19.4ns – 10 ns = 9.4ns