ECSE 323
LAB REPORT 1
Group No.- 20
Aditya Saha- 260453165
Shayan Ahmad- 260350431

# g20_Seconds_to_Days

## Objective

To make a circuit (g20_Seconds_to_Days) that converts a time of day in seconds to a day fraction representation

The Seconds to Days converter circuit is a combinational circuit that shifts an input vector by a certain number of bit positions and adds subsequently. This version of the circuit only shifts to the left. The bits on the right are added as zeros. The circuit was built using 9 adders and 9 shifters. The function implemented by the circuit is : d = (N*2^23 + N*2^22 + N*2^17 + N*2^13 + N*2^11 + N*2^10 + N*2^9 + N*2^6 + N*2^2+ N)/2^40; where N represents time of day in seconds and d represents day fraction.

The Seconds-to-Days circuit has one input and one output:

- 17 bits input called seconds (pin named Seconds in the diagram), representing the original vector being added and shifted simultaneously
- 40 bits output called day_fraction (pin named Days in the diagram), representing the final output of the circuit

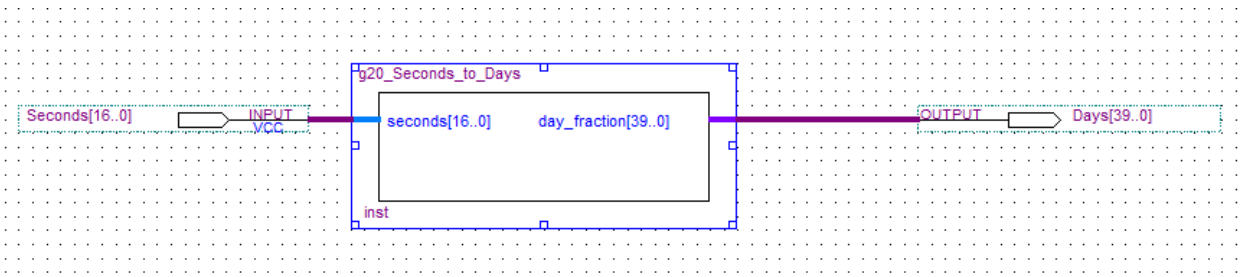



Fig: Higher abstraction for the converter circuit

## VHDL description

```
1  -- Converts a time of day in seconds to a day fraction representation
2  --
3  -- entity name: g20_Seconds_to_Days
4  --
5  -- Copyright (C) 2014 Aditya Saha- 260453165,
6  --                    Shayan Ahmad- 260350431
7  -- Version 1.0
8  -- Author: Aditya Saha- aditya.saha@mail.mcgill.ca,
9  --         Shayan Ahmad- shayan.ahmad@mail.mcgill.ca
10 -- Date: 24th January 2014
11
12 library ieee; -- allows use of the std_loginc_vector type
13 use ieee.std_logic_1164.all;
14 use ieee.numeric_std.all;
15
16 entity g20_Seconds_to_Days is
17     port ( seconds  : in unsigned(16 downto 0);
18            day_fraction : out unsigned(39 downto 0) );
19 end g20_Seconds_to_Days;
20
21 architecture behavior1 of g20_Seconds_to_Days is
22     signal adder1: unsigned(19 downto 0);
23     signal adder2: unsigned(23 downto 0);
24     signal adder3: unsigned(26 downto 0);
25     signal adder4: unsigned(27 downto 0);
26     signal adder5: unsigned(28 downto 0);
27     signal adder6: unsigned(30 downto 0);
28     signal adder7: unsigned(34 downto 0);
29     signal adder8: unsigned(39 downto 0);
30     signal adder9: unsigned(39 downto 0);
31
32 begin
33     adder1 <= seconds +("0" & seconds & "00");
34     adder2 <= adder1 + ("0" & seconds & "000000");
35     adder3 <= adder2 + ("0" & seconds & "000000000");
36     adder4 <= adder3 + ("0" & seconds & "0000000000");
37     adder5 <= adder4 + ("0" & seconds & "00000000000");
38     adder6 <= adder5 + ("0" & seconds & "0000000000000");
39     adder7 <= adder6 + ("0" & seconds & "00000000000000000");
40     adder8 <= adder7 + ("0" & seconds & "0000000000000000000000");
41     adder9 <= adder8 + (seconds & "000000000000000000000000");
42     day_fraction <= adder9;
43 end behavior1;
44
```

## Circuit testing

The original input vector is unshifted. This input is subsequently shifted and finally the shifted output vector results. The circuit is run for eight different inputs (including the boundary values), and for each case the corresponding output is noted. The simulation diagram verifies that the circuit works correctly.

Test cases used- Boundary conditions (0 & 86400), 3600, 7200, 1800, 4800, 6000 and 8000

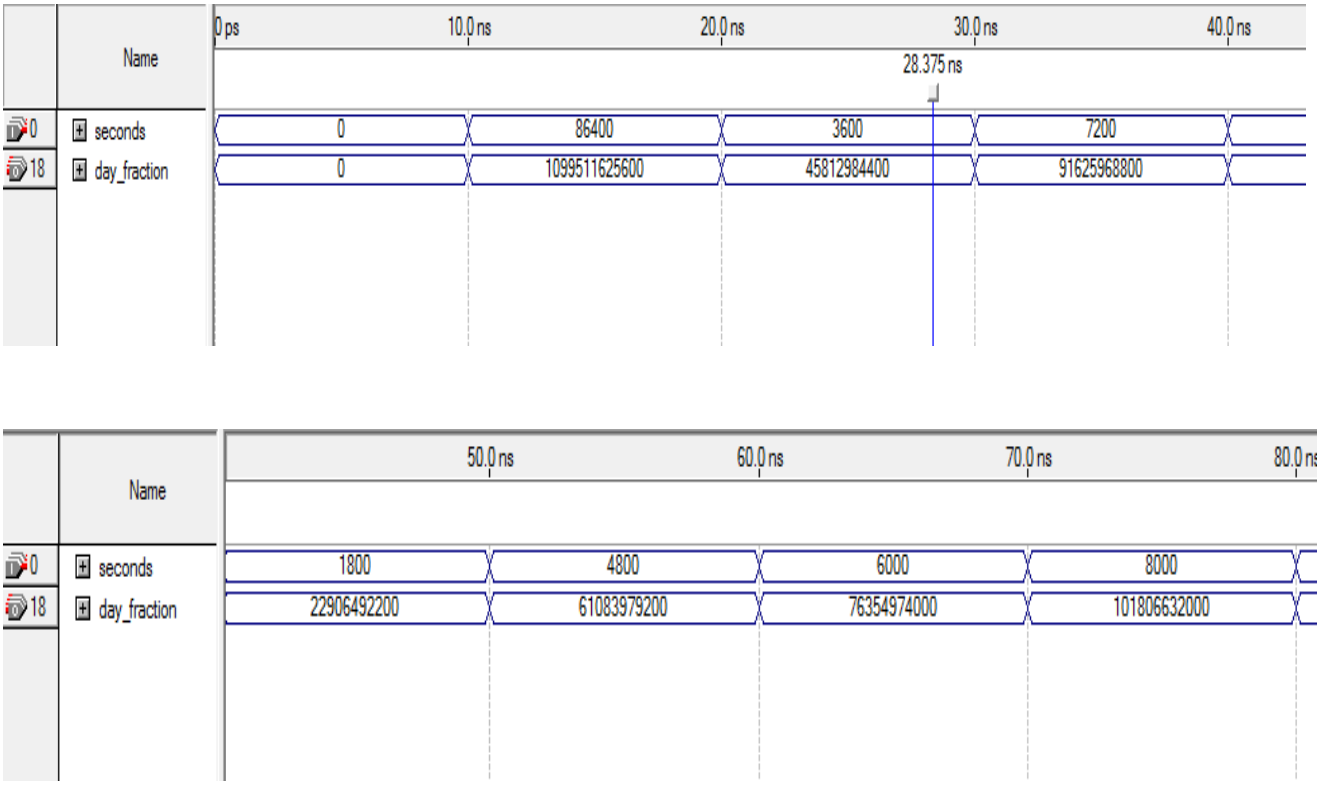
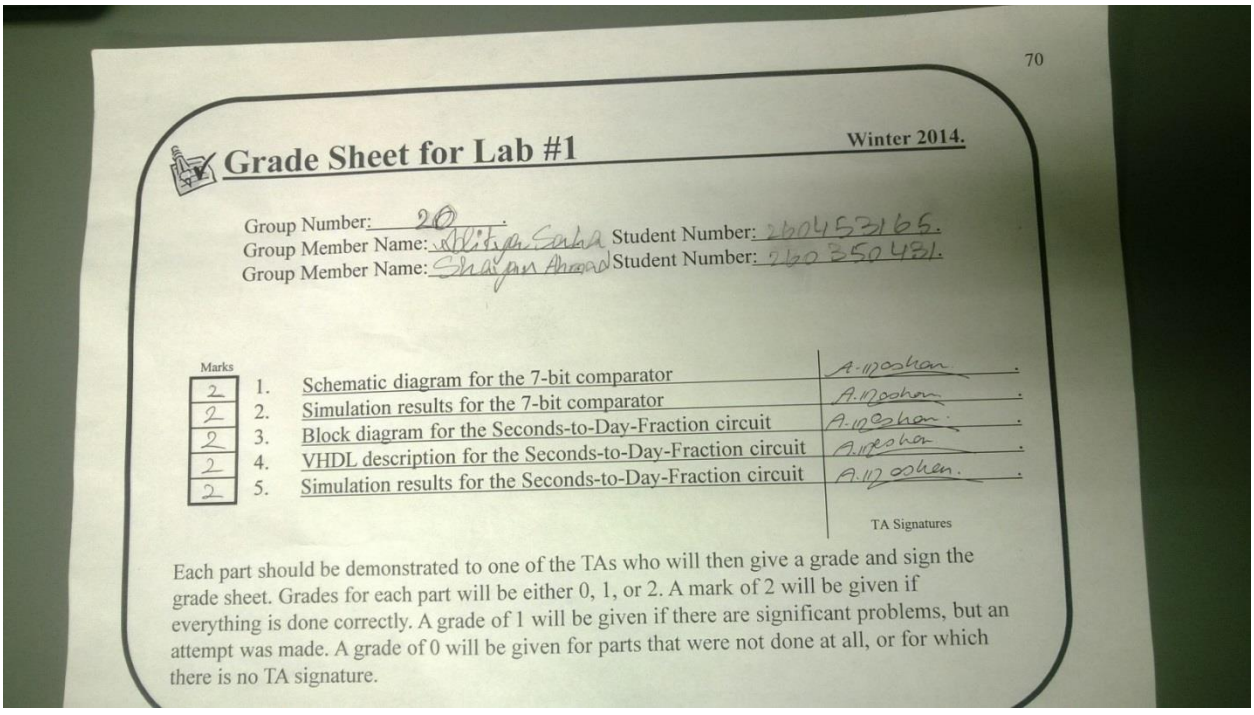



Fig: Simulation diagrams for the predefined values

The simulation outputs were confirmed by manual calculation using the formula defined in the circuit function. This verifies that the circuit works correctly.



70

**Grade Sheet for Lab #1** Winter 2014.

Group Number: 20
Group Member Name: [illegible] Sarka Student Number: 260453165.
Group Member Name: Shayan Ahmad Student Number: 260350431.

| Marks | | | TA Signatures |
|---|---|---|---|
| 2 | 1. | Schematic diagram for the 7-bit comparator | A. Mohan |
| 2 | 2. | Simulation results for the 7-bit comparator | A. Mohan |
| 2 | 3. | Block diagram for the Seconds-to-Day-Fraction circuit | A. Mohan |
| 2 | 4. | VHDL description for the Seconds-to-Day-Fraction circuit | A. Mohan |
| 2 | 5. | Simulation results for the Seconds-to-Day-Fraction circuit | A. Mohan |

Each part should be demonstrated to one of the TAs who will then give a grade and sign the grade sheet. Grades for each part will be either 0, 1, or 2. A mark of 2 will be given if everything is done correctly. A grade of 1 will be given if there are significant problems, but an attempt was made. A grade of 0 will be given for parts that were not done at all, or for which there is no TA signature.