ECSE 323

LAB REPORT 2

Group No. - 20

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# **g20\_binary\_to\_BCD**

## Objective

To make a circuit (g20\_binary\_to\_BCD) that converts a 6-bit binary value to its 2-digit Binary-Coded-Decimal (BCD) representation.

This circuit is implemented using a lookup table (LUT). In the LUT approach, a memory unit is used that has an entry for every 64 possible input pattern. In the Altera, the LPM module implementation is used for the circuit design, and the code snippet given in the lab specification is used for declaration the lpm\_rom component. An .mif file is created to specify the contents of the LUT, which is being referred to in the code.

The binary\_to\_BCD has two inputs and one output:

* 6-bit value named `bin` which represents the binary input
* 1-bit clock input, specified as `clock`
* 8-bit output named `BCD` which represents the converted decimal value

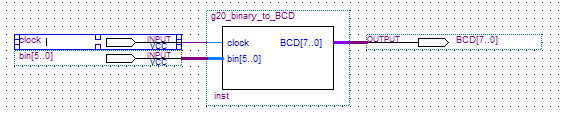


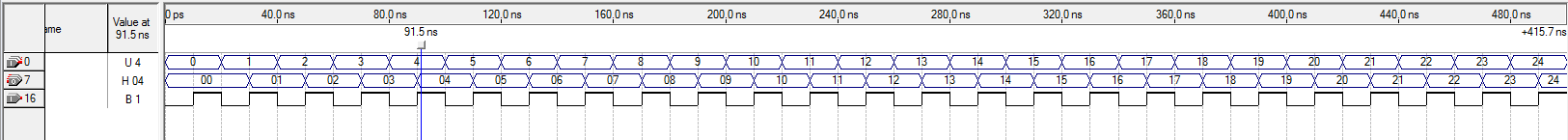
Fig: Higher abstraction for the converter circuit

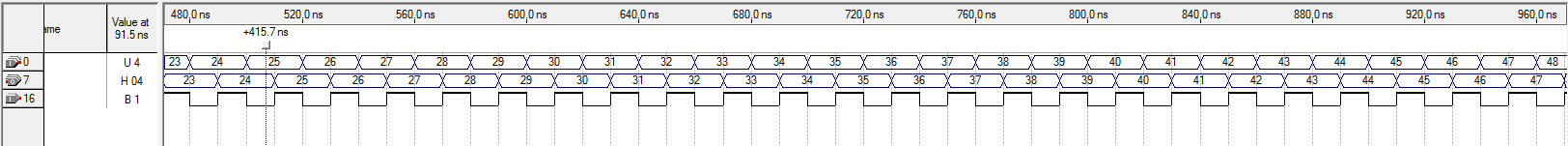
## VHDL description

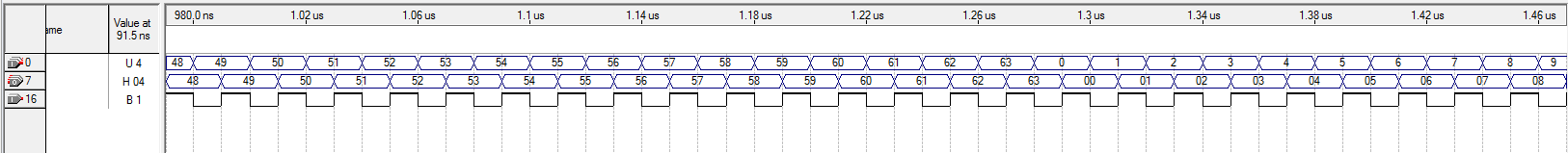
The VHDL description of the circuit has been attached as a separate file in the zipped folder. The VHDL primarily used the code snippet as given in the lab specification to declare the lpm rom module in Altera Quartus. There has been attempts to implement the rom module via altsyncram, but the circuit performance was not reliable. The .mif file representing the lookup table has been appropriately referred to in the code. All the required library import has been

## Circuit testing

Two fold circuit simulation was carried out- functional and timing simulation. The functional simulation was carried out on 64 different input values, and the timing simulation was carried out on 4 distinct values. Motivation for conducting the timing simulation arises from the fact that the circuit introduces an extent of propagation delay, which the functional simulation doesn’t account for. For the functional simulation, the each of the test cases are changed by unit incremental difference as specified in the waveform file. These tests verified the robustness of the circuit. The respective simulation output diagrams are given in the following.







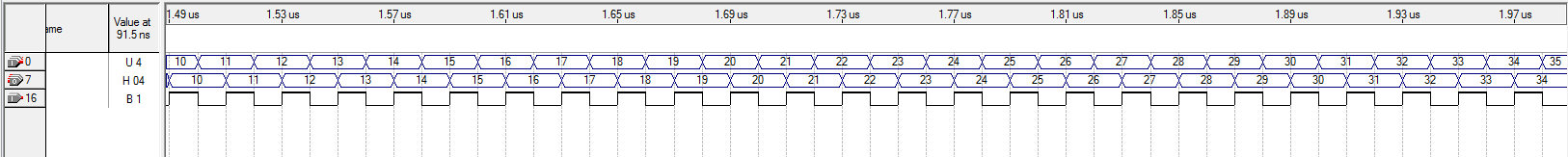


Fig: Functional simulation diagrams for inputs 0-63 (inputs stated in unsigned decimal and output in hexadecimal)

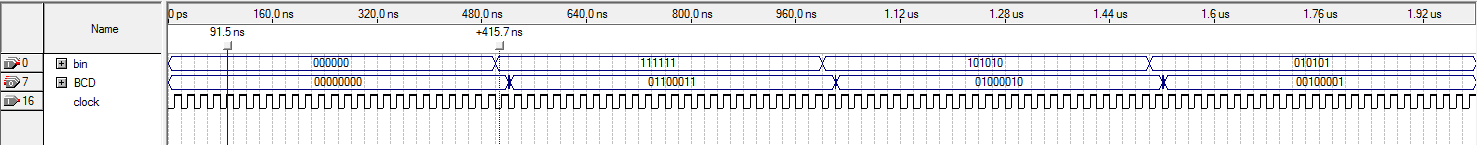


Fig: Timing simulation diagrams for inputs 000000, 111111, 101010, and 010101 (both stated in binary)

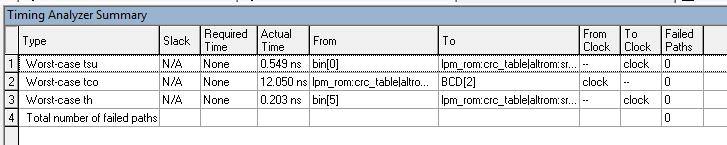


Fig: Timing analyzer summary for the circuit

The timing difference as evidenced in the simulation compares well with the values provided in the timing analyzer summary. Hence it can be concluded that the propagation delays reported and the settling time compares well. Also, it can be roughly seen that the settling time is approximately the same for every transition. Notably according to the simulation summary, 0 logic elements were used.