Kai-Chung Hsieh

Hsinchu City, Taiwan
+886-972932876 kchs.tw@gmail.com ASa Hsieh asahsieh asahsieh

OBJECTIVE

Digital Verification (DV) engineer with 7 years of experience working on Media Processor SoCs, seeking jobs related to **CPU** (listed by expected order):

- CPU Performance Architect
- CPU Design Verification and Emulation Engineer
- CPU Physical Design Implementation

TECHNICAL SKILLS

Languages: SystemVerilog, Verilog, C/C++, Arm assembly, Shell scripting, Perl, Java
Simulators/Tools: VCS, NC-Verilog, Design compiler, Verdi, SimVision
Technologies/Frameworks: UVM, VMM, SVN, Linux
SPECs: USB 2.0/3.0, IEEE 802.3/Ethernet, Arm AMBA AXI/AHB/APB

Currently learned

RISC-V assembly, Ripes simulator, Git, Linux kernel, Python

WORK EXPERIENCE

Communication Network(CN) BU, Realtek | Digital Verification Engineer **Sep 2014 – Sep 2021**
Average performance rating: **A**
Promotion from junior to senior engineer: Sep 2018

- Worked on various digital Home products, e.g., **Set-up box**, **NAS**, etc
- I was responsible for testing High-Speed peripherals by SystemVerilog VMM/UVM methodologies, including **USB** from 1.0 to 3.0 in both of hosts and devices and **Ethernet** supporting media-independent interfaces include MII/GMII/RMII/RGMII
- Worked with the Hardware System Design group to verify ROM code for USBs, including testing for hardware security to enable USB booting following mass storage protocols between PC hosts and USB modules and writing USB data to different flash types or DDR
- Worked as part of a 4-member team to do a whole-system verification for **an in-house memory system**, the system does arbitration on transactions for dozens of HW clients to DDR. We designed a unified and flexible verification platform by UVM, replacing HW clients with Bus Functional Modules (BFMs) of common bus protocols. I was responsible for the BFM of in-house data bus protocol, designing functional test patterns by using top-level sequences, and designing a user-friendly GUI for easy to use
- I was responsible for coordinating a team who worked on peripherals, including USB, Ethernet, PCI-E, SATA, flash controllers and card readers and integrating the peripherals module testbenches into the verification platform
- Worked with and described to vendors issues with their testbenches for the verification of the revision on USB and PCI-E IPs
- Designed a parameterized testbench to verify master/slave supported **wrappers of hardware modules** on all bus protocols including in-house register/data buses and Arm AMBA
- Verified control GPIOs shared by different hardware clients; designed a flow to update test cases automatically according to various combinations and revisions on the SPEC
- Wrote test cases using C language for the above-mentioned modules to verify **test chips** embedded on a demo board

DT/HPC1, MediaTek | Arm CPU verification internship **July 2011 – Aug 2011**

- I was responsible for writing test patterns in assembly code to verify an in-house processor which supports ARMv7-A instruction set

OFF-THE-JOB TRAINING

Currently completing the Computer Architecture based by RISC-V and Linux Kernel Design courses ran by the Linux kernel expert, **Jim Huang**

Computer Architecture based by RISC-V | Assembly, C++ used **Nov 2021 - Present**

The course is based on CS 61C at UC Berkeley, CS152/252: Computer Architecture

Linux Kernel Design | C/C++ used **Sep 2021 - Present**

The course is a comprehensive look at C language based on the CS:APP3e and on the Linux Kernel using the book The Linux Kernel Module Programming Guide (LKMPG) as course materials

COURSEWORK

- Computer Architecture
- Embedded System Design
- Embedded System Software/Tools
- Real-time Computing

EDUCATION

National Chiao Tung University **Sep 2008 – Dec 2013**
Master of Computer Science

- Master thesis: Adaptive Cache Replacement Policies for High Hit Rate of a Cache of Base Register
- Mater research: Mechanisms to accommodate software diversity in chip multiprocessors
- Teaching Assistant for the computer Architecture, Computer Organization and Embedded System Design course

National Chung Cheng University **July 2008 – Sep 2008**
Summer vacation training in the SOC lab

Implemented a pre-synthesis 5-stage pipeline ARM processor by Verilog

Chung Yuan Christian University **Sep 2004 – July 2008**
Bachelor of Computer Science

Courses included:

- Computer organization: A+
- Logic circuit design experiment, which to implement CPUs on FPGA: A+
- Independent study on VLSI design automation, the topic:
  Rectilinear Steiner Routing Problem with Obstacles in Multiple Layers

Honor: Dean's List on 2006 (1st senior year)

EXTRACURRICULAR

MotionPro | Motion Detection, Stepper motor, Zoom lens, ... used **July 2016 – Present**
A project that came from my love of surfing. I tried to design a camera that can detect one of surfers who is catching a wave **without wearing tags**

Surf & house **Oct. 2021 – Present**
Part-time job

- Class C surfing coach license from the Chinese Taipei Exploration Exercise Association
- Designed and taught surfing courses to beginners

Ramen Kikkou **Dec. 2021 – Present**
Part-time job

- Assisted the chef in making various ramen dishes
- Assisted with service in the restaurant