EED 359 - Digital System Design with FPGA's

Assignment-1 **Spring 2017**

a) Write a Verilog code to design logic gates (AND, OR, NOT) and simulate using TestBench.
b) Write a Verilog code to design Universal logic gates (NAND, NOR) and simulate using TestBench.
c) Write a Verilog code to design derived logic gates (XOR, XNOR) and simulate Using TestBench.
d) Write a Verilog code to design a 2:1 Multiplexer and simulate using TestBench.
e) Write a Verilog code to design a 4:1 Multiplexer using 2:1 Multiplexers and simulate using TestBench?
f) Write a Verilog code to design XOR gate using 2:1 Multiplexer and simulate using TestBench.