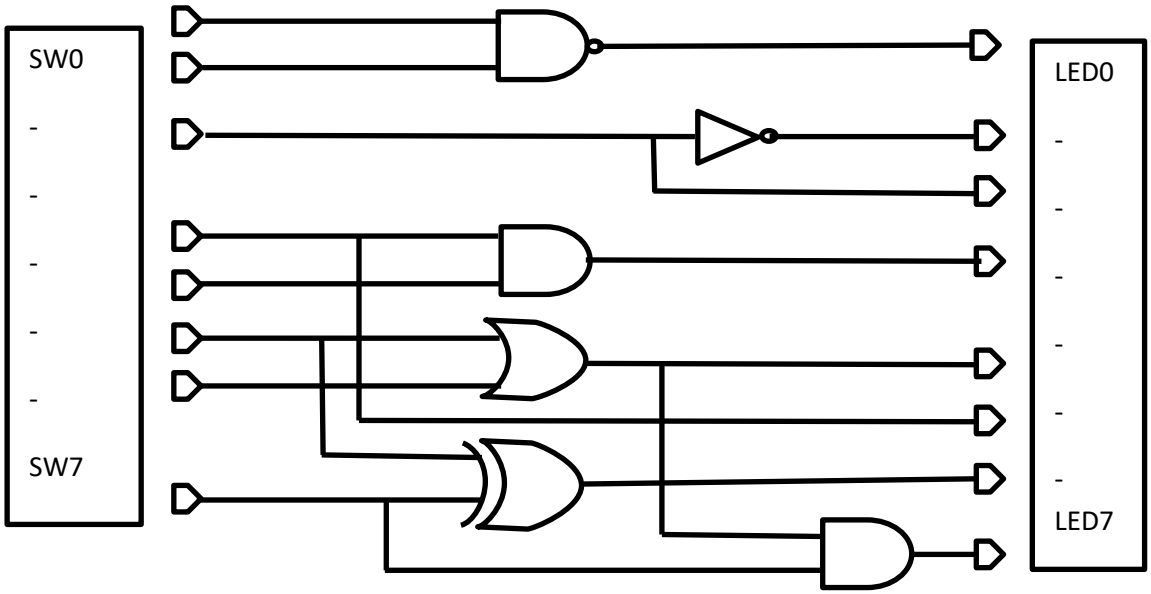
EED 359 - Digital System Design with FPGA's

Assignment-2 **Spring 2017**

a) Write Verilog code to design ALU with following Operations
Operations: Addition, Subtraction, Multiplication and Arithmetic Shifts (Left and Right)
Synthesize the same with Xilinx Nexys4 FPGA target. Also simulate the same using iSim software.

b) Write a Verilog code to design and implement the following Combinational Circuit to drive LEDs. On NEXYS4 FPGA board



c) Write a Verilog code to design and implement 4-bit shift register. First simulate the design in Vivado ISIM and then synthesize the same on Nexys4 FPGA

d) Write a Verilog code to design and implement BCD counter (00-99) with delay approx. 1sec for each count. Run the design on the FPGA to observe the outputs on LCD