EED 359 - Digital System Design with FPGA's

Assignment-3 **Spring 2017**

a) Perform Zero Delay Simulation of SISO, SIPO, PIPO shift registers in VERILOG HDL using a Test bench.

b) Perform Zero Delay Simulation of asynchronous and synchronous 4-bit up - down BCD counter in VERILOG HDL using a Test bench.

c) Perform Zero Delay Simulation of up- down counter. The counter has a 'u' input that controls its count direction. If 'u' is 1, it counts {010, 011, 101, 011, 111, 001…..}. If 'u' is 0, it counts this same sequence in opposite direction.

d) Write a Verilog code to create a digital clock display hh:mm:ss on seven segment display of NEXYS 4 FPGA

e) Write a Verilog code to perform VGA interface with FPGA showing on monitor display as "Hello World".