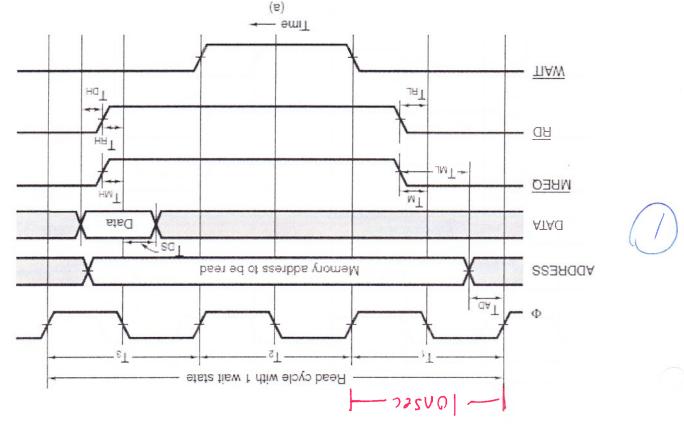
1242

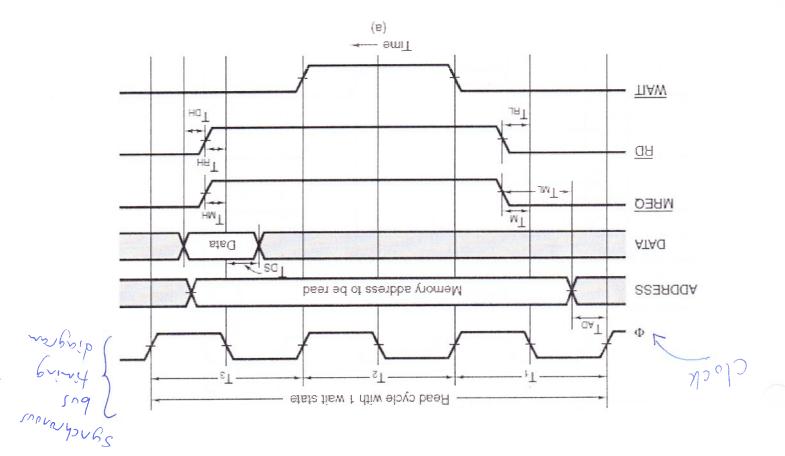
voss d



tinU xsM nii		niM	Parameter	lodmys
pesu	7		Address output delay	αΑΤ
oəsu		2	Address stable prior to DEAM of noing eldsts assured	1MT
uzec	8		Λ T in Φ to edge of Φ in T,	MT
oəsu	ε		T ni & to agba gnillst mort vslab GR	Ter
uzec		2	Φ to egbe gnillst of noring emit guttes atsQ	sal
uzec	3		$\overline{\text{MREQ}}$ delay from falling edge of Φ in T_3	HMT
oəsu	8		ϵT ni Φ to egbe gnillst mort valeb \overline{GR}	няТ
oəsu		0	QA to noitsgan mort amit blod stsQ	HaT

1) OO MHZ Frequery but the top of the doth whomy solders

	3 H 8	2 GHz	5 Hz	250 MHZ	2HWOH	- GHZ	100 MHz	Ht, cycles
	125 msec/cycle	500 picoses/sycle	200 Msec/cycle	4 Kseckou 4000 sec/cych	25 sec/cycle	1 n sec/cycle	10 nsec/cycle	Clock Cycle And Seconds/Cycle
32	- 67 - 57	1- ~1-	~\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \		100000 16966		100 million cycles	100 × 166



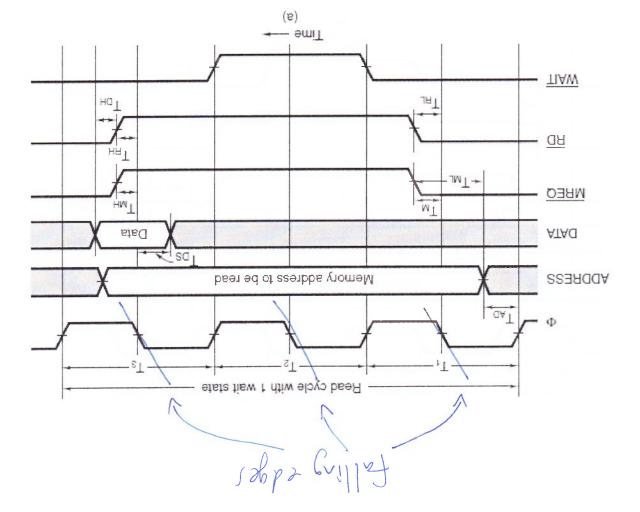
tinU xsM niM		niM	Рагатетег	lodmy2	
usec	Þ		Address output delay	□AT	
oəsu		2	Address stable prior to MPEQ	TML	
pesu	3		1 T ni Φ to egbe gnillst mort ysleb $\overline{\text{DAPM}}$	MT	
Desu	3		RD delay from falling edge of Φ in T_1	T	
oəsu		2	Φ to egbe gaillist of noing emit gutes sts Ω	saT	
วอรน	3		$_{\rm E}$ T ni Φ to agba gnillst mort yelab $\overline{ m OBAM}$	HMT	
pesu	ε		$_{\rm E}T$ ni Φ to edge orillst mort vsleb $\overline{\rm GR}$	HAT	
usec		0	OR to notize an mort emit blod stsO	HGT	

Piche of orders and duddines, Reguest and

responds.

CPU puts an address on the bus and then issues a selders and the requests. Memory receives the address and the requests from the bus, Memory comust be a while with the speed so it till the speed; it'll be a while. The it tills the speed is it cpu the data is ready, the speed it is the speed.

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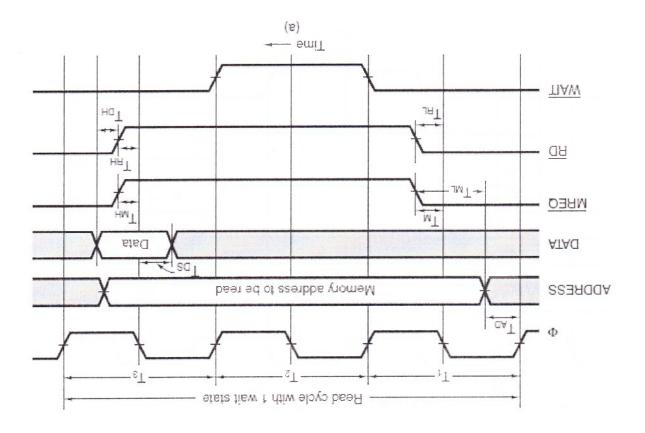


tinU xsM niM		niM	Parameter	lodmy2
Desu	Þ		Address output delay	QA.T
oəsu		2	Address stable prior to MREQ	TMT
pesu	8		T ni Ф to agba gnillst mort yslab QHMM	MΤ
pesu	ε		T ni Φ to egbe gnillet mont γείεb ΩR	JRT.
uzec		2	Φ to agbe gnills) of noring emit guttes atsQ	SOI
oəsu	3		cT ni Φ to egbe gnills mort γsleb Ω∃ЯМ	HMT
oesu	3		ϵT ni Φ to Φ be goills from talling edge of Φ in Γ_3	HET
nsec		0	QR to notiseen mort emit blod stsQ	HOT

CPU; squesting data (b) from remary and the CPU's dead line to receive it is measured from

Start & Lour Countdown OAT -> 225560 phone _ mirso Order a pizza: (q) QR to noitegen mort emit blod sisQ pesu do not check HH I εT ni Φ to egbe gnillst mon ysleb QA E Desu HWI ET πi Φ to agba gnillst most yelab ΩΞΗΜ oəsu 3 be Rady :. (sal Φ to egbe gnills of roing emit gutes stsΩ Desu 5 You Ilin pesu 8 AT ni & to agbe anillat mort yaleb OA 50080 MI Tri to to edge edillst most valed QEAM 8 Desu PHSarba OBAM of nonq elasts asenbbA \mathbb{T}^{NL} 7 pesu 10# ndo my & Address output delay DAT วอธน t lodmys Parameter 2/0400 tinU Max uin the data 29 from the Cpy 2445 one Junit TIAW aЯ MREQ Data ATAG ₹ SO Memory address to be read **ADDRESS** DAT - Read cycle with 1 wait state -25 cycles -9-

20T -> 60:F fry of lavers 02:3



tinU xsM niM		niM	Parameter	lodmy2	
oesu	Þ		Address output delay	ΩĄΤ	
oəsu		2	Address stable prior to AMREO		
oəsu	ε		† T ni † 0 to agba gnillst mort yelab $^{\prime}$ 2ARM	MT	
pesu	3		T ni & to agba gnillst mort vsfab QR	JRT	
oəsu		2	Data setup time prior to falling edge of $\boldsymbol{\Phi}$	SGL	
nsec	3		ϵT ni Φ to agba gnillst mort yelab $\overline{O}\overline{A}\overline{A}\overline{A}\overline{A}$	HMT	
oəsu	3		$\overline{\text{BD}}$ delay from falling edge of Φ in T_3	няТ	
Desu		0	QR to noitspan mort amit blod stsQ	HaT	

(q)

Jeb. 22

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Thursday - revre } 5 set reps Thursday - revre