- Textbook v. 6 - bring to each lab

30 85 grades

- (ding rams) focus

Sw2-301 Jason - Harrison @ boit. ca

> - don't full behind 522110 8 20H -- read text before class How to do well! - questions - no cheating work together

- Web/Mobile Entrepreneurship

Diagrams: (1) 13 5, 18, 50 &

Comp 1113 (3) 161, 164, 165, 167, 173, (4) 245, 292, 307 63 ,28 'x54 '99' t5 61 (2)

Reading? John von Neumann

y diagrams

stee

John von Neumann

Jan 10 2510 2526 quiz every week Camm 2714 1272 faster 2/20/7 Marina chris ICST grad genius SSD MOR RAM First quil : Tresday
Jan 17

5

Byt: 8 6,75 word size: depends: eg 32 bits, 64 bits 238-1212-64 M word: addressable prit 724 = 16 M 1 1 1 6 K 5° = 2° × 2 18= 256 K es coddress value 735 32 G ) 36 = 64 G , 25 = 32 M 75=32 word-sized memory inside the cpu register: 720 = 710 = 1024 = 1 Kilo 2 40 = 7= 128 () tera 1 negs 1 9,90

4

Sud electrical pathway along which central processing unit fetiles, decodes, and executes instructions data passes between devices

big slow far from cpu 10D 85D cache Cache registes inside Cpu

3

[uli: Scan rates + send to set rips

interpretation: Compilation: Converts instructure from some compilation: Converts language all at one to some lower-level language, the which is ultimately executable. Can discard the program instruction to the connects one HLL Can't discard the original. corresponding set of LLL in structions then repeat with the rext HLL instruction. original HLL code.

but its exectable runs fast intropretation is a slow prouds but it can begin running source. 213 × 214 = 128 M