

④

Memory takes 15 nsec to put the data on the bus from the memory address when is stable.

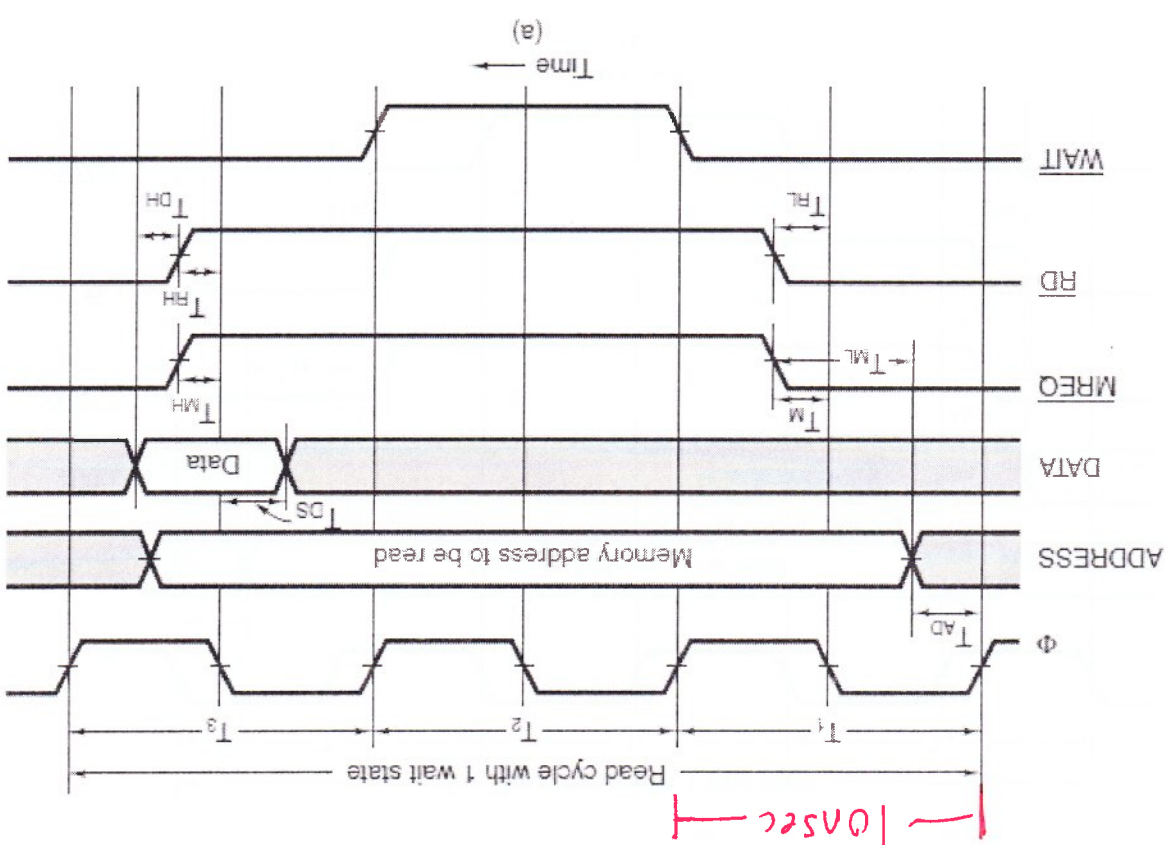
③

100 MHz frequency bus $\rightarrow 10 \text{ nsec/cycle}$

②

Symbol	Parameter	Min	Max	Unit
T_{AD}	Address output delay		4	nsec
T_{ML}	Address stable prior to \overline{MREQ}	2		nsec
T_M	\overline{MREQ} delay from falling edge of ϕ in T_1	3		nsec
T_{RL}	RD delay from falling edge of ϕ in T_1	3		nsec
T_{DS}	Data setup time prior to falling edge of ϕ	2		nsec
T_{MH}	\overline{MREQ} delay from falling edge of ϕ in T_3	3		nsec
T_{RH}	RD delay from falling edge of ϕ in T_3	3		nsec
T_{DH}	Data hold time from negation of RD	0		nsec

(b)



①

2+21

Lesson 11

frequency Hz, cycles/second	clock cycle time seconds/cycle
100 MHz	10 nsec/cycle
→ 1 GHz ←	1 nsec/cycle
40 MHz	25 sec/cycle
250 MHz	4 ksec/cycle 4000 sec/cycle
5 Hz	200 msec/cycle
2 GHz	500 piconsec/cycle
8 Hz	125 msec/cycle

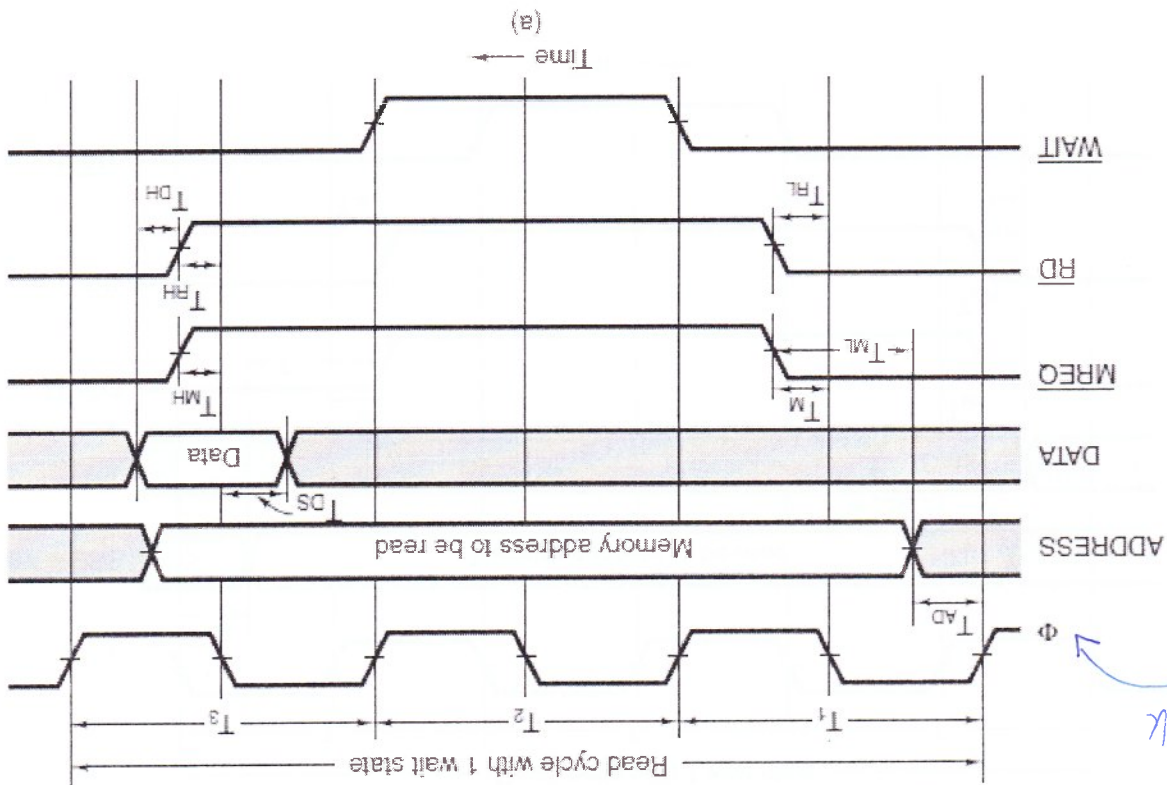
$$100 \times 10^6$$

$$100 \text{ million cycles/second}$$

$$= \frac{1}{100,000,000} \text{ sec/cycle}$$

$$\frac{1}{2} \quad \frac{1}{4} \quad \frac{1}{8} \quad \frac{1}{16} \quad \frac{1}{32} \quad \frac{1}{64}$$

Synchronous bus timing diagram



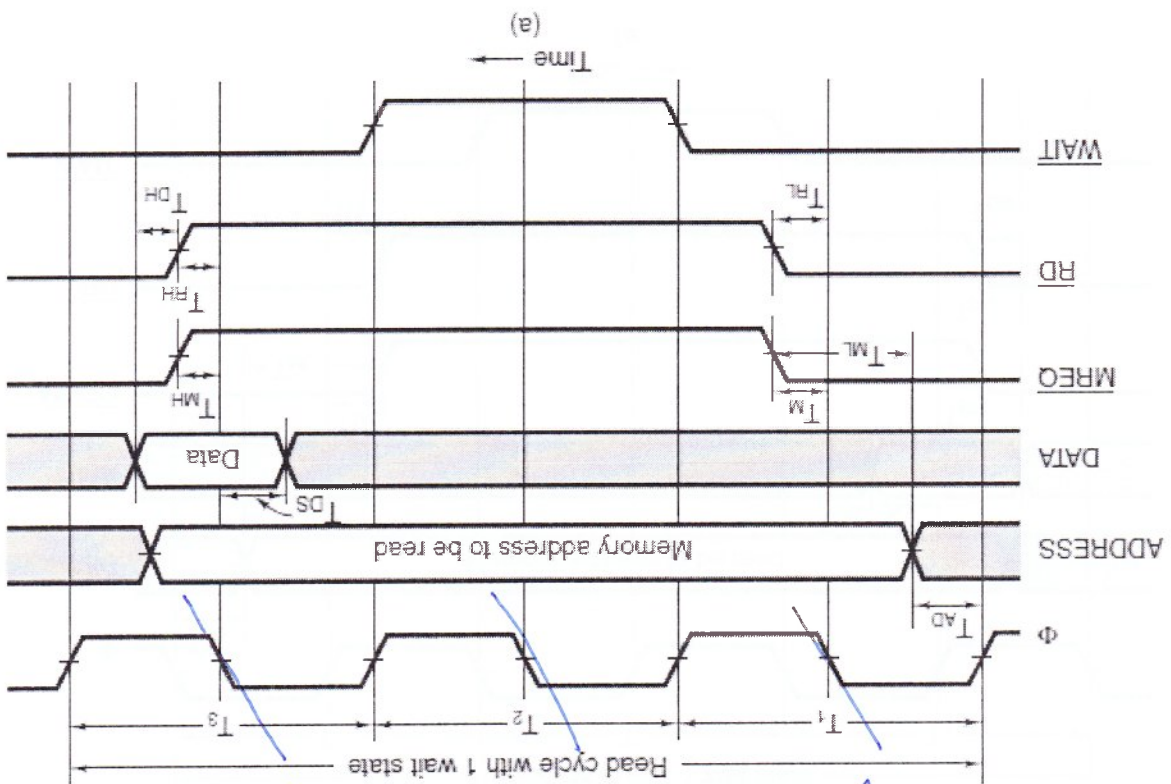
Symbol	Parameter	Min	Max	Unit
T_{AD}	Address output delay		4	nsec
T_{ML}	Address stable prior to $MREQ$	2		nsec
T_M	$MREQ$ delay from falling edge of Φ in T_1	3		nsec
T_{RL}	RD delay from falling edge of Φ in T_1	3		nsec
T_{DS}	Data setup time prior to falling edge of Φ	2		nsec
T_{MH}	$MREQ$ delay from falling edge of Φ in T_3	3		nsec
T_{RH}	RD delay from falling edge of Φ in T_3	3		nsec
T_{DH}	Data hold time from negation of RD	0		nsec

Picture of orders and deadlines. Request and

responses.
CPU puts an address on the bus and then issues a READ request. Memory receives the address and the request from the bus. Memory cannot keep up with the speed so it tells the CPU it'll be a while. Then it tells the CPU the data is ready, the CPU reads the data and uses it.

the falling edge of the clock.

Symbol	Parameter	Min	Max	Unit
T_{AD}	Address output delay		4	nsec
T_{ML}	Address stable prior to <u>MREQ</u>	2		nsec
T_M	<u>MREQ</u> delay from falling edge of Φ in T_1	3		nsec
T_{RL}	RD delay from falling edge of Φ in T_1	3		nsec
T_{DS}	Data setup time prior to falling edge of Φ	2		nsec
T_{MH}	<u>MREQ</u> delay from falling edge of Φ in T_3	3		nsec
T_{RH}	RD delay from falling edge of Φ in T_3	3		nsec
T_{OH}	Data hold time from negation of RD	0		nsec



falling edges



100 metre long field

start $\frac{1}{2}$ hour Countdown
6:50 arrival to eat 7:00 \rightarrow TOS

Phase \rightarrow MREQ
 order \rightarrow TAD

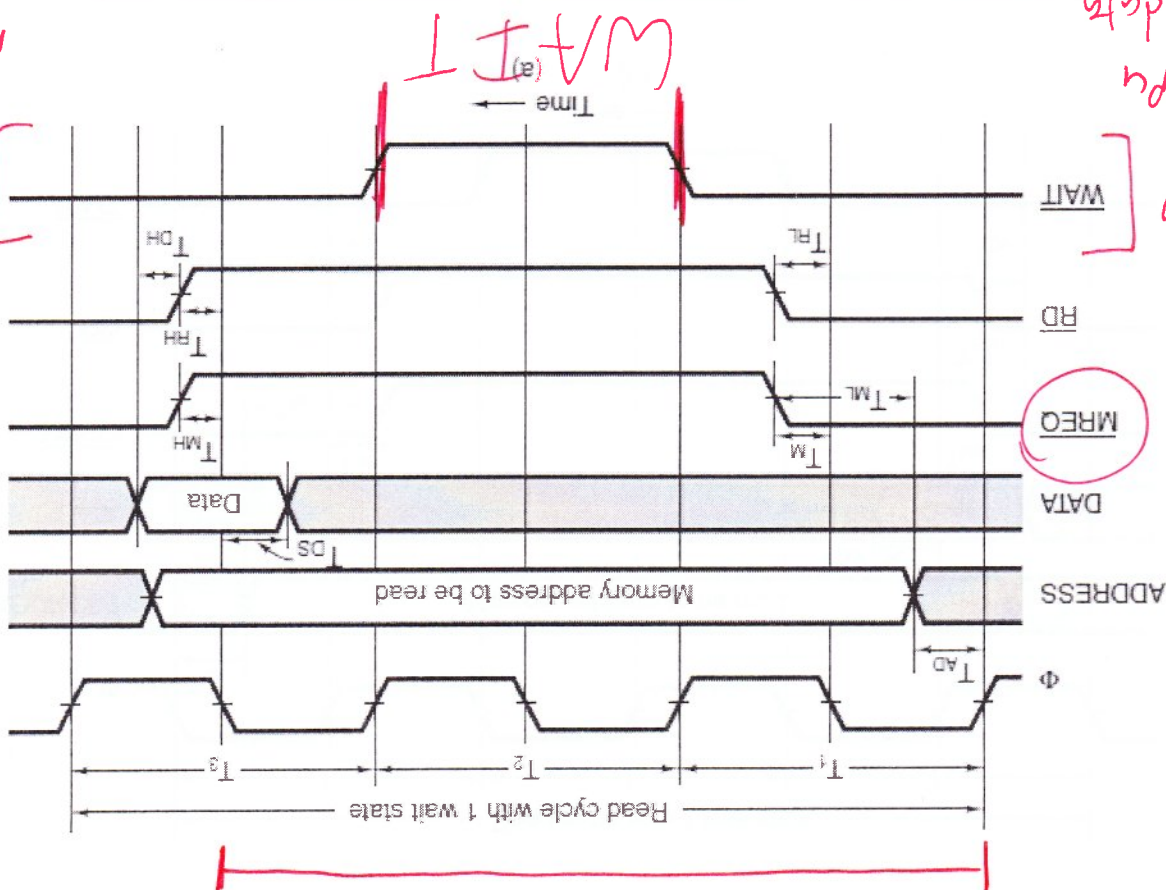
order a pizza!

(b)

Symbol	Parameter	Min	Max	Unit
<u>TAD</u>	Address output delay		4	nsec
TML	Address stable prior to MREQ	2		nsec
T _M	MREQ delay from falling edge of Φ in T ₁	3		nsec
T _{RL}	RD delay from falling edge of Φ in T ₁	3		nsec
<u>TDS</u>	Data setup time prior to falling edge of Φ	2		nsec
T _{MH}	MREQ delay from falling edge of Φ in T ₃	3		nsec
T _{RH}	RD delay from falling edge of Φ in T ₃	3		nsec
T _{DH}	Data hold time from negation of RD	0		nsec

do not clock
 be ready ::
 will not
 requests
 the data
 the CPU
 memory tells

one wait state
 must be
 a whole
 # of
 cycles



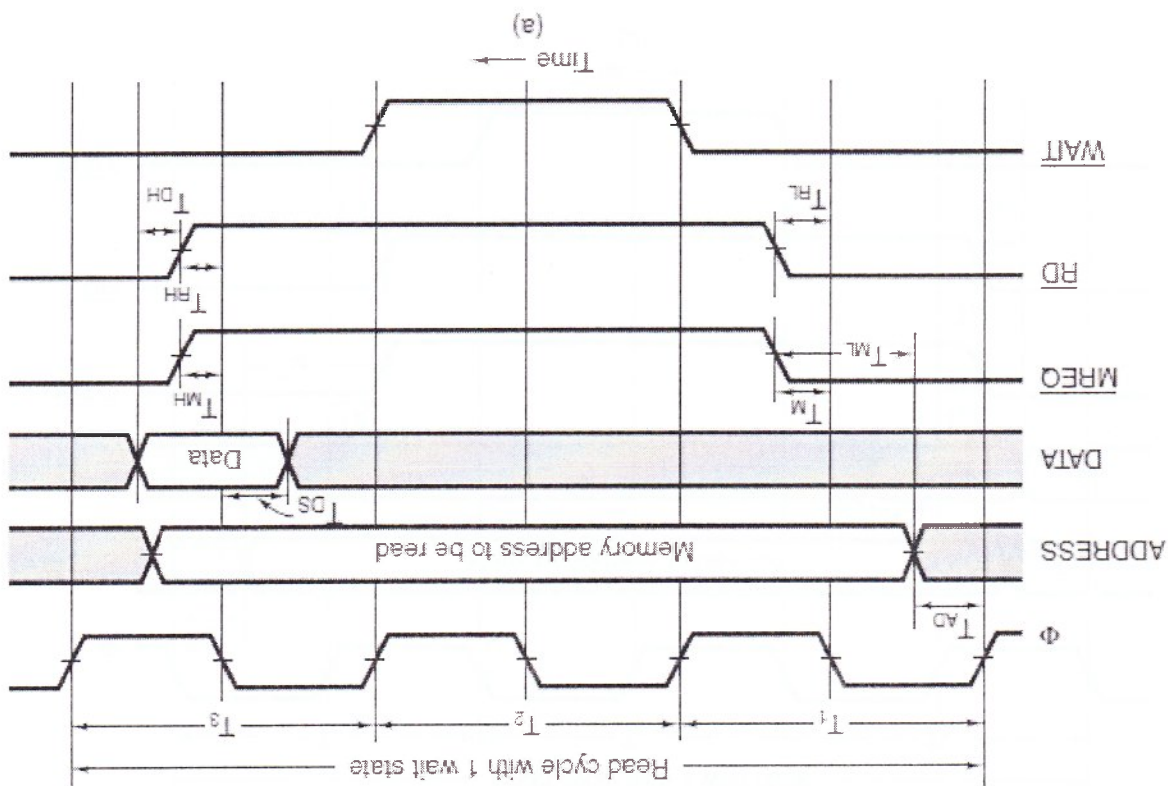
$2\frac{1}{2}$ cycles

Wednesday
Feb. 22

330-530
Ne 1-331

Widren

Symbol	Parameter	Min	Max	Unit
T_{AD}	Address output delay		4	nsec
T_{ML}	Address stable prior to <u>MREQ</u>	2		nsec
T_M	<u>MREQ</u> delay from falling edge of Φ in T_1	3		nsec
T_{RL}	RD delay from falling edge of Φ in T_1	3		nsec
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T_{MH}	<u>MREQ</u> delay from falling edge of Φ in T_3	3		nsec
T_{RH}	<u>RD</u> delay from falling edge of Φ in T_3	3		nsec
T_{DH}	Data hold time from negation of <u>RD</u>	0		nsec



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