CMOS-VLSI Design

CDA 4213L 001/002/003/004: (Undergraduate)

CIS 6930 Sec 012: (Graduate)

Final Project Report

User Document

Submission Deadline

Upload to Canvas By

11:59PM Saturday, December 12th 2015

Report must be in PDF format

Submission MUST be in ZIP Format

Today's Date:	12/11/2015
Team Name:	Netlist and Chill
Team Members & U#:	Team Member 1: Muhaimen Shamsi % Work Distribution: 33.33 Team Member 2: Andres Izurieta % Work Distribution: 33.33 Team Member 3: Arpit Saluja % Work Distribution: 33.33
No. of Hours Spent:	200
Exercise Difficulty: (Easy, Average, Hard)	Hard
Any Other Feedback:	Make simulations run faster. Pls.

A. Introduction

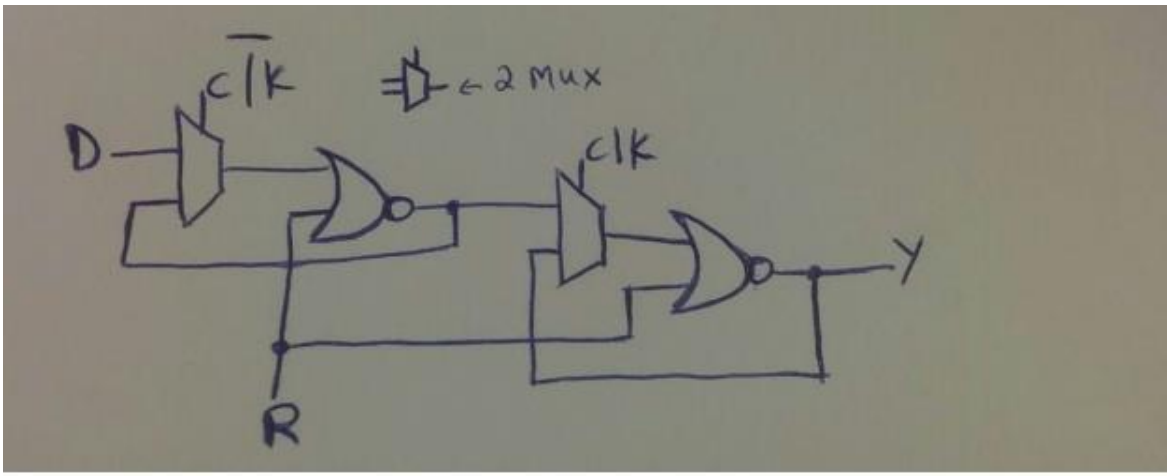
In one paragraph describe the project and the requirements

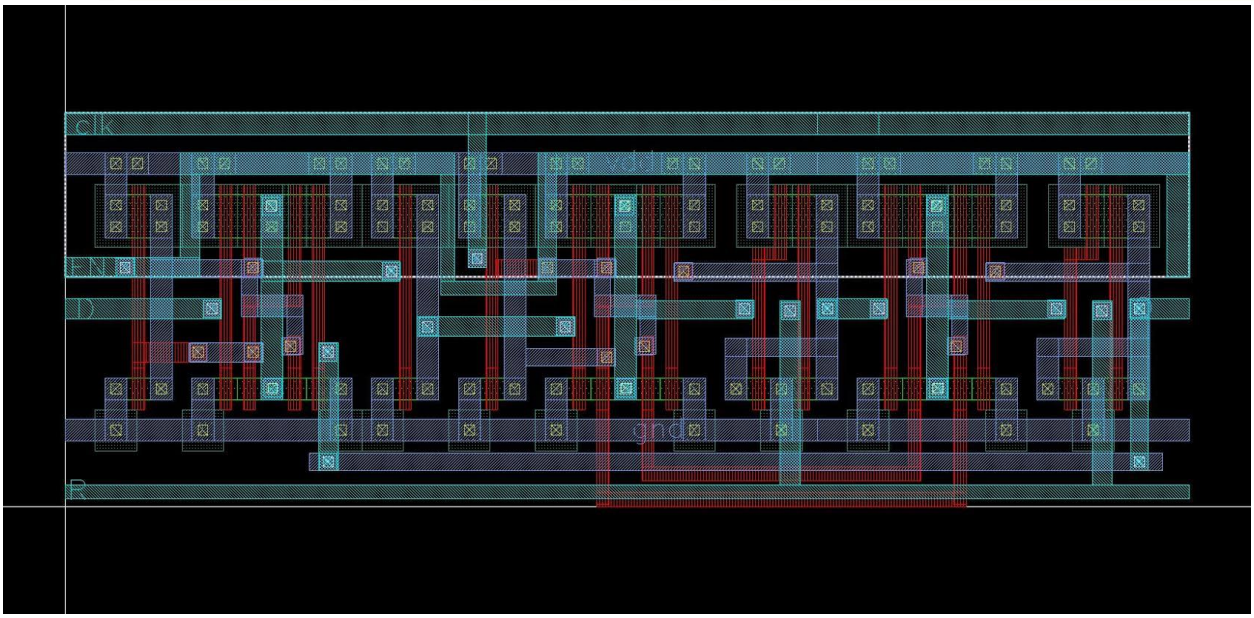
This project requires us to design and implement an array multiplier using the Cadence tools. The minimum number of bits for the inputs is 8, and both inputs and outputs are shifted in/out serially. It is required that the design fits within the padframe provided and that it uses the available I/O pins.

B. Design Details

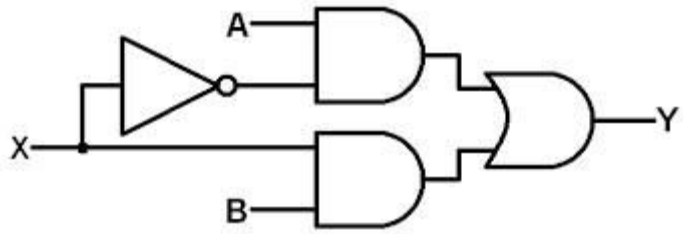
B.1 For each of the following, include gate-level and layout level designs

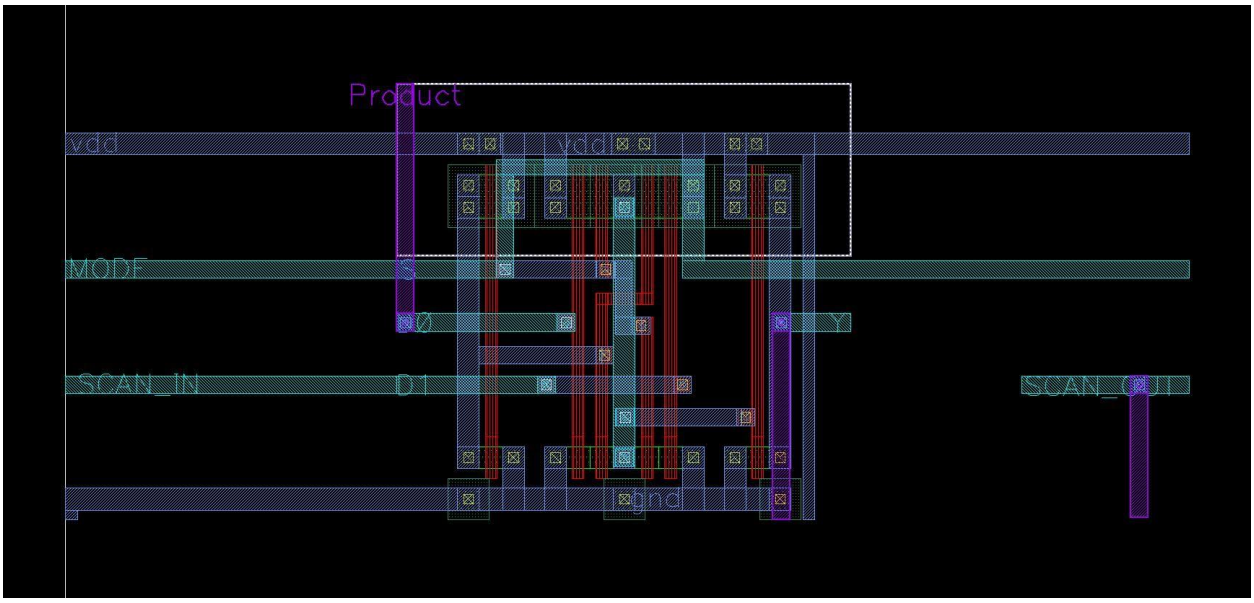
- *D Flip Flop Bit slice*



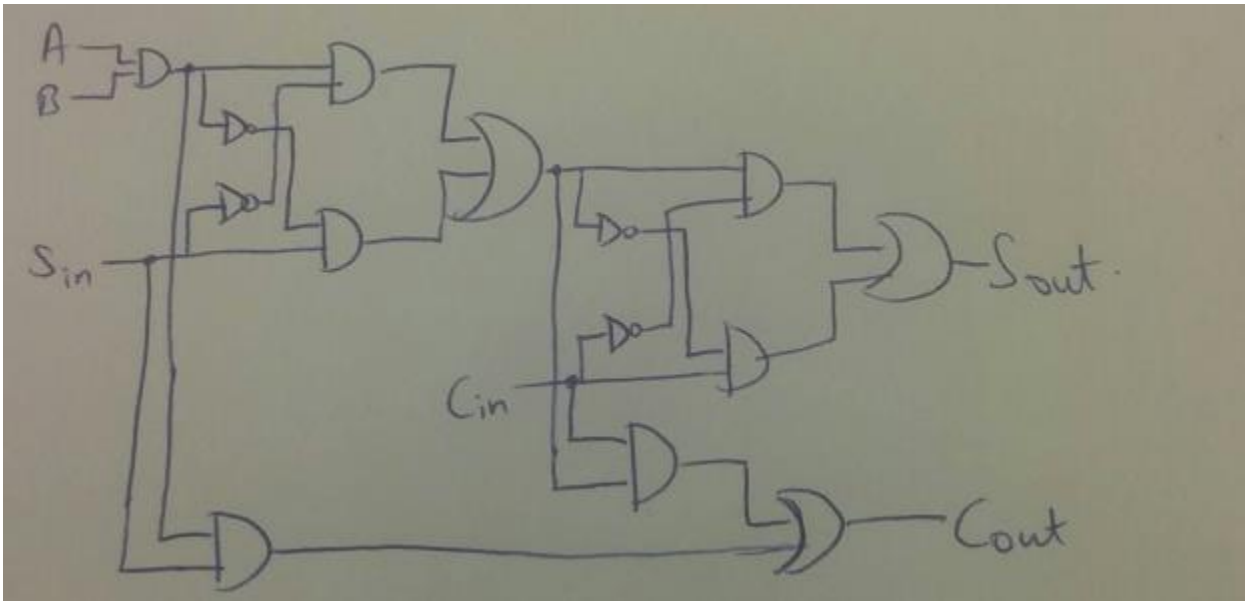


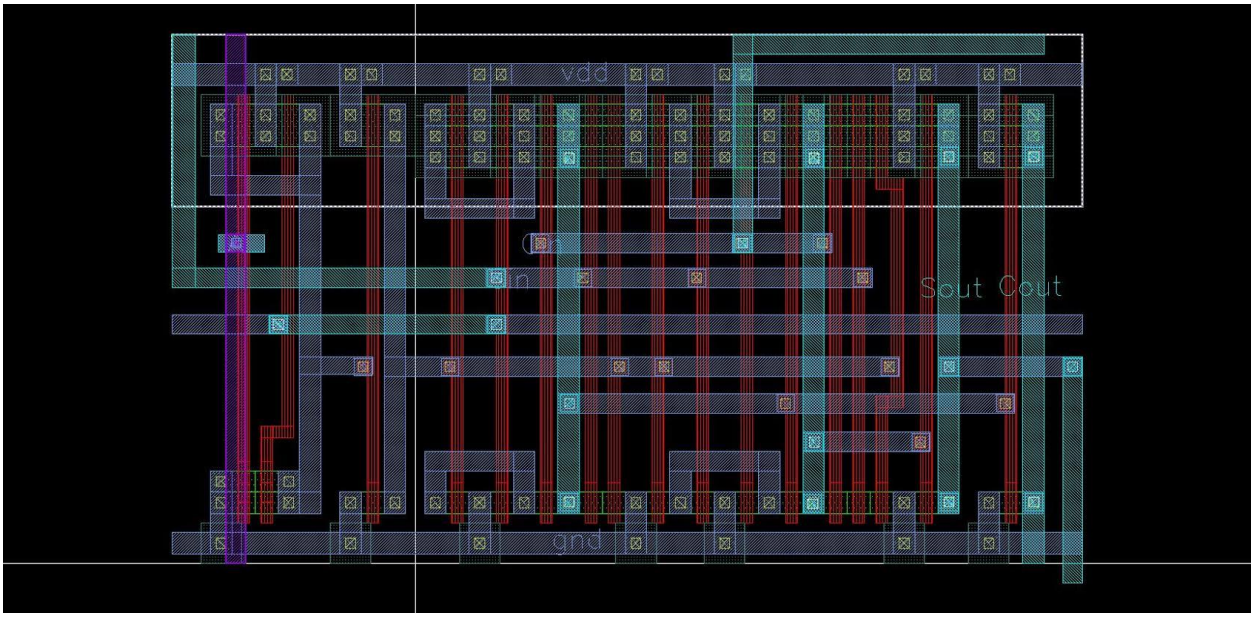
- *Multiplexor Bit slice*

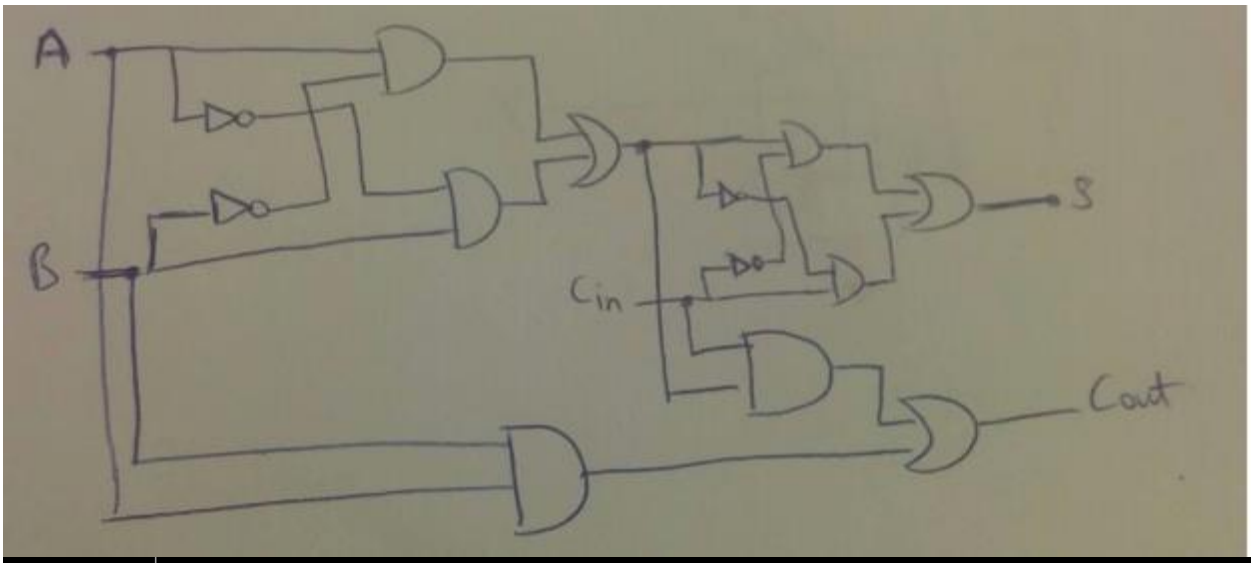

A
X
B
Y
Y = (A • X̄) + (B • X)

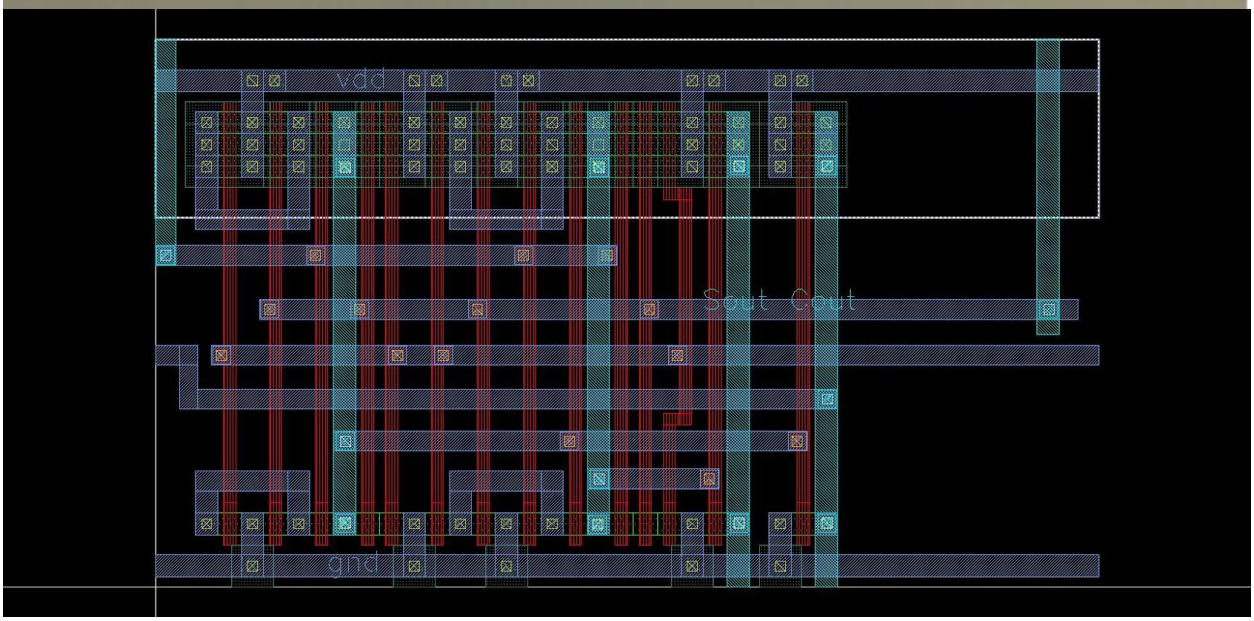

Product
vdd
vdd
MODE
S
Y
SCAN_IN
D1
SCAN_OUT
gnd

- *Multiplier Bit slice cells (Two)*



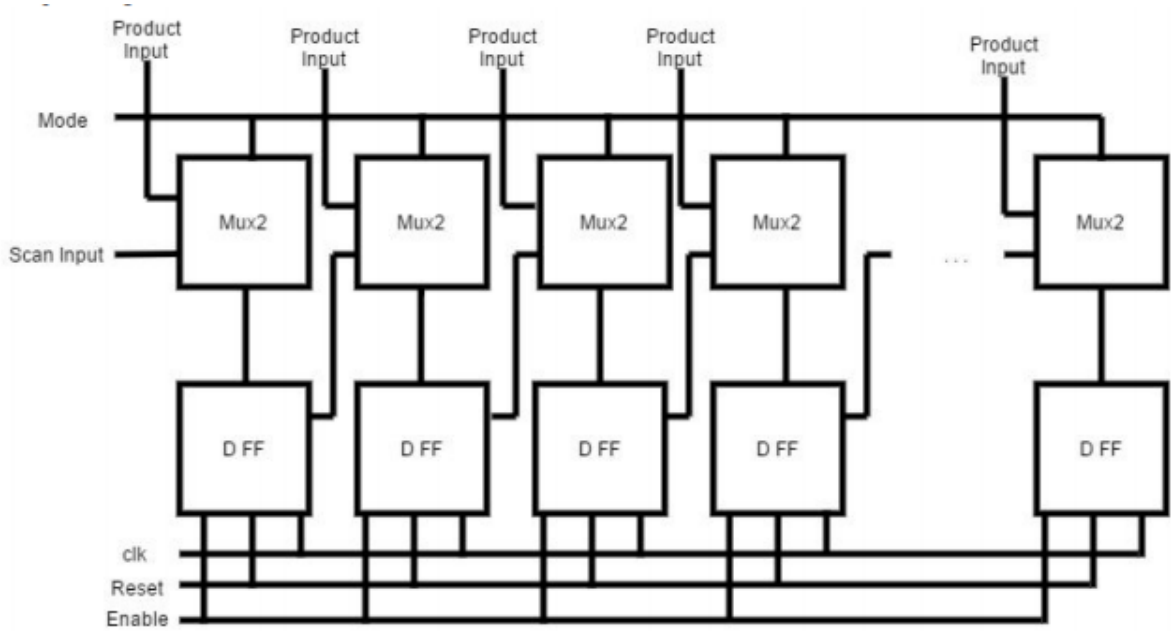


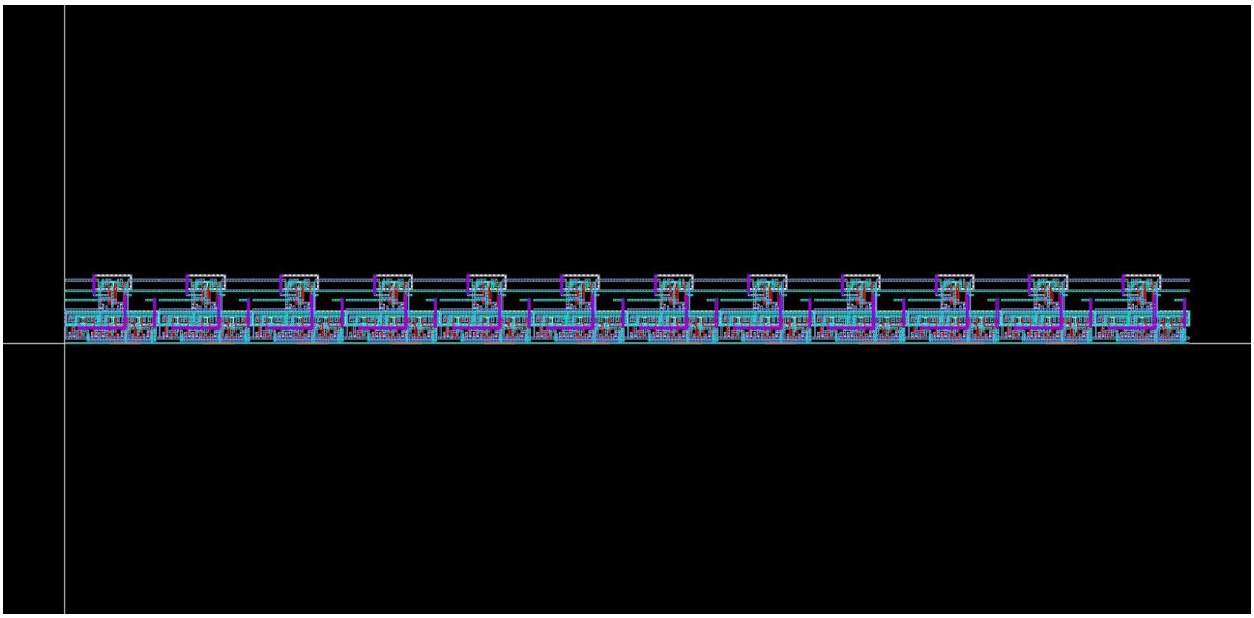

A
B
Cin
S
Cout


vdd
Sout Cout
gnd

- *N-bit Register*

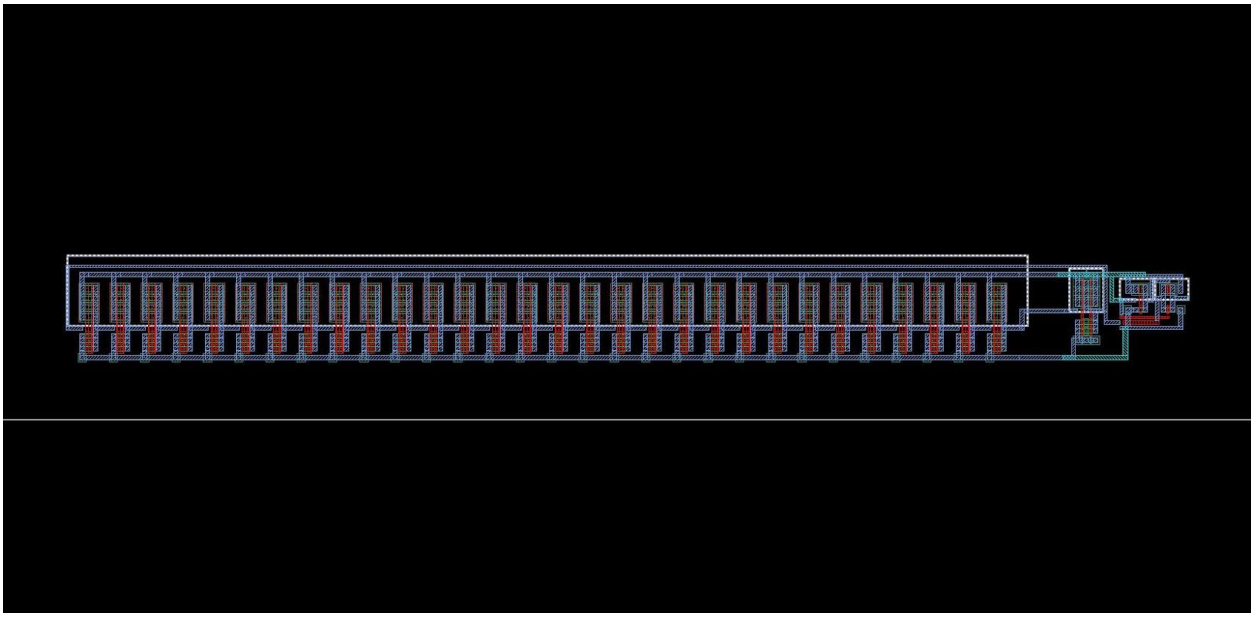
Note: This is our output register, which includes a D-FF <u>and</u> a MUX at each bit-slice. Our input register is just a series of D-FFs.

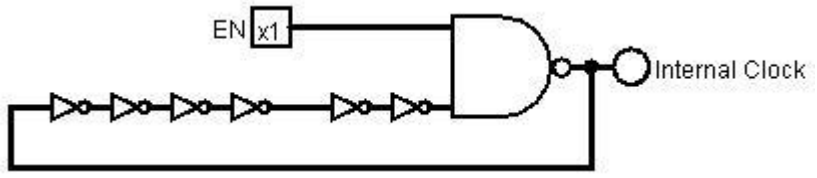




- *Ring Oscillator (if attempted)*

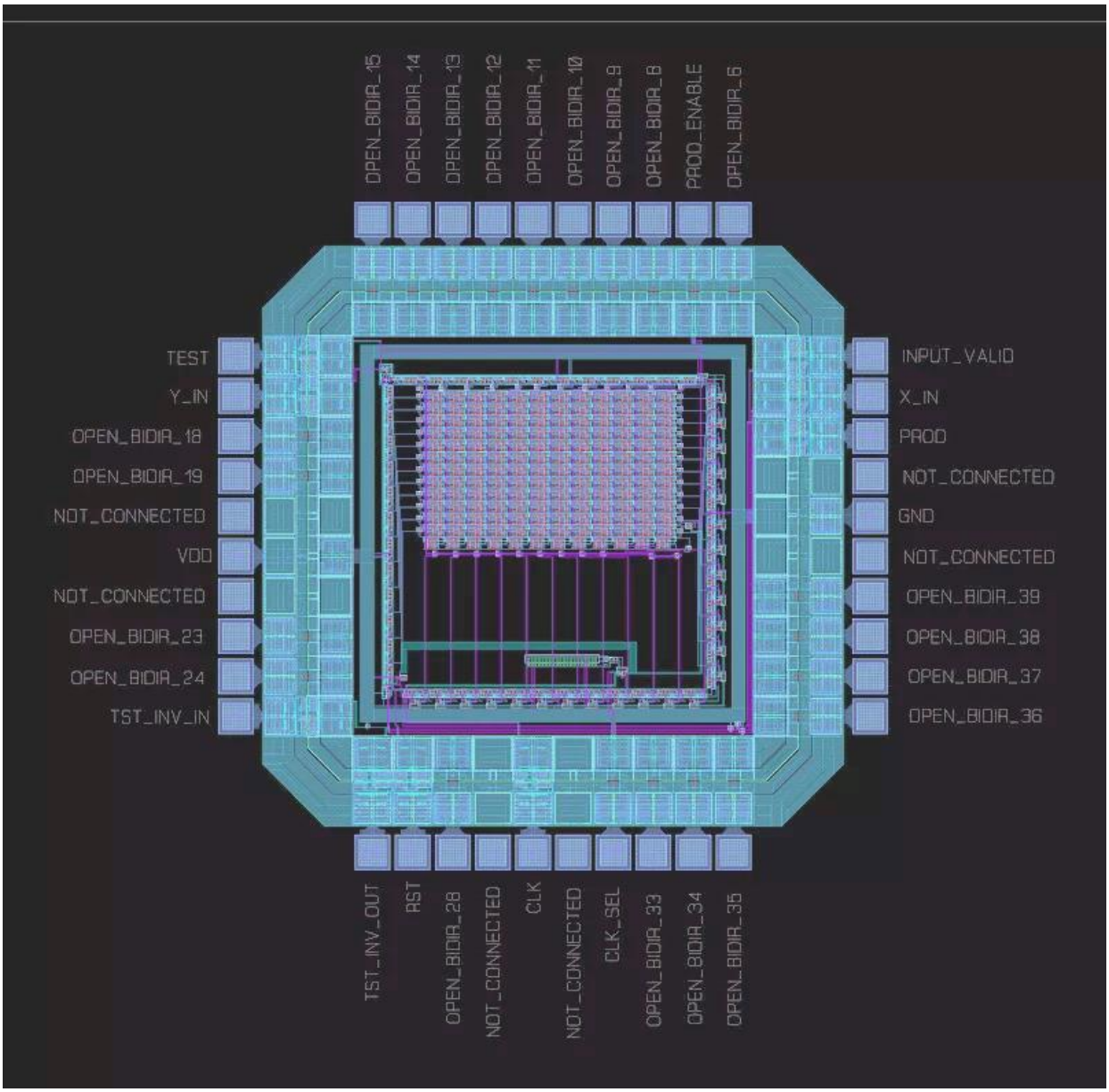
Produces a clock cycle time of approximately 30ns. The design is instantiated, flattened and modified inside the Padframe to reduce it to 20ns.





The EN signal is connected to Vdd inside the Padframe so that the internal clock is always on.

B.2 Chip Layout – Include a screen shot of your chip layout with padframe



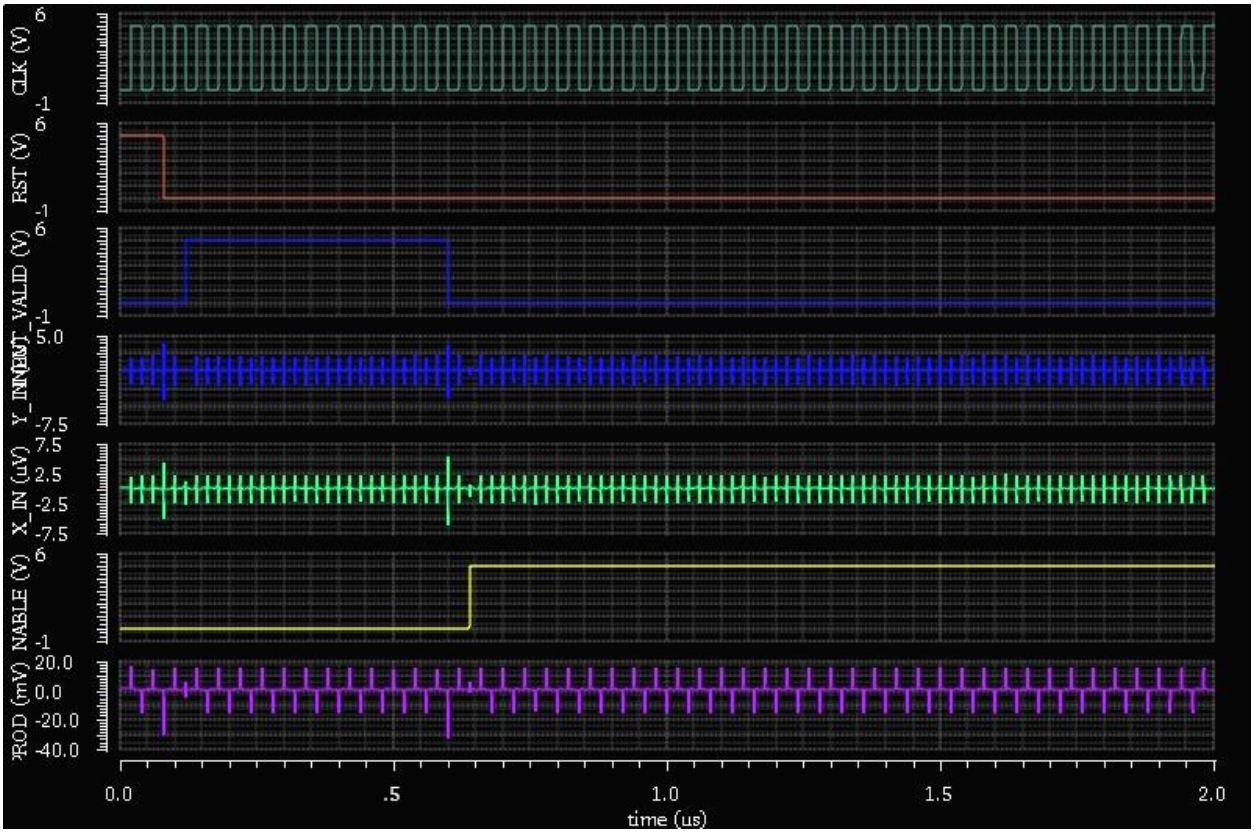
B.3 Simulations and Results – For each of the following stimuli provide a waveform screenshot (1 per page).

Notes: For all waveforms in section B.3, the CLK_SEL input is set to 0V (Select External Clock). Unless shown otherwise,the TEST input is also set to 0V (Select Non-Scan Chain Mode) These labels are not included in all waveforms because of a bug where the simulation software fails to plot them.

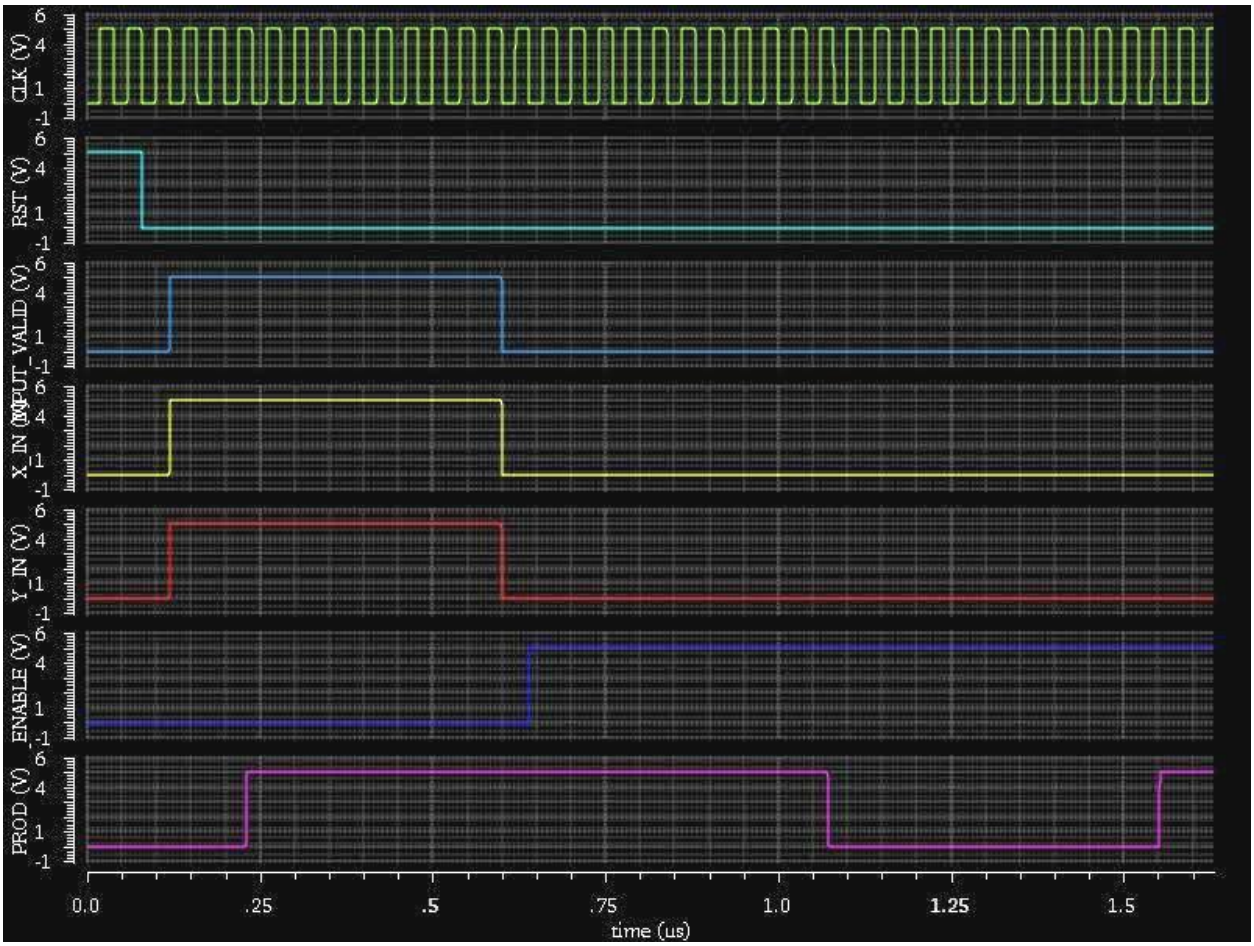
The labels for all the waveforms except for the last one (Scan Chain/Test Inverter) are from top to bottom:

- CLK
- RST
- INPUT_VALID
- X_IN
- Y_IN
- PROD_ENABLE
- PROD

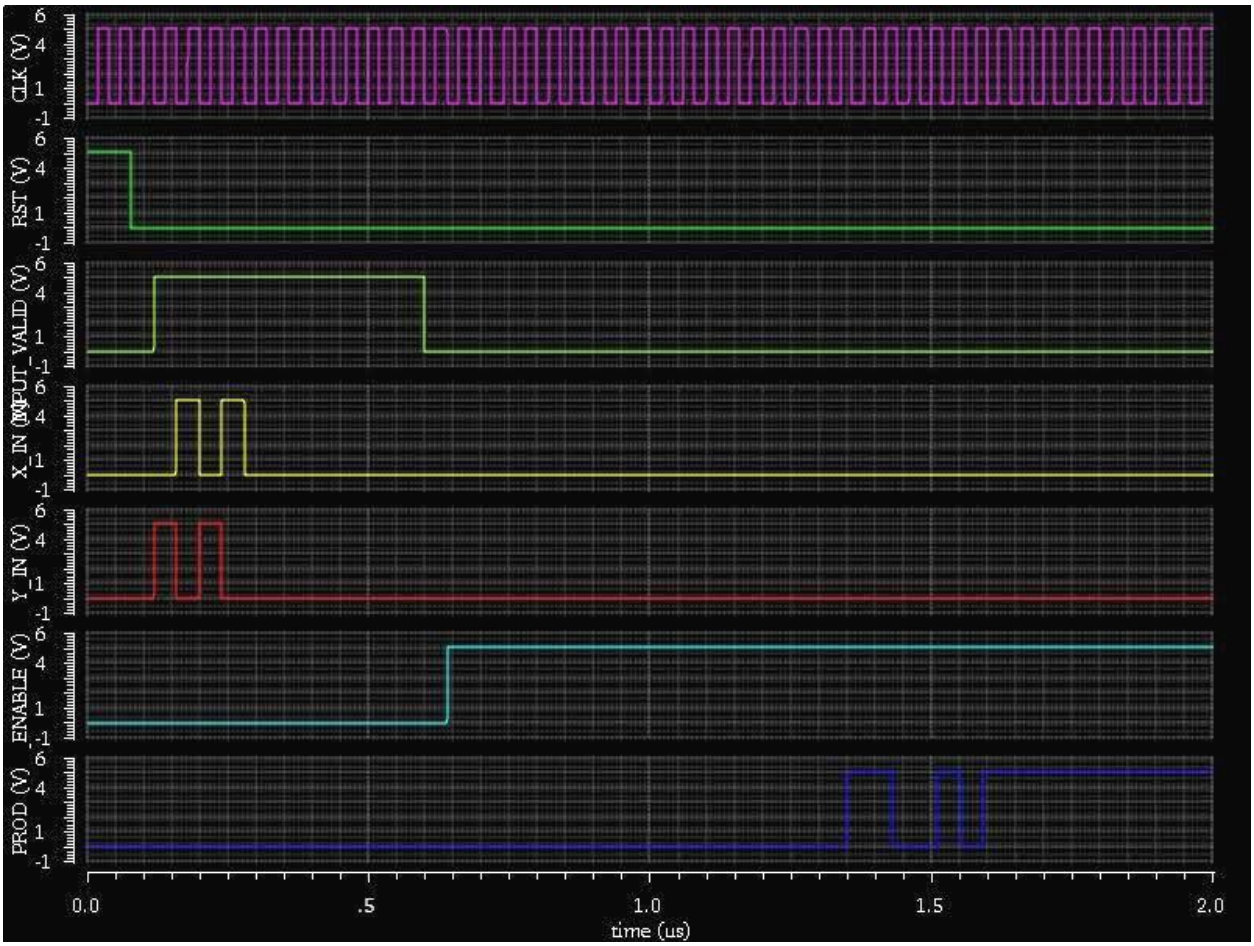
- All 0s



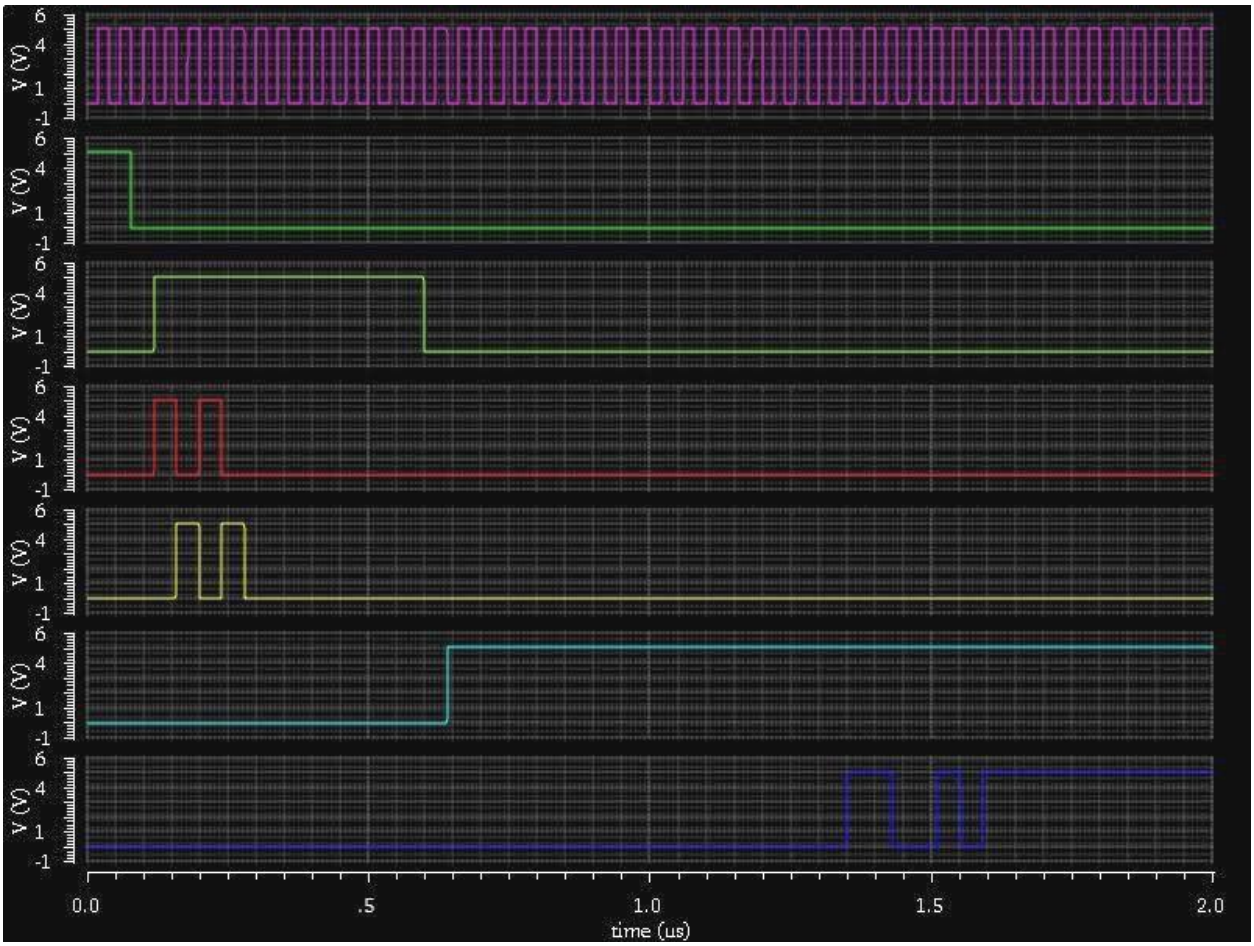
- All 1s


CLK (V)
RST (V)
INPUT_VALID (V)
X_IN (V)
Y_IN (V)
ENABLE (V)
PROD (V)
6
4
1
-1
0.0
.25
.5
.75
1.0
1.25
1.5
time (us)

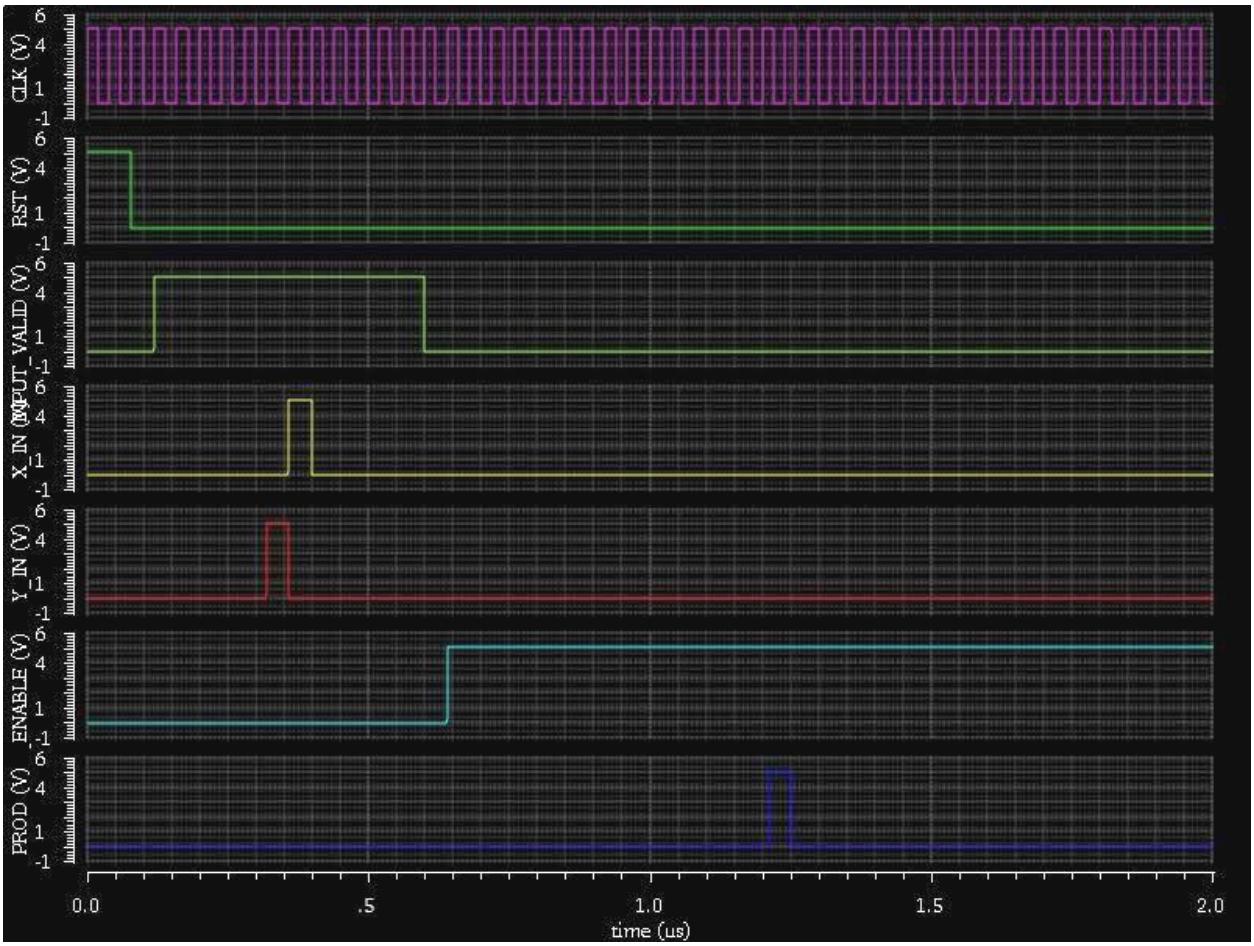
- 10 x 5


CLK (V)
RST (V)
INPUT_VALID (V)
X_IN (INPUT
Y_IN (V)
ENABLE (V)
PROD (V)
6
4
1
-1
0.0
.5
1.0
1.5
2.0
time (us)

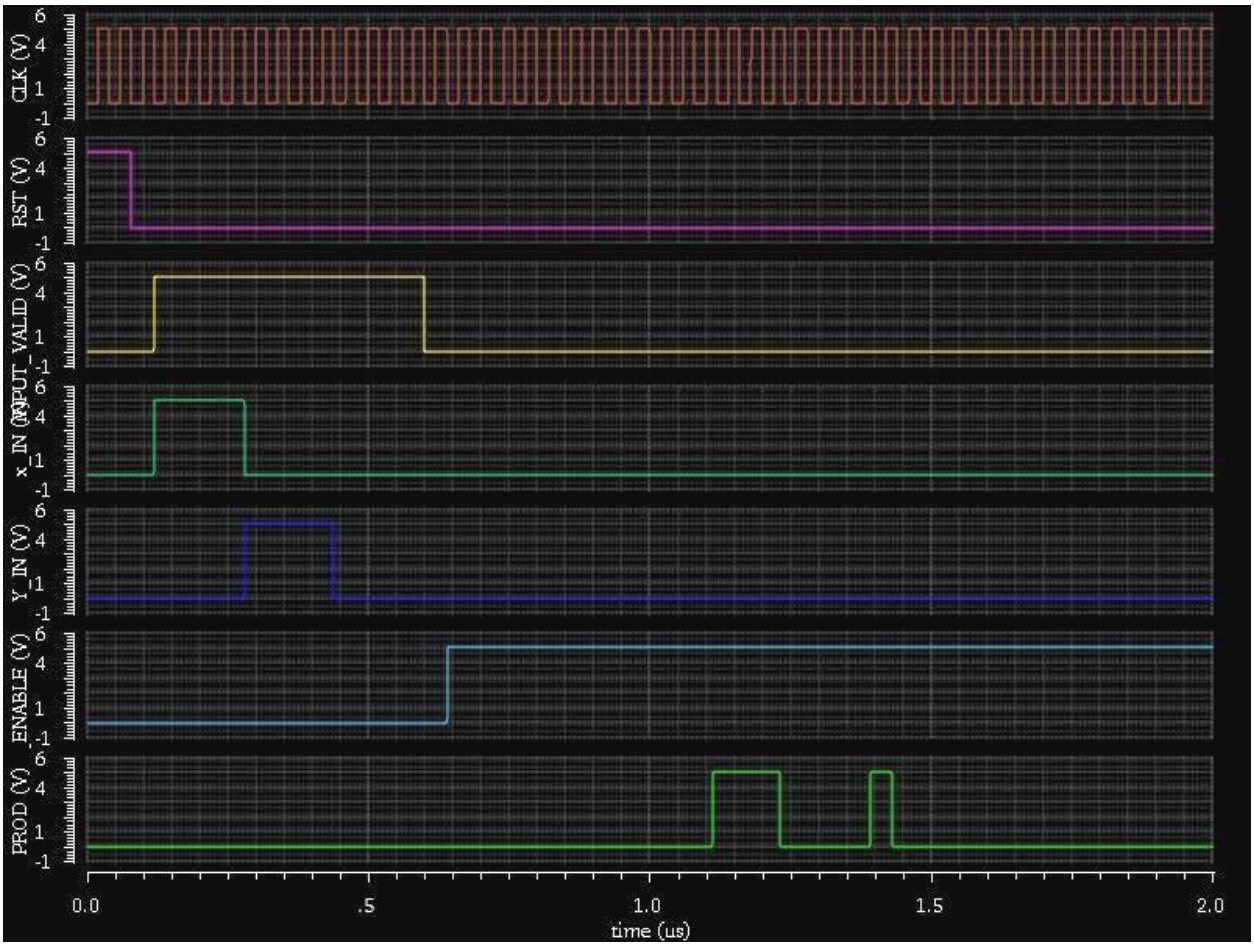
- 5 x 10



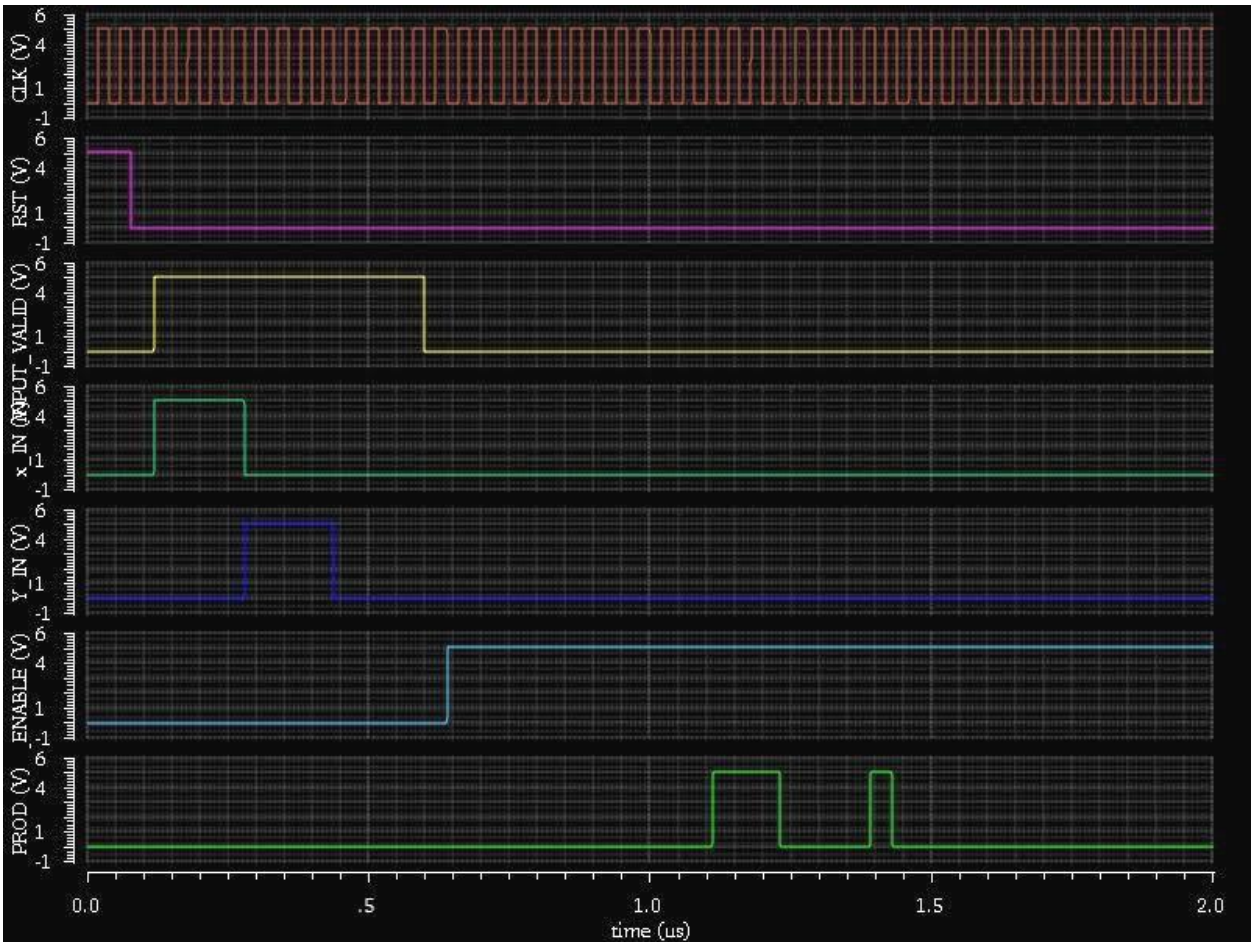
- 64 x 32


CLK (V)
RST (V)
INPUT_VALID (V)
X_IN (INPUT)
Y_IN (V)
ENABLE (V)
PROD (V)
6
4
1
-1
0.0
.5
1.0
1.5
2.0
time (us)

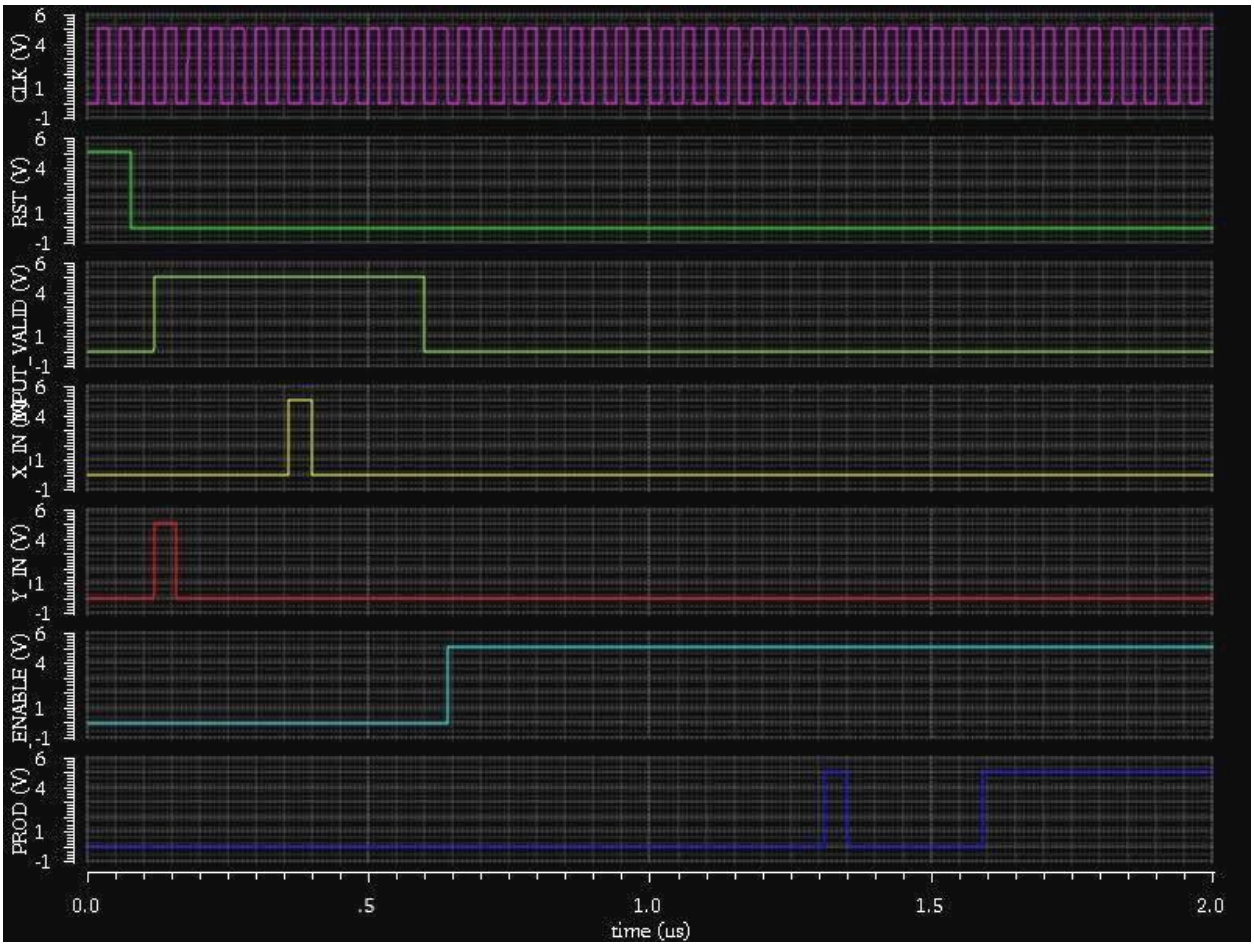
- 00001111 x 11110000



- 11110000 x 00001111

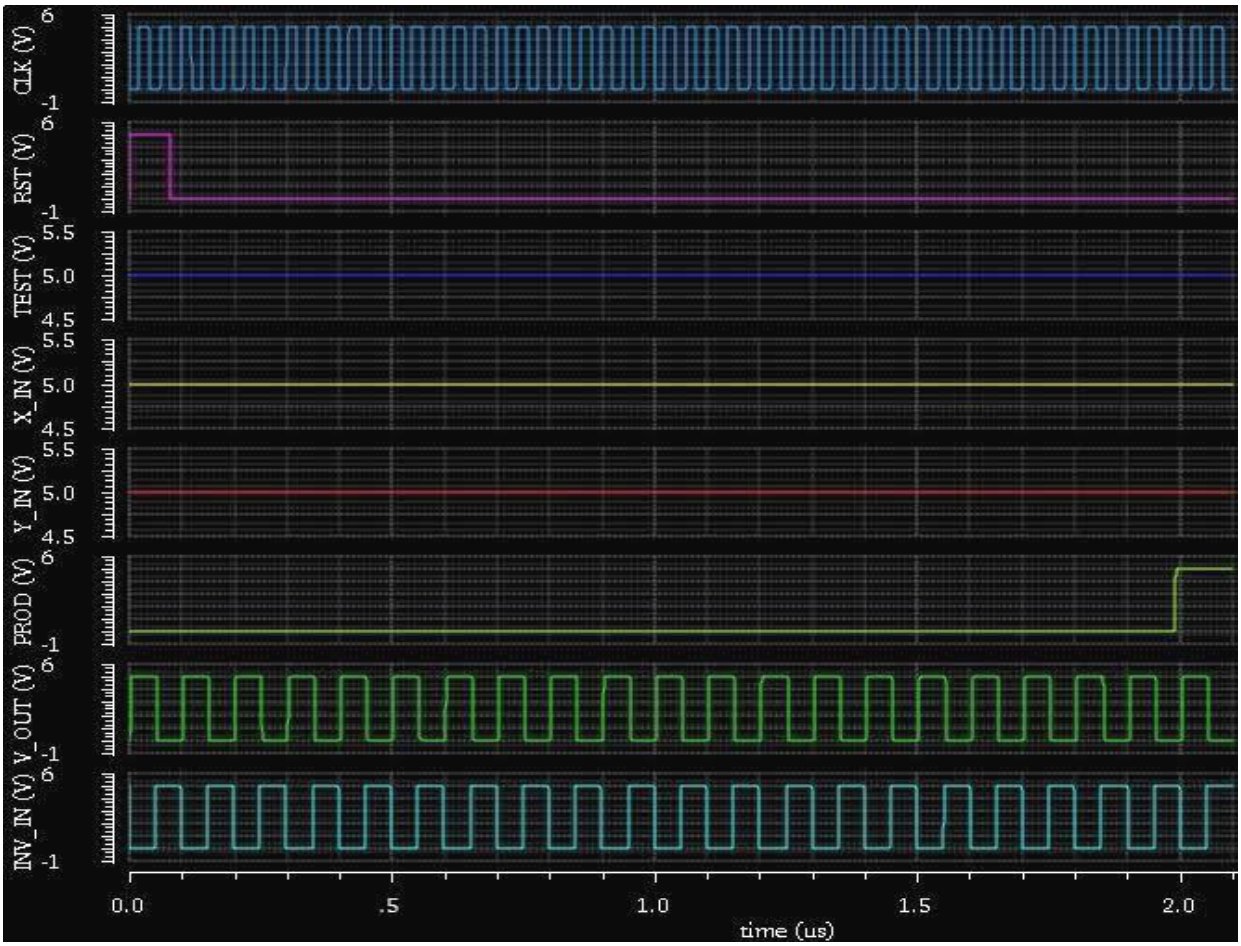


- 64 x1


CLK (V)
RST (V)
INPUT_VALID (V)
X_IN (V)
Y_IN (V)
ENABLE (V)
PROD (V)
6
4
1
-1
0.0
.5
1.0
1.5
2.0
time (us)

- Test Inv / Scan Chain

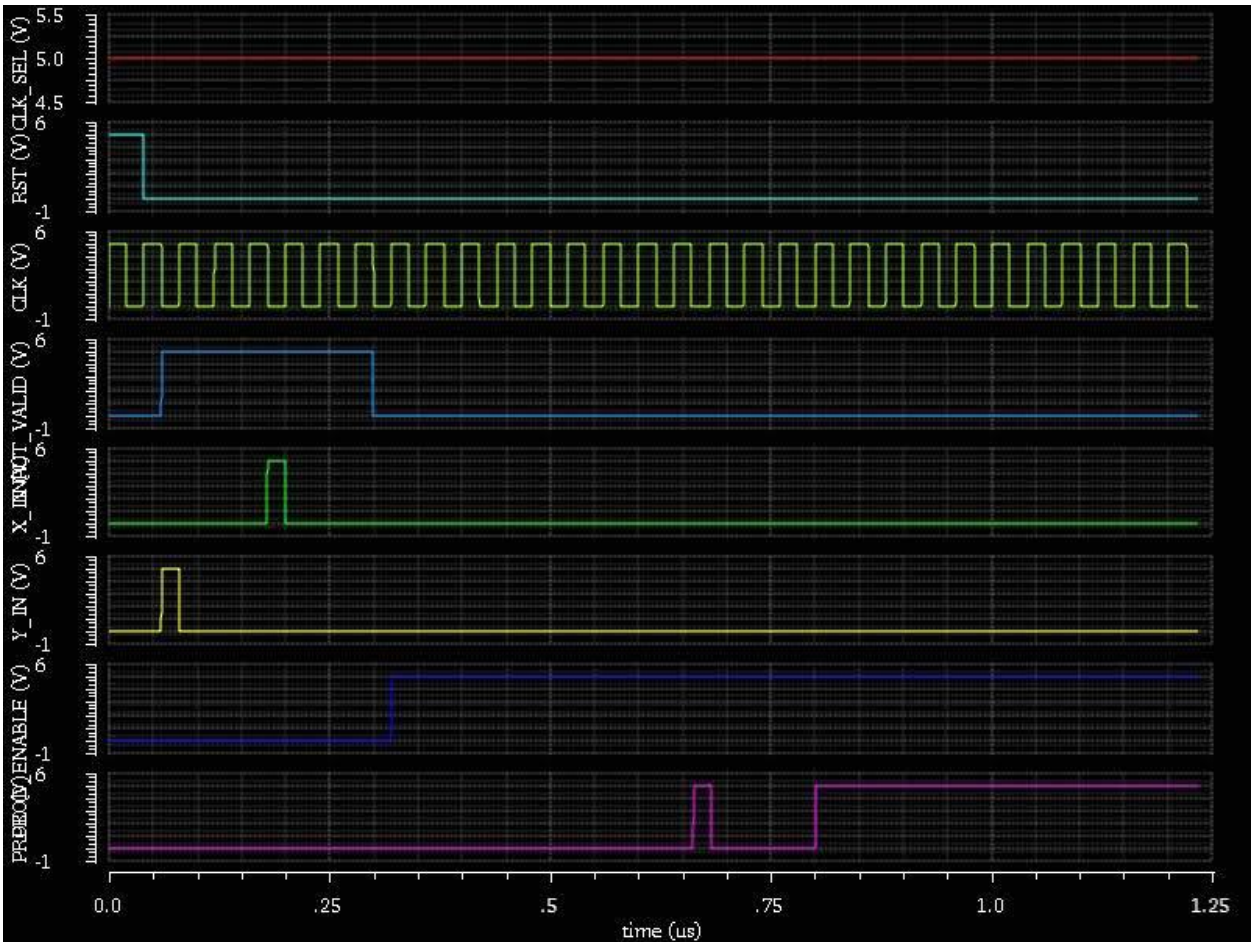
PROD_ENABLE and INPUT_VALID are set low during this simulation, but have no effect on the use of the scan chain.



B.4 Extra Credit Results -- **For each of the following stimuli provide a waveform screenshot (1 per page).**

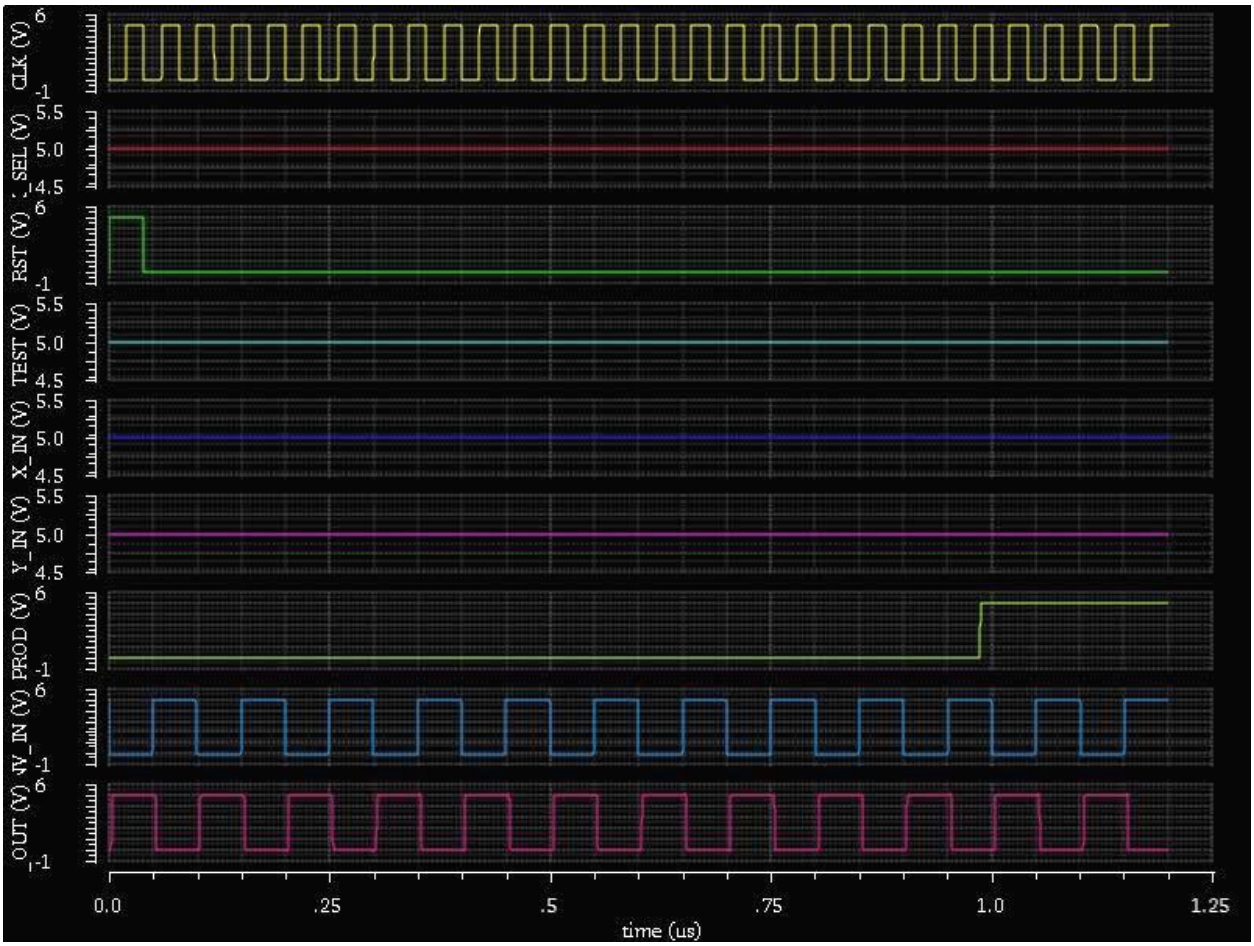
- All 0s
- All 1s
- 10 x 5
- 5 x 10
- 64 x 32
- 00001111 x 11110000
- 11110000 x 00001111

- 64 x1



External Clock cycle time = 40ns (Not used)
Internal Clock cycle time = 20ns

- Test Inv / Scan Chain



PROD_ENABLE and INPUT_VALID are set low during this simulation, but have no effect on the use of the scan chain.

C. Design Experience – Each team member should write a paragraph on their design experience. What could you have done differently, any design issues, any re-designs of blocks, etc.

C.1 Team Member 1 (ANDRES IZURIETA-OCHOA)

Given another chance at doing this project, I probably would have taken a more critical approach than a liberal one with respect to the layouts I did and the ones my partners designed. Small things such as incorrectly oriented buffers, wires that weren't connected properly took the majority of the time the project demanded. And that's without considering the memory swapping and the bigger design than the average 8x8 multiplier the simulation had to account for. Additionally, I feel the bulk of the work could have been more effectively distributed among all team members since some designs required more time to implement than others. Strangely, the registers were the limiting factor as to how many bits the design could implement. A more efficient flipflop design could have permitted the implementation of a 16x16 bit or even 18x18 bit multiplier given the dimensions of the adders. Unfortunately this could not be accomplished due to time constraints and extremely slow simulation times. All that in consideration, the project was a demanding one, but an interesting one that granted a sense of great accomplishment.

C.2 Team Member 2 (ARPIT SALUJA)

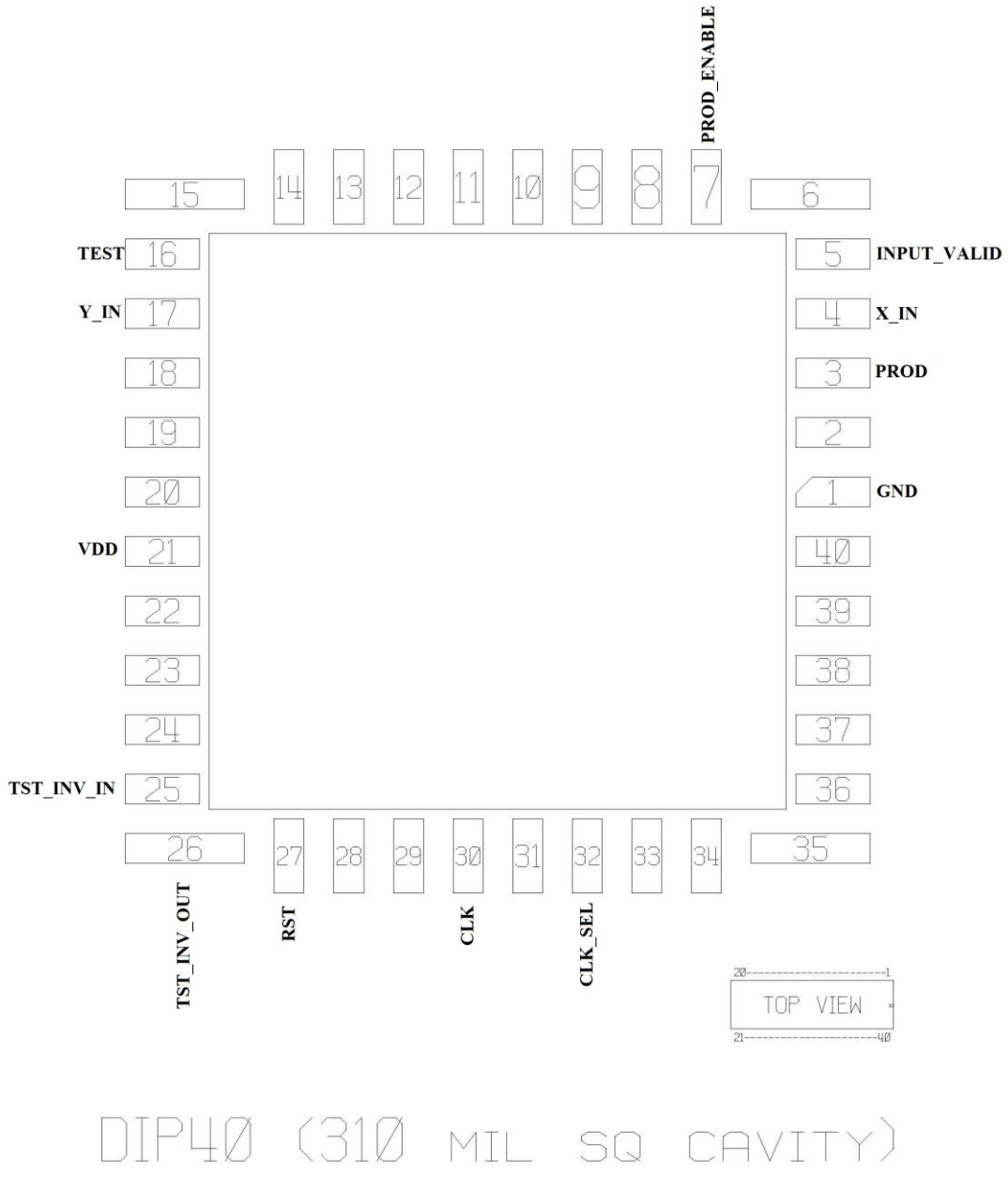
If I could do the lab again I would make changes to the way I address flattening issues. Instead of working with a flattened layout, I would keep everything as instances, make my modifications, and flatten a copy of my design for running PEX. This would make it easy to ensure that fewer mistakes are made, and to make large-scale modifications if necessary (all benefits of having instances). The only design issue we faced was choosing the number of input and output bits to accommodate. Our decision rested on two metrics: simulation time and bonus points. In the end, a 12 X 12 multiplier was decided upon because it made simulation times bearable while also providing the opportunity for extra credit. Other than that the project went smoothly, no blocks had to be re-designed.

C.2 Team Member 3 (MUHAIMEN SHAMSI)

One of the design issues I faced was making the internal clock oscillate from the beginning of the simulation. To fix this, I ANDed the internal clock with an enable signal which was always connected to Vdd.

D. User Document/Data Sheet (1-2 pages) – **Write a 1-2 user document/datasheet which should provide relevant information to the end user. If your chip is sold as a component, what should the user know so that (s)he can use it in their system (see a sample datasheet provided). Should have the following information: brief description, features, applications, pin diagram, timing diagram (how to apply inputs, how to register the output), test/normal modes. Note that the packaging is done with DIP 40 package. The bonding diagram:**

https://www.mosis.com/files/Packaging/Ceramic/dip40-diagram.pdf



PINS:

-Pin 1:	GND	
-Pin 3:	PROD	Output pin
-Pin 4:	X_IN	Input pin
-Pin 5:	INPUT_VALID	Input register enabler(high)
-Pin 7:	PROD_ENABLE	Output register enabler(high)
-Pin 16:	TEST	Chooses between test mode(high) and product mode(low)
-Pin 4:	Y_IN	Input pin
-Pin 21:	VDD	
-Pin 25:	TEST_INV_IN	Input for inverter test
-Pin 26:	TEST_INV_OUT	Output for inverter test
-Pin 27:	RST	Resets register(high)
-Pin 30:	CLK	Input for external clock
-Pin 32:	CLK_SEL	Chooses between internal clock(high) and external clock(low)

This array multiplier accepts two 12-bit positive binary numbers as inputs and produces a 24-bit product. The inputs are fed in serially and shifted out serially. Additionally, if need be, the chip can run a test mode to see if all the registers are shifting as needed. Each register can be clocked by either the internal clock (20ns) already implemented or an external clock (suggested at around 20ns). The chip also provides a supplementary inverter to ensure the chip is functing properly which receives input from pin 25 and is output to pin 26.

NOTE: It is suggested that pin 27 be set to high for one clock cycle before modes and in between them

NORMAL MODE:
This mode is available in order to output the desired multiplication operation and is activated by setting pin 16 to low for the duration of the operation. The inputs are fed in serially to two registers from pins 5 and 17 and the product is shifted out serially to pin 3. Each input bit must last one clock cycle for a total of 12 cycles. Pin 5 will be set to high for the duration of these 12 clock cycles. Once these 12 clock cycles are over, one extra clock cycle must be left before pin 7 can be set to high in order to allow the product register to shift. Once pin 7 is set to high, it must be held high for 24 clock cycles. This accounts for a total of 37 clock cycles before the operation is complete.

TEST MODE:
This mode is provided as a feature to make sure all registers in the chip are shifting properly. To activate Scan chain mode, pin 16 is set to high for the duration of the operation. The input is fed in serially through pin 4 and shifted out serially to pin 3. Each input bit must last one clock cycle for a total of 48 cycles before the first output bit reaches pin 3.