1 Electronics Design

By applying a voltage, V, and measuring the current, I, the conductance, G, of a tunnel junction between tips can be determined using $I = GV$. From this macroscopic value the underlying quantum tunnelling transmission can be seen and correlated with optical measurements to gain a sense of spatial separation and the extent of charge transfer across the gap.

The experimental chamber contains two triaxial connectors, one attached to each Cu tip clamp, to send and return electronic signals, permitting biasing and electrical measurement of the gap between atomic force microscopy (AFM) tips. Electronic signals are controlled and redirected using a control box, which attaches to the chamber triax cables. Electronics are split between an a.c. circuit that drives a resonant capacitive tip alignment procedure and a d.c. circuit for electrical measurements. The d.c. electronics are further split into low and high bandwidth measurement circuits. The low bandwidth ($< 10\,\text{Hz}$) circuit measures electronics continually over long time periods, typically giving spatial information linked to sample separation. The high bandwidth circuit operates on a trigger to capture single shot events on much shorter time scales. Both d.c. circuits are typically ran simultaneously while the a.c. and d.c. circuitry is manually switchable. A block schematic of this system is shown in Figure 1.

The a.c. circuit consists of a signal generator connected to a $20\times$ voltage amplifier to drive the junction capacitance. This is used to resonantly drive an AFM cantilever into oscillation and align tips into a tip-to-tip dimer configuration. A $40\,\text{k}\Omega$ current limiting resistor is placed after the amplifier to prevent damage to the tip junction in the event of a direct conductive contact.[1] The return signal from the circuit is then terminated at ground. The separate d.c. circuit consists of a source-meter unit (SMU) circuit for low-bandwidth (sub-10 Hz) measurements with a switchable high-bandwidth measurement extension. The SMU (Keithley 2635A) is used to apply a voltage across the junction and measure the current. The switchable high-bandwidth path routes the current through a $10^4\times$ gain transimpedance amplifier (Femto DLPCA-200) and then a 1 MHz low-pass filtering stage (SRS SR560). The amplified voltage is measured on a digital storage oscilloscope (DSO) (Agilent DSOX-2012) with the shield becoming the return path of the current back to the SMU via the routing box.[2]

The fundamental feature of combined circuity is their separability. The a.c. circuit is not required to be low-noise but the d.c. circuitry is used to measure low-level tunnelling currents. For the d.c. circuit to operate correctly it must be isolated from any other electronics. The a.c. circuit remains completely disconnected and held at ground when the d.c. circuit is engaged, and vice-versa. To achieve measurements of small, sensitive currents, reducing the noise level to a minimum is imperative. The noise floor at low bandwidths, along with the current range of the SMU, sets the minimum current which can be measured. The sub-10 Hz bandwidth of

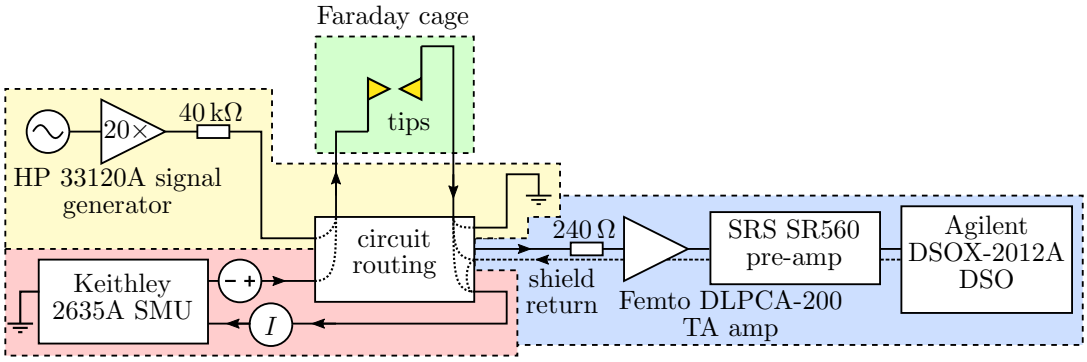

Figure 1: Block schematic of the electrical circuit design. The central routing box allows switching between a.c. and d.c. circuits and low-and high-bandwidth d.c. measurements. The a.c. circuit is used to align two AFM probes together while the d.c. circuit is used to measure spatially dependent signals from the gap between two AFM probes.

[1] The optimum resistance value is calculated using $R = V/I_{\text{limit}}$ where $V = 10\,\text{V}$ typically and a safe current limit is $I_{\text{limit}} = 250\,\mu\text{A}$. This gives a resistance of $40\,\text{k}\Omega$.

[2] An alternative strategy for converting a current into a voltage is to pass the current through a well-known resistor and differentially amplify the voltage drop across the resistor. This was not used since the transimpedance amplifier was readily available and of a low noise specification.

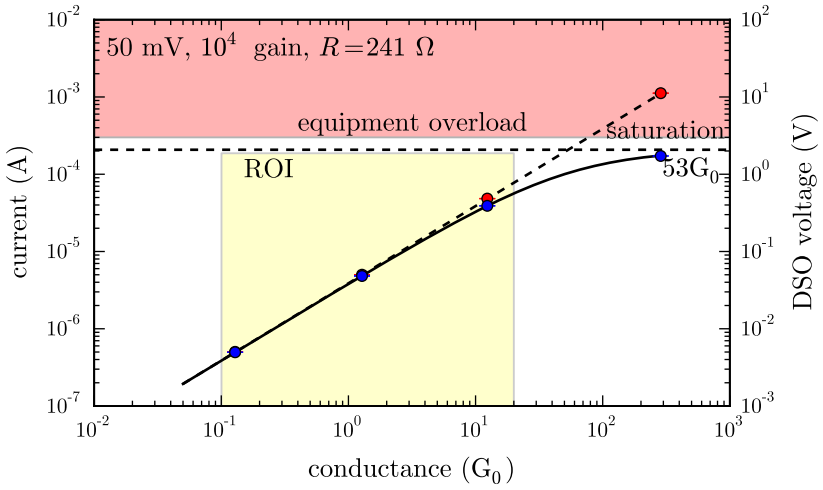

Figure 2: Characterisation of electronic measurements based on junction conductance. Solid lines show the calculated SMU currents and amplified voltages for given junction conductances under a 50 mV applied voltage with a 241 Ω current limiting resistor to prevent saturation (high bandwidth circuit). Dashed lines show the calculated oscilloscope voltages for the case without the current limiting resistor (low bandwidth circuit). Circles mark experimentally measured points using resistors in place of the junction in both circuits. Error bars are present but too small to visibly see.

the SMU removes much of the noise during spatial measurements. Correct grounding of all electronic chassises to a single point (the SMU) shields electromagnetic interference (EMI) and prevents ground loops from inducing current offsets. Triax cabling is used with guarded connections where possible to prevent leakage currents.

A standard operating voltage between 10–50 mV is used to drive high quality tunnelling currents. Conductances greater than $10^{-8}G_0$ are then clearly measured above noise. Using lower voltages means currents are only observable for larger tunnelling conductances, i.e. smaller gap widths, whilst higher voltages lead to larger overall currents and electrostatic interaction between tips, both of which should be avoided to prevent damage to the tip junction. To maintain good scan speeds the current range is restricted to 10 nA with a ±10 pA error, since more accurate ranges have longer settling times. Limiting the current range is the dominant source of current measurement error as opposed to the noise floor.

Noise on the SMU is measured by varying a series resistance in place of the tip junction and taking the standard deviation of 20 measurements across a range of voltages in 10 mV steps. The open circuit noise measures ±10 pA. Johnson noise for such a circuit is estimated to be around 1 pA. If current measurements are strictly limited by the current range then the percentage error of each range should be equivalent. This is not the case, with the percentage error increasing from 10^{-3}% to 10^{-2}% as the current decreases to the nA range, signifying the approach of the noise floor. Actual noise levels around ±100 pA are found at 50 mV with a 1 MΩ ($10^{-2}G_0$) junction resistance characteristic of electron tunnelling. Given the small percentage errors, circuit noise is not a problem for tunnelling current measurements.

Noise predominantly affects high bandwidth measurements, where it limits the conductance resolution and minimum trigger level for single shot measurements. High bandwidth noise typically originates from digital circuitry, e.g. switch-mode power supplies and powered relays. Power supplies are therefore covered in foil to shield EMI and manual toggle switches are used instead of remote-controlled relays. Applying a 1 MHz filter goes some way to reducing high bandwidth noise. Any more filtering smooths measurements too much.

The maximum allowed current is set to 250 µA to prevent damage to contacted AFM tips. Upon surpassing this limit the SMU attenuates the voltage to reduce the current. A current limiting resistor is also included in the circuit to ensure a hardwired maximum and to prevent overloading of the DSO and transimpedance amplifier. The value of this resistor is calculated using,

$$R = \frac{AV}{0.95V_{\text{overload}}}, \tag{1}$$

where V is the operating voltage, A is the amplifier gain and V_{overload} is the minimum overload voltage for the

circuit at a given voltage V (determined by whichever overload voltage is surpassed first, either the maximum transimpedance input current of 5 mA pre-amplification or the maximum output voltage of 5 V). The pre-factor of 0.95 is chosen to prevent the current getting close to overloading. For a 50 mV bias and 10^4 gain the ideal resistance is 175 Ω but for a 10 mV bias with 10^5 gain the idea resistance becomes 350 Ω. To accommodate a range of voltages and both gain settings, a middle resistance of 241 Ω is used, which provides some headroom for increasing the voltage. The calculated current and DSO voltage as a function of junction conductance for the low and high bandwidth circuits is shown in Figure 2. Excellent agreement with experimental current and voltage measurements taken with a set of resistors demonstrates the circuit behaves exactly as predicted.

The presence of the current limiting resistor means that measured circuit conductances, G_{measured}, contain a series resistance that needs to be taken into account. Junction conductances are calculated using,

$$G_{\text{junction}} = \left(G_{\text{measured}}^{-1} - R\right)^{-1}. \tag{2}$$

The maximum conductance value that can be measured is found by inverting the limiting resistance using $G_{\max} = 1/R$. For a 50 mV bias the conductance limit is 53G_0. Conductances greater than this value are small compared to the series resistance and are therefore much harder to measure reliably. For this reason the range of interesting conductances ($G < 20\text{G}_0$) is ideally kept to the linear part of the current curve by limiting the voltage and gain.