PROGRAM OF EVENTS

Links will be emailed to registrants.

Wednesday, July 7th, 2021 (All times are PDT)

Start Time	End Time	Event
8:00 AM	8:15 AM	**Opening Remarks**
8:15 AM	9:00 AM	Keynote I "21st-Century NanoSystems for Abundant-Data Computing: The N3XT 1,000X" Session Chair: Prof. Deming Chen, University of Illinois at Urbana-Champaign, USA Speaker: Prof. Subhasish Mitra, Stanford University, USA
9:00 AM	9:10 AM	**Break**
9:10 AM	10:10 AM	Paper Session 1 - Hetergeneous designs and architectures I Session Chair: Dr. Meng Li, Facebook, USA 1.1 "To buffer, or not to buffer? A case study on FFT accelerators for ultra-low-power multicore clusters" Luca Bertaccini, Luca Benini and Francesco Conti, ETH Zurich, Switzerland 1.2 "Algorithm and Hardware Co-Design for FPGA Acceleration of Hamiltonian Monte Carlo Based No-U-Turn Sampler" Yu Wang and Peng Li, University of California, Santa Barbara, USA 1.3 "Improving Inference Lifetime of Neuromorphic Systems via Intelligent Synapse Mapping" Shihao Song, Twisha Titirsha and Anup Das, Drexel Universi ty, USA 1.4 "A lightweight ISE for ChaCha on RISC-V" Ben Marshall, Daniel Page and Thinh Hung Pham, University of Bristol, UK 1.5 "RFC-HyPGCN: A Runtime Sparse Feature Compress Accelerator for Skeleton-based GCNs Action Recognition Model with Hybrid Pruning" Dong Wen, Jingfei Jiang, Jinwei Xu, Kang Wang, Tao Xiao, Yang Zhao and Yong Dou , National University of Defense Technology, China 1.6 "Virtual Circuit-Switching Network with Flexible Topology for High-Performance FPGA Cluster" Tomohiro Ueno, Atsushi Koshiba and Kentaro Sano, RIKEN, Japan

10:10 AM	11:10 AM	Lunch Break/Poster Session I Session Chair: Prof. Caiwen Ding, University of Connecticut, USA
11:10 AM	12:10 PM	Paper Session 2 (Special Session: Real-time AI) Session Chair: Dr. He Li, University of Cambridge, UK 2.1 “Real-time super resolution system of 4K-video based on deep learning” He Li, University of Cambridge, UK 2.2 “An efficient real-time object detection framework on resource-constricted devices via software and hardware co-design” Yu Bai, California State University, Fullerton, USA 2.3 “Binary Complex Neural Network Acceleration on FPGA” Caiwen Ding, University of Connecticut, CT, USA 2.4 “How to Reach Real-Time AI on Consumer Devices? Solutions for Programmable and Custom Architectures” Stylianos I. Venieris, Samsung AI Center-Cambridge, UK
12:10 PM	12:20 PM	**Break**
12:20 PM	1:20 PM	Paper Session 3 - ML algortihms and Tools Session Chair: Prof. Siddharth Garg, New York University, USA 3.1 "Talos: A Weighted Speedup-Aware Device Placement of Deep Learning Models" Yuanjia Xu, Heng Wu, Wenbo Zhang, Yuewen Wu, Tao Wang, Chen Yang and Heran Gao, Institution of Software, Chinese Academy of Sciences, China 3.2 "Hodgkin-Huxley-Based Efficient Neural Simulation with Networks Connecting to Near-Neighbor Neurons" Masashi Ogaki and Yukinori Sato, Toyohashi University of Technology, Japan 3.3 "Accelerating Recurrent Neural Networks for Gravitational Wave Experiments" Zhiqiang Que, Erwei Wang, Umar Marikar, Eric Moreno, Jennifer Ngadiuba, Thea Aarrestad, Hamza Javed, Bartłomiej Borzyszkowski, Vladimir Loncar, Sioni Summers, Maurizio Pierini, Cheung Peter and Wayne Luk, Imperial College London, UK 3.4 "Array-Aware Neural Architecture Search" Krishna Teja Chitty-Venkata and Arun Somani, Iowa State University, USA 3.5 "TwinDNN: A Tale of Two Deep Neural Networks" Hyunmin Jeong and Deming Chen, University of Illinois at Urbana-Champaign, USA 3.6 "Image caption generation method based on an interaction mechanism and scene concept selection module" Liping Zhang and Qin Lu, Qilu University of Technology, China
1:20 PM	1:30 PM	Break

1:30 PM	2:15 PM	Keynote II "Scalable ML Architectures for Real-time Energy-efficient Computing" Session Chair: Dr. Mondira (Mandy) Deb Pant, Academic Research Director at Intel, USA Speaker: Prof. R. Iris Bahar, Brown University, USA

Thursday, July 8th, 2021 (All times are PDT)

Start Time	End Time	Event
8:00 AM	9:30 AM	Panel: Coarse-Grained Reconfigurable Arrays and their Opportunities as Application Accelerators Moderator: Prof. Jason Anderson, University of Toronto, Canada Panelists: Dr. Kentaro Sano, RIKEN, Japan Prof. Shouyi Yin, Tsinghua University, China Dr. Cheng Tan, Pacific Northwest National Lab (PNNL), USA Prof. Hideharu Amano, Keio University, Japan Prof. Masato Motomura, Tokyo Institute of Technology, Japan Prof. Yasuhiko Nakashima, Nara Institute of Science and Technology (NAIST), Japan
9:30 AM	10:15 AM	Keynote III "Amplifying Human Potential with AI" Session Chair: Prof. Yingyan (Celine) Lin, Rice University Speaker: Intel Fellow Lama Nachman, Intel Corporation, USA
10:15 AM	10:25 AM	**Break**
10:25 AM	11:25 AM	Paper Session 4 - Green designs and security Session Chair: Dr. Richard Chow, Intel, USA 4.1 "Number Theoretic Transform Architecture suitable to Lattice-based Fully-Homomorphic Encryption" Rogério Paludo and Leonel Sousa, INESC-ID, Instituto Superior Técnico, Universidade de Lisboa, Portugal. Portugal 4.2 "ABACa: Access Based Allocation on Set Wise Multi-Retention in STT-RAM Last Level Cache" Sukarn Agarwal and Shounak Chakraborty, Indian Institute Of Technology (BHU) Varanasi, India 4.3 "DARM: A Low-Complexity and Fast Modular Multiplier for Lattice-Based Cryptography" Xiao Hu, Minghao Li, Jing Tian and Zhongfeng Wang, Nanjing University, China 4.4 "XDIVINSA: eXtended DIVersifying INStruction Agent to Mitigate Power Side-Channel Leakage" Thinh Hung Pham, Ben Marshall, Alexander Fell, Siew-Kei Lam and Daniel Page, University of Bristol, Department of Computer Science, UK 4.5 "Memory-aware Efficient Deep Learning Mechanism for IoT Devices" Jishnu Banerjee, Sahidul Islam, Wei Wei, Chen Pan, Dakai Zhu and Mimi Xie, University of Texas at San Antonio, USA 4.6 "AERO: Towards Energy-Efficient Autonomous Flight in MAVs Using Approximate Execution"

		Ben Li, Jingweijia Tan and Kaige Yan, Jilin University, China
11:25 AM	12:25 PM	Lunch Break/Poster Session II Organizing Chair: Prof. Caiwen Ding, University of Connecticut
12:25 PM	1:25 PM	Paper Session 5 (Special Session: Design Automation of Robust and Secure Machine Intelligence) Session Chair: Prof. Xun Jiao, Villanova University, USA 5.1 “On the Efficacy of Privacy-Preserving Neural Network Inference based on Hardware Security Primitives” Song Bian, Kyoto University, Japan 5.2 “Assessing Robustness of Hyperdimensional Computing Against Errors in Associative Memory” Xun Jiao, Villanova University, USA 5.3 “Design Automation for Safe and Robust Autonomous Systems” Qi Zhu, Northwestern University, USA 5.4 “Towards automatic and agile ML/AI accelerator design with end-to-end synthesis” Jeff (Jun) Zhang, Harvard University, USA
1:25 PM	2:25 PM	Paper Session 6 - Hetergeneous designs and architectures II Session Chair: Prof. Zhenman Fang, Simon Fraser University, Canada 6.1 "ASBNN: Acceleration of Bayesian Convolutional Neural Networks by Algorithm-hardware Co-design" Yoshiki Fujiwara and Shinya Takamaeda-Yamazaki, The University of Tokyo, Japan 6.2 "A novel Ring-based small-world NoC for Neuromorphic Processor" Yuchen Qiu, Chao Xiao, Linghui Peng, Junhui Wang, Ziyang Kang, Shiming Li and Lei Wang, National University of Defense Technology, China 6.3 "Double-Pumping the Interconnect for Area Reduction in Coarse-Grained Reconfigurable Arrays" Xinyuan Wang, Tianyi Yu, Hsuan Hsiao and Jason Anderson, University of Toronto, Canada 6.4 "An Efficient Hardware Architecture for Sparse Convolution using Linear Feedback Shift Registers" Murad Qasaimeh, Joseph Zambreno and Phillip Jones, Iowa State University, USA 6.5 "WinoCNN: Kernel Sharing Winograd Systolic Array for Efficient Convolutional Neural Network Acceleration on FPGAs" Xinheng Liu, Yao Chen, Cong Hao, Ashutosh Dhar and Deming Chen, University of Illinois at Urbana-Champaign, USA 6.6 "FlexACC: A Programmable Accelerator with Application-Specific ISA for Flexible Deep Neural Network Inference" En-Yu Yang, Tianyu Jia, David Brooks and Gu-Yeon Wei, Harvard University, USA
2:25 PM	2:40 PM	Closing Remarks