實驗主題(Lab07)

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Exercise 1:

- The simplified functions (Circuit 1)
  - $z = D'$
  - $y = CD+C'D'$
  - $x = B'C+B'D+BC'D'$
  - $w = A+BC+BD$
- Another implementation (Circuit 2)
  - $z = D'$
  - $y = CD+C'D' = CD + (C+D)'$
  - $x = B'C+B'D+BC'D' = B'(C+D)+B(C+D)'$
  - $w = A+BC+BD = A+B(C+D)$
- Draw the logic diagrams of Circuit 1 and Circuit 2, and then verify Circuit 1 = Circuit 2 (using Verilog Dataflow modeling)

Exercise 2:

- Derive the following Boolean functions using Karnaugh maps
- $S = z\oplus(x\oplus y)$, $C = xy + xz + yz$ (Circuit 1)
- Draw the logic diagram of Circuit 1

- Derive the following Boolean functions using Karnaugh maps
- $S = z\oplus(x\oplus y)$, $C = z(x\oplus y)+xy$ (Circuit 2)
- Draw the logic diagram of Circuit 2
- Verify Circuit 1 = Circuit 2
  (using Verilog Structural level modeling)

Exercise 3:

- Design and verify the 8-bit ripple-carry adder composed of eight full-adders (using Verilog Structural level modeling)

實驗內容

一、Exercise 1:

- The simplified functions (Circuit 1)
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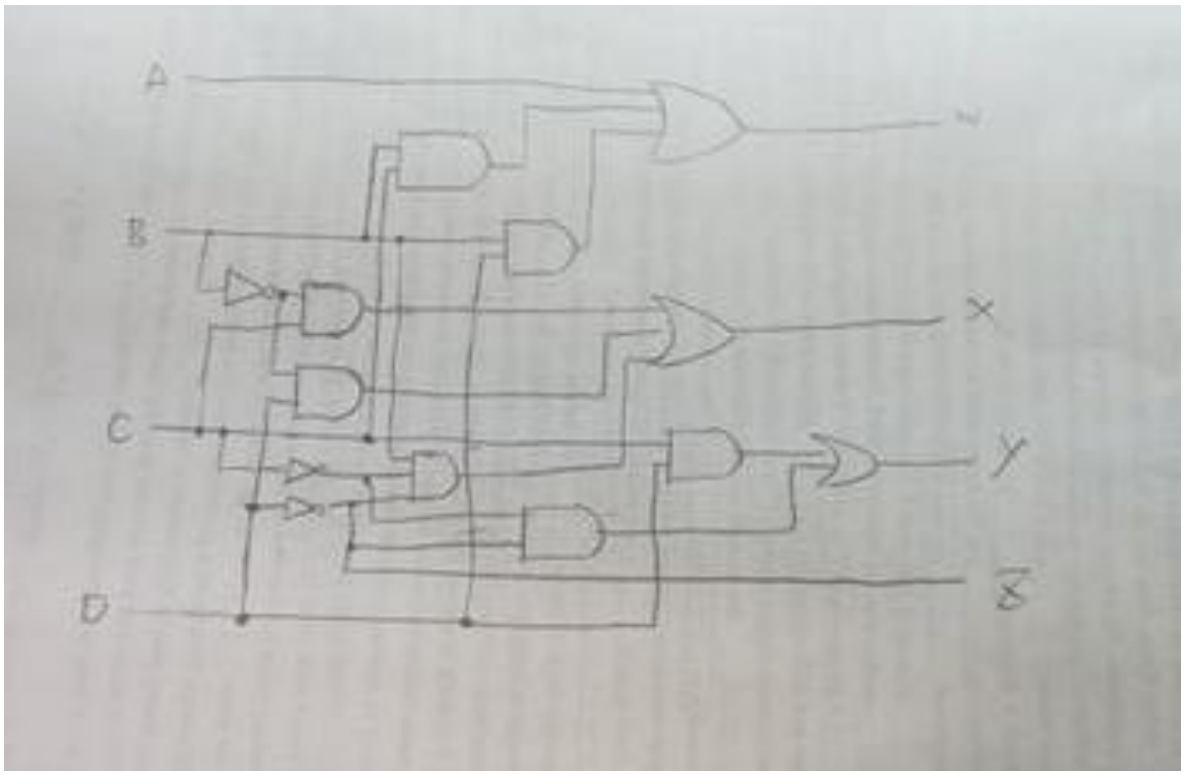
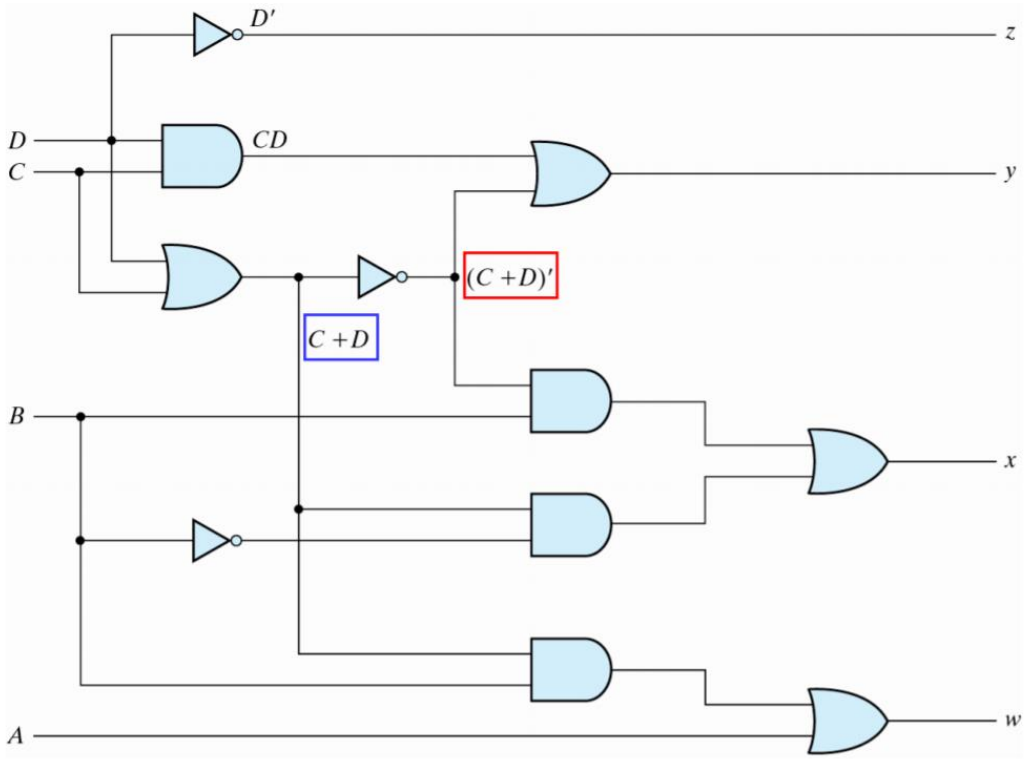
Circuit 1 :

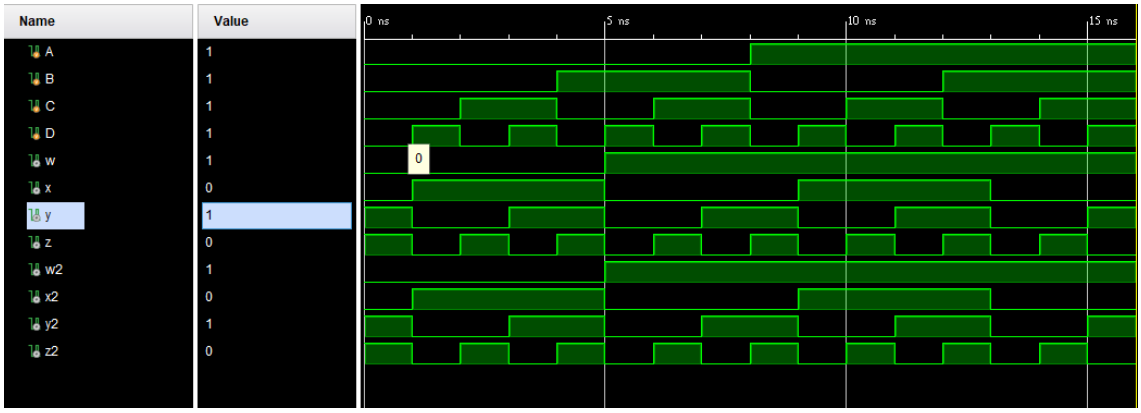


Circuit 2 ：




```
1   `timescale 1ns / 1ps
2
3   module exercise_1(w,x,y,z,w2,x2,y2,z2, A,B,C,D);
4       output w,x,y,z,w2,x2,y2,z2;
5       input A,B,C,D;
6       assign z = ~D;
7       assign y = (C & D)|(~C & ~D);
8       assign x = (~B & C)|(~B & D)|(B & ~C & ~D);
9       assign w = A|(B & C)|(B & D);
10
11      assign z2 = ~D;
12      assign y2 = (C & D)|~(C | D);
13      assign x2 = (~B & (C | D))|(B & ~(C | D));
14      assign w2 = A|(B & (C | D));
15  endmodule
16
```

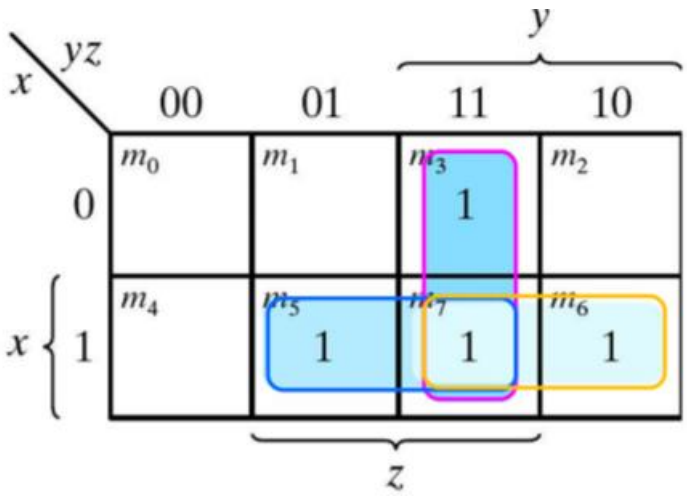
Curcuit 2 中將(C+D)都提出來，在 Schematic 中可以使成本節省，體積變小



w=w2,x=x2,y=y2,z=z2，所以 Circuit 1= Curcuit 2

二、Exercise　2:

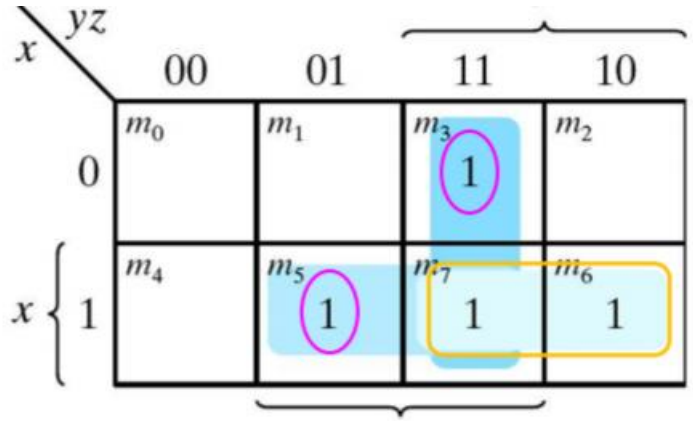
- Derive the following Boolean functions using Karnaugh maps
- $S = z \oplus (x \oplus y)$, $C = xy + xz + yz$ (Circuit 1)
- Draw the logic diagram of Circuit 1



: C = xy + xz + yz

這是一般的 Karnaugh maps 化簡。

- Derive the following Boolean functions using Karnaugh maps
- $S = z \oplus (x \oplus y)$, $C = z(x \oplus y) + xy$ (Circuit 2)
- Draw the logic diagram of Circuit 2
- Verify Circuit 1 = Circuit 2
  (using Verilog Structural level modeling)

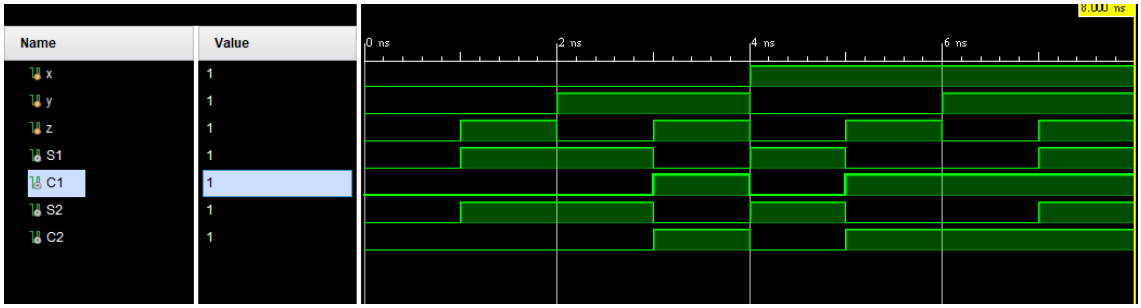


: $C = z(x \oplus y) + xy$

因為(x⊕y)在 S 就已經出現了，可以節省電晶體，但延遲會多一點。

程式如右:

```
1   `timescale 1ns / 1ps
2
3   module exercise_2(S1,C1,S2,C2,x,y,z);
4       output S1,C1,S2,C2;
5       input x,y,z;
6       wire n1,n2,n3,n4,n5,n6,n7;
7
8
9       xor(n1,x,y);
10      xor(S1,z,n1);
11
12      and(n2,x,y);
13      and(n3,x,z);
14      and(n4,z,y);
15      or(C1,n2,n3,n4);
16
17      buf(S2,S1);
18      and(n5,z,n1);
19      or(C2,n2,n5);
20  endmodule
21
```



由電壓圖 S1=S2 , C1=C2(上到下: 輸入:x,y,z 輸出:S1,C1;S2,C2)

三、Exercise　3:

- Design and verify the 8-bit ripple-carry adder composed of eight full-adders (using Verilog Structural level modeling)

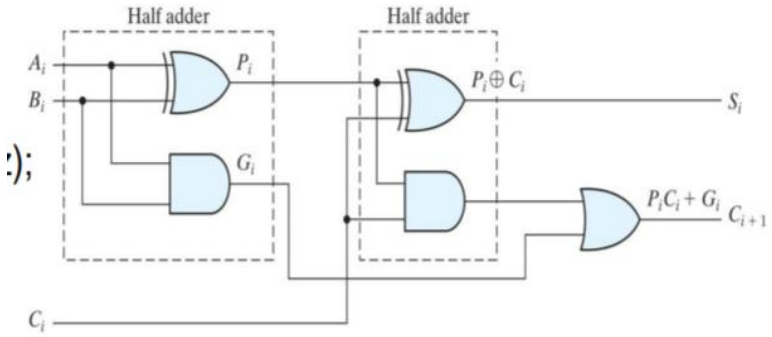
```
1   `timescale 1ns / 1ps
2
3   module half_adder (output S,C,input x,y);
4       xor(S,x,y);
5       and(C,x,y);
6   endmodule
7
8   module full_adder (output S,C,input x,y,z);
9       wire S1,C1,C2;
10
11      half_adder HA1(S1,C1,x,y);
12      half_adder HA2(S,C2,S1,z);
13      or(C,C2,C1);
14  endmodule
15
16
17  module exercise_3(output [7:0]S, output C8, input [7:0]A,B,input C0);
18      wire C1,C2,C3,C4,C5,C6,C7;
19
20      full_adder FA0(S[0],C1,A[0],B[0],C0),
21          FA1(S[1],C2,A[1],B[1],C1),
22          FA2(S[2],C3,A[2],B[2],C2),
23          FA3(S[3],C4,A[3],B[3],C3),
24          FA4(S[4],C5,A[4],B[4],C4),
25          FA5(S[5],C6,A[5],B[5],C5),
26          FA6(S[6],C7,A[6],B[6],C6),
27          FA7(S[7],C8,A[7],B[7],C7);
28  endmodule
29
```

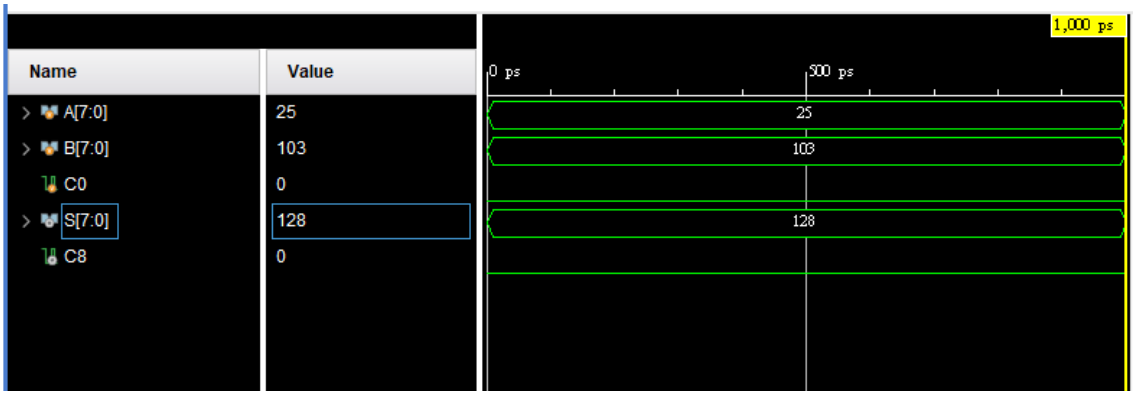
程式碼如右:

(1) half_adder :

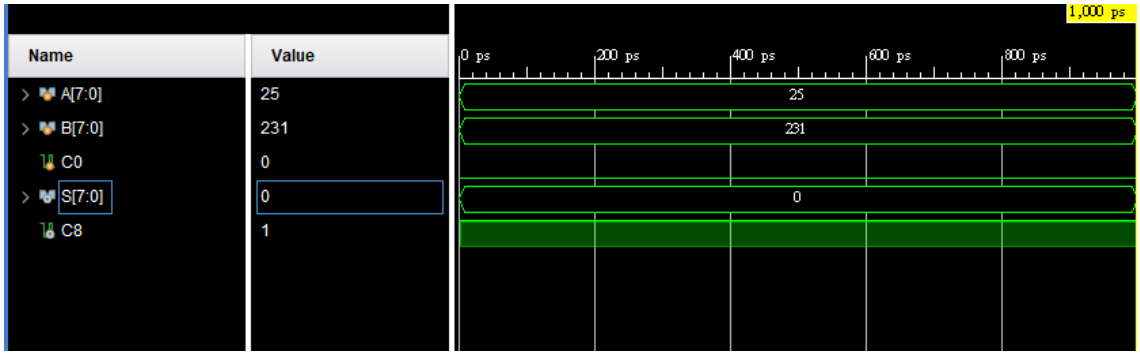
(2) full_adder :
含 2 個半加器與 1 個 OR 閘

(3) 將 8 個全加器接在一起就是 8_bit 加法器





由電壓圖[7:0]A+[7:0]B=[7:0]S



由電壓圖[7:0]A+[7:0]B=[7:0]S，S 無法顯示大於(含)2^8 ->也就是 S 只能<256

若 S > 256 ，則 C8 輸出 1；

實驗心得

1. Structural level modeling 中邏輯閘使用函數表示
2. Structural level modeling 可以很直觀的轉換成 Schematic
3. Structural level modeling 需要宣告邏輯閘之間的線路
4. 所有的 modeling 都需要注意該邏輯閘是否有交換律或結合律
5. Exercise 1 的 don't care conditions 很好用可以簡化電路
6. Exercise 2、3、4 電路的轉換用 Schematic 畫出來後比較簡單。

例如:exercise2:AND-OR gate 轉成 multi-level NAND gate、multi-level NOR gate…..。