實驗主題(Lab12)

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Exercise 1:

Exercise 1: D Latch

- Design and verify the D latch using Verilog HDL
  - Structural level (Gate-level) modeling

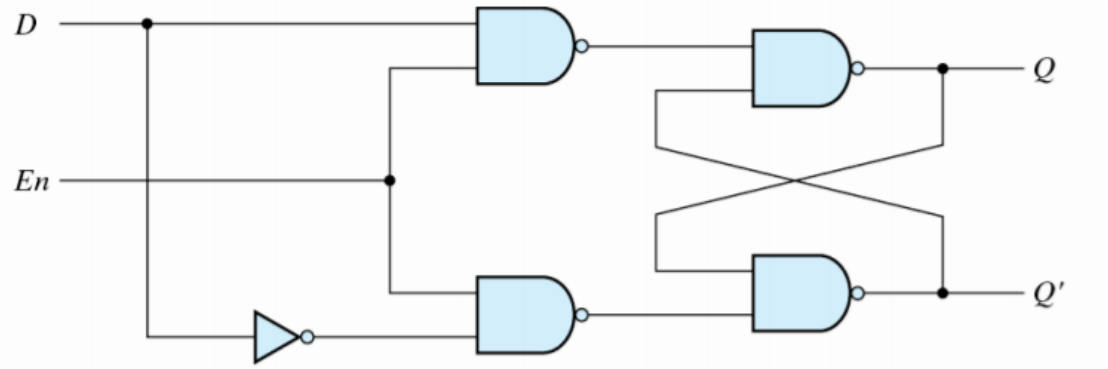


Fig. 5.6 *D* latch (a) Logic diagram

Exercise 2:

Exercise 2: Master-slave D Flip-Flop

- Design and verify the positive-edge-triggered master-slave D flip-flop using Verilog HDL
  - Structural level (Gate-level) modeling

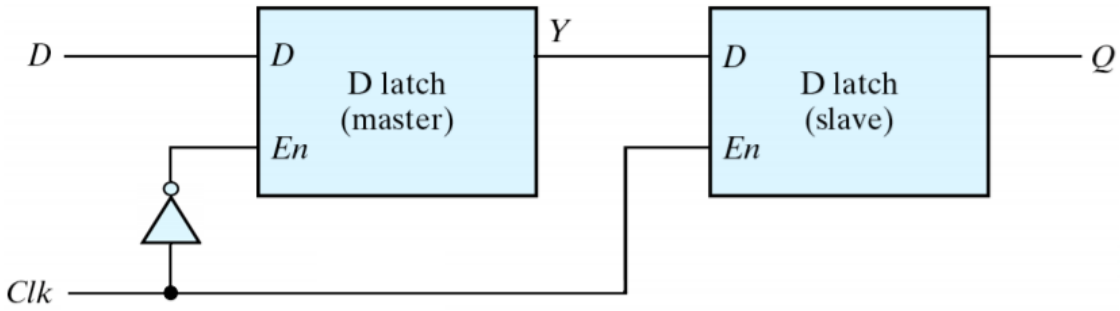
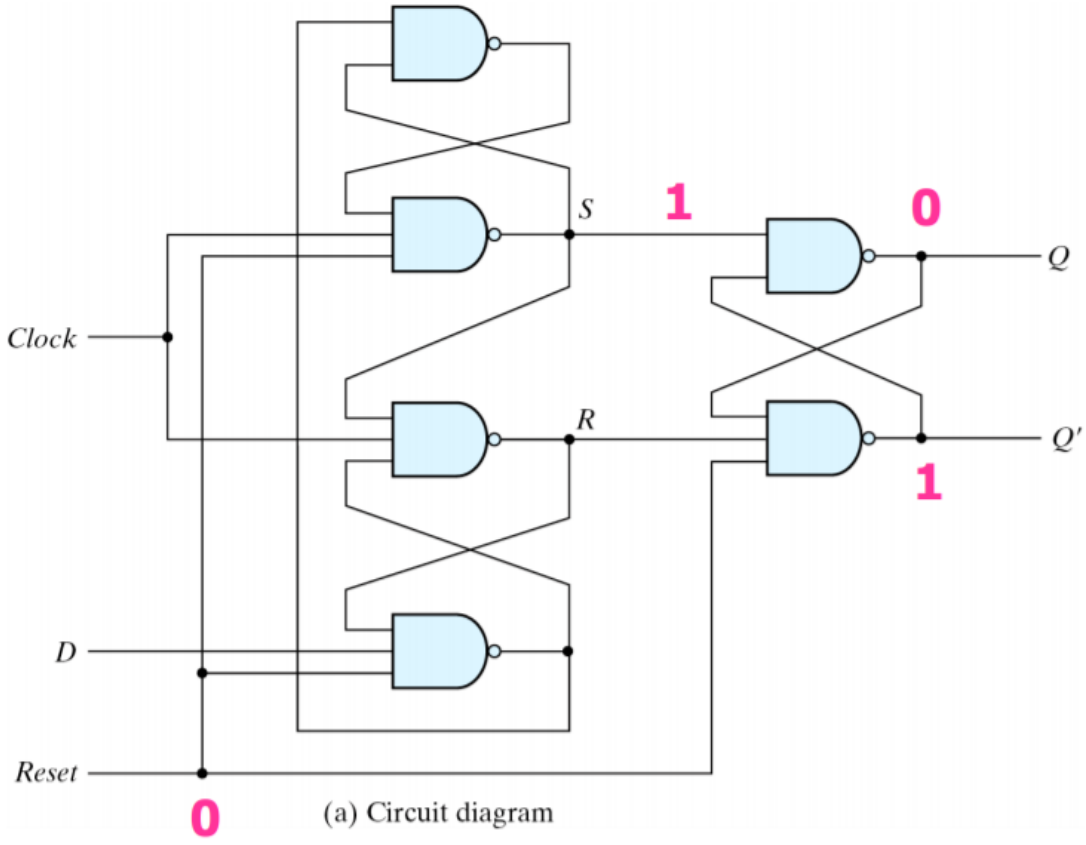


Fig. Positive-edge-triggered master-slave *D* flip-flop

Exercise 3:

Exercise 3: D flip-flop with asynchronous reset

- Design and verify the *D* flip-flop with asynchronous reset shown in Fig. 5.14 using Verilog HDL (Gate-level modeling)



(a) Circuit diagram

實驗內容

一、 Exercise 1:

Exercise 1: D Latch

- Design and verify the D latch using Verilog HDL
  - Structural level (Gate-level) modeling

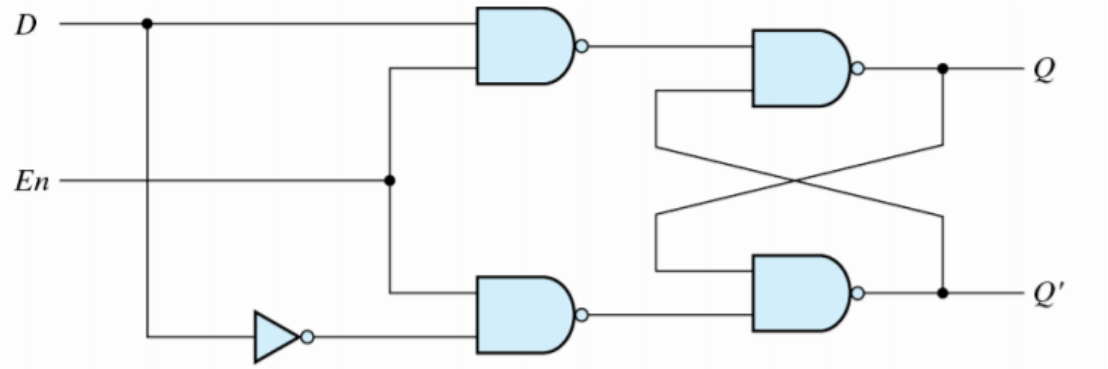
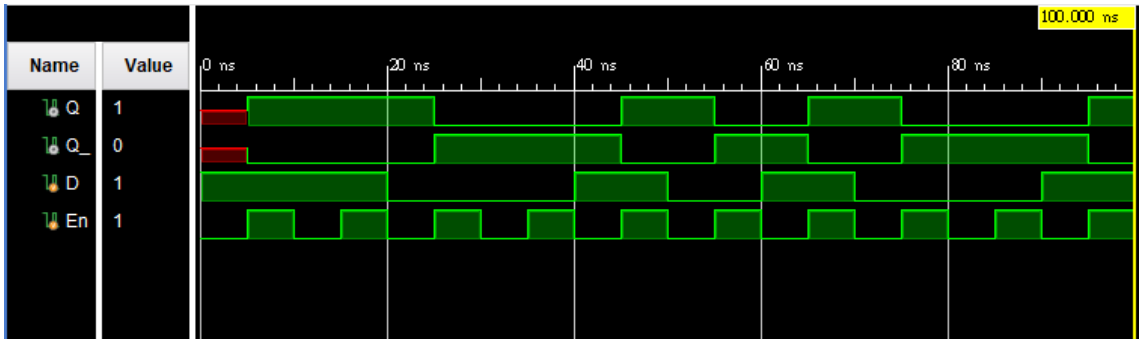


Fig. 5.6 *D* latch (a) Logic diagram

基本上就照著圖片邏輯閘擺放

En	*D*	Next state of *Q*
0	X	No change
1	0	*Q* = 0; reset state
1	1	*Q* = 1; set state

```
1   `timescale 1ns / 1ps
2
3
4   module D_latch (Q, Q_, D, En);
5       output Q, Q_;
6       input D, En;
7
8       wire D_,n1,n2,n3,n4;
9
10      not(D_,D);
11      nand(n1, En, D);
12      nand(n2, En, D_);
13      nand(n3, n1, n4);
14      nand(n4, n3, n2);
15
16      buf(Q, n3);
17      buf(Q_, n4);
18  endmodule
```



初始的 Q 和 Q’ 電壓未知是正常的，當 En=1 時，D 將會賦值給 Q

二、Exercise　2:

Exercise 2: Master-slave D Flip-Flop

- Design and verify the positive-edge-triggered master-slave D flip-flop using Verilog HDL
  - Structural level (Gate-level) modeling

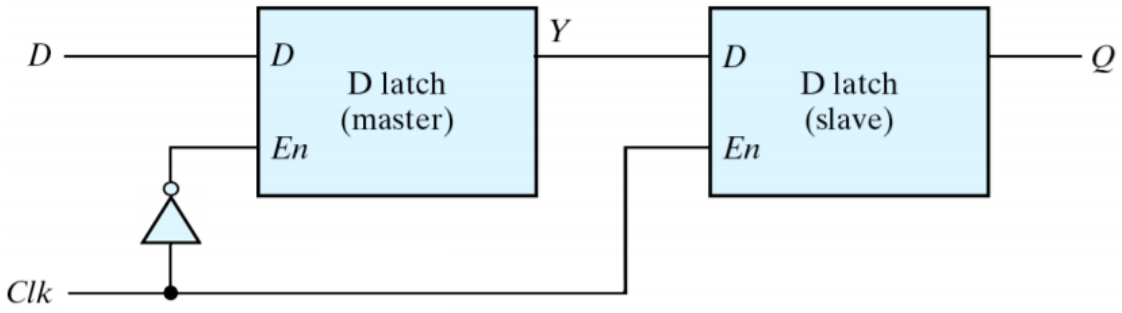


Fig. Positive-edge-triggered master-slave *D* flip-flop

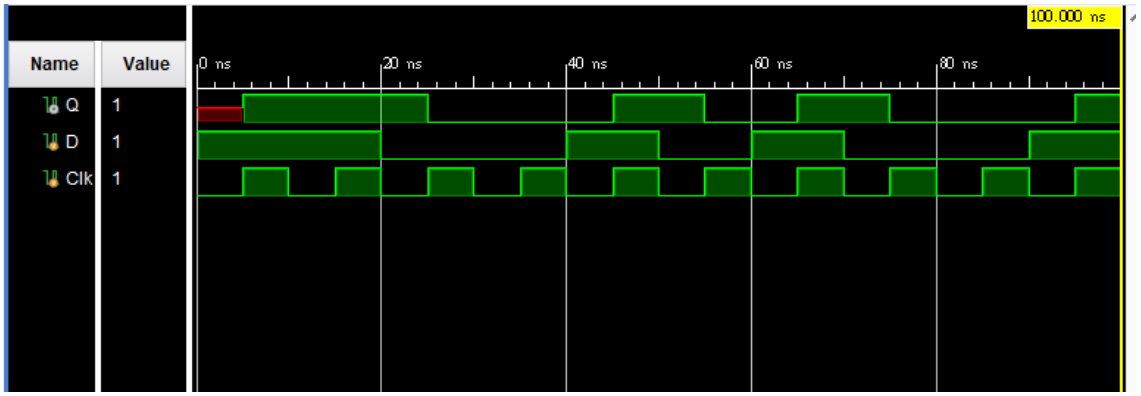
第一個 D latch 是在 Clk 為負時，D 賦值給 Y。

第二個 D latch 是在 Clk 為正時，Y 賦值給 Q。

總結來說，僅在 Clk 正緣時，D 賦值給 Q。

Clk	*D*	*Q*	*Q'*
↑	0	0	1
↑	1	1	0

```
3   module D_latch (Q, D, En);
4       output Q;
5       input D, En;
6
7       wire D_,n1,n2,n3,n4;
8
9       not(D_,D);
10      nand(n1, En, D);
11      nand(n2, En, D_);
12      nand(n3, n1, n4);
13      nand(n4, n3, n2);
14
15      buf(Q, n3);
16  endmodule
17
18  module  Master_slave_D_Flip_Flop (Q, D, Clk);
19      output Q;
20      input D, Clk;
21
22      wire Clk_,Y;
23
24      not(Clk_, Clk);
25      D_latch A1(Y, D, Clk_);
26      D_latch A2(Q, Y, Clk);
27
28  endmodule
```

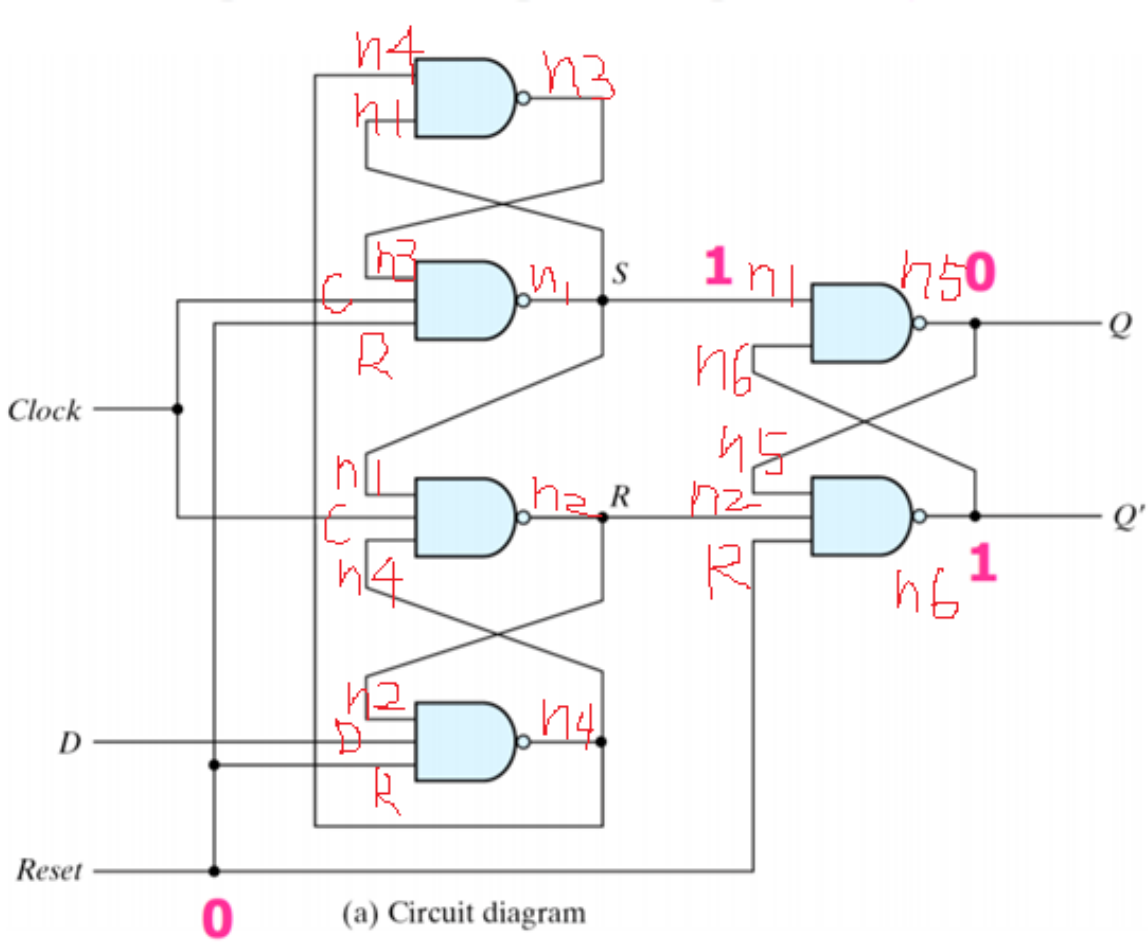


如圖所示，僅在 Clk 正緣時，D 賦值給 Q。

三、Exercise　3:

Exercise 3: D flip-flop with asynchronous reset

- Design and verify the *D* flip-flop with asynchronous reset shown in Fig. 5.14 using Verilog HDL (Gate-level modeling)

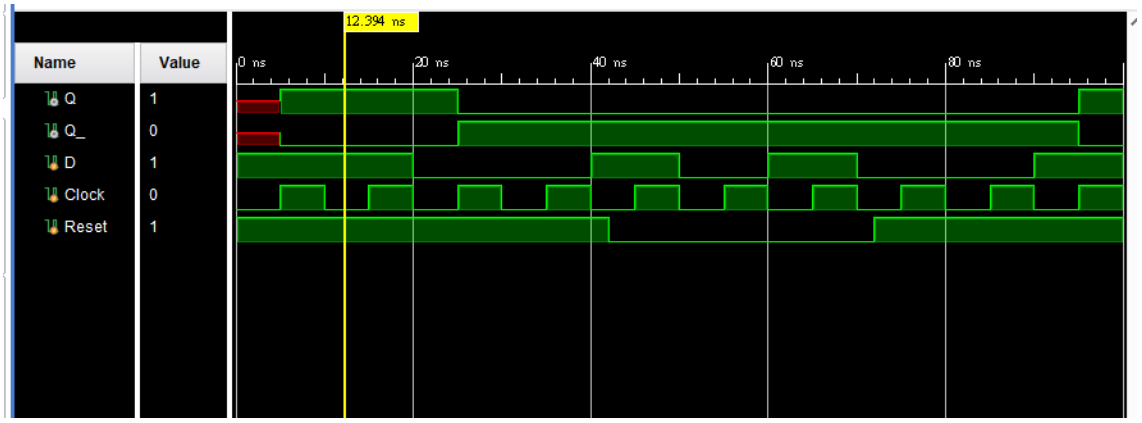


當 Reset=0，n6 必為 1，n5 必= not (n1)

當 Reset=0，n1 必為 1，n5 必= not (n1) = 0

當 Reset=1，僅在 Clk 正緣時，D 賦值給 Q

```
1   `timescale 1ns / 1ps
2
3   module D_flip_flop_with_as_r(Q, Q_, Clock, D, Reset);
4       output Q, Q_;
5       input Clock, D, Reset;
6       wire n1,n2,n3,n4,n5,n6;
7
8       nand(n1, n3, Clock, Reset);
9       nand(n2, n1, Clock, n4);
10      nand(n3, n1, n4);
11      nand(n4, n2, D, Reset);
12      nand(n5, n1, n6);
13      nand(n6, n2, n5 , Reset);
14
15      buf(Q, n5);
16      buf(Q_, n6);
17  endmodule
```



如圖所示，當 R=0 時，Q 必為 0，僅在當 R=0、Clk 正緣時，D 賦值給 Q。

```
`timescale 1ns / 1ps

module testbench();
wire Q, Q_;
reg D, Clock, Reset;
D_flip_flop_with_as_re M0 (.Q(Q), .Q_(Q_), .D(D), .Clock(Clock), .Reset(Reset));

    initial
        #100
    $finish;

    initial
        begin
        Clock = 0;
        forever #5
            Clock = ~Clock;
        end

    initial
    fork
        D = 1;
        Reset = 1;
        #20 D = 0;
        #40 D = 1;
        #50 D = 0;
        #60 D = 1;
        #70 D = 0;
        #90 D = 1;
        #42 Reset = 0;
        #72 Reset = 1;
    join
endmodule
```

Testbench 中，所有的 initial 均會同時開始

forever=每 X 單位時間，重複執行到分號

fork-join 中，使用的是絕對時間。

實驗心得

1. Structural level modeling 中邏輯閘使用函數表示
2. Structural level modeling 可以很直觀的轉換成 Schematic
3. Structural level modeling 需要宣告邏輯閘之間的線路
4. 所有的 modeling 都需要注意該邏輯閘是否有交換律或結合律