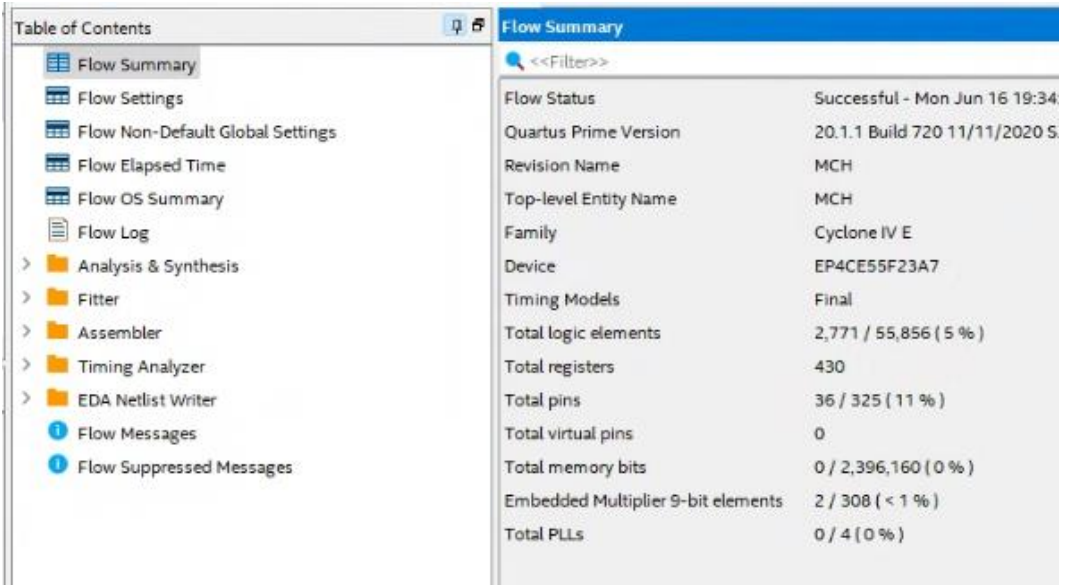


## 2025 Digital IC Design Homework 5

| NAME  | 黃啟桓                           |   |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
|---|-------------------------------|---|-------------|-------------|-------------------------------|-----------------------|-------------------------------|---------------|-----|-----------------------|-----|--------|--------------|--------|--------------|---------------|-------|----------------------|------------------------|-----------------|-----|------------|-------------------|--------------------|---|-------------------|-----------------------|------------------------------------|-------------------|------------|---------------|
| Student ID  | P76134927                     |   |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
| <b>Simulation Result</b>  |                               |   |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
| Functional simulation   | <b>Pass</b>                   | Pre-Layout simulation   | <b>Pass</b> |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
| <pre># ===== RESULT ===== # All 10 patterns passed! # Cycle: 2581 # ** Note: \$finish      : E:/GG/Code/DIC_HW/HW5/file/testfix #           Time: 51620 ns Iteration: 0 Instance: /testfixture # 1</pre>  |                               | <pre># ===== RESULT ===== # All 10 patterns passed! # Cycle: 2581 # ** Note: \$finish      : E:/GG/Code/DIC_HW/HW5/syn_HW5/simul #           Time: 49039 ns Iteration: 0 Instance: /testfixture # 1</pre> |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
| <b>Synthesis Result</b>   |                               |   |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
| Total logic elements  | 2771                          |   |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
| Total memory bits   | 0                             |   |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
| Total registers   | 430                           |   |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
| Embedded multiplier 9-bit elements  | 2                             |   |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
| Clock period (ns)   | 19.0                          |   |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
| Total Cycle used  | 2581                          |   |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
|  <p>The screenshot shows the Quartus Prime Flow Summary window. On the left is a 'Table of Contents' with items like Flow Summary, Flow Settings, Flow Non-Default Global Settings, Flow Elapsed Time, Flow OS Summary, Flow Log, Analysis &amp; Synthesis, Fitter, Assembler, Timing Analyzer, EDA Netlist Writer, Flow Messages, and Flow Suppressed Messages. The main area is titled 'Flow Summary' and contains a table of synthesis results:</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Flow Status</th> <th>Successful - Mon Jun 16 19:34</th> </tr> </thead> <tbody> <tr> <td>Quartus Prime Version</td> <td>20.1.1 Build 720 11/11/2020 S</td> </tr> <tr> <td>Revision Name</td> <td>MCH</td> </tr> <tr> <td>Top-level Entity Name</td> <td>MCH</td> </tr> <tr> <td>Family</td> <td>Cyclone IV E</td> </tr> <tr> <td>Device</td> <td>EP4CE55F23A7</td> </tr> <tr> <td>Timing Models</td> <td>Final</td> </tr> <tr> <td>Total logic elements</td> <td>2,771 / 55,856 ( 5 % )</td> </tr> <tr> <td>Total registers</td> <td>430</td> </tr> <tr> <td>Total pins</td> <td>36 / 325 ( 11 % )</td> </tr> <tr> <td>Total virtual pins</td> <td>0</td> </tr> <tr> <td>Total memory bits</td> <td>0 / 2,396,160 ( 0 % )</td> </tr> <tr> <td>Embedded Multiplier 9-bit elements</td> <td>2 / 308 ( &lt; 1 % )</td> </tr> <tr> <td>Total PLLs</td> <td>0 / 4 ( 0 % )</td> </tr> </tbody> </table> |                               |   |             | Flow Status | Successful - Mon Jun 16 19:34 | Quartus Prime Version | 20.1.1 Build 720 11/11/2020 S | Revision Name | MCH | Top-level Entity Name | MCH | Family | Cyclone IV E | Device | EP4CE55F23A7 | Timing Models | Final | Total logic elements | 2,771 / 55,856 ( 5 % ) | Total registers | 430 | Total pins | 36 / 325 ( 11 % ) | Total virtual pins | 0 | Total memory bits | 0 / 2,396,160 ( 0 % ) | Embedded Multiplier 9-bit elements | 2 / 308 ( < 1 % ) | Total PLLs | 0 / 4 ( 0 % ) |
| Flow Status   | Successful - Mon Jun 16 19:34 |   |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
| Quartus Prime Version   | 20.1.1 Build 720 11/11/2020 S |   |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
| Revision Name   | MCH                           |   |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
| Top-level Entity Name   | MCH                           |   |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
| Family  | Cyclone IV E                  |   |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
| Device  | EP4CE55F23A7                  |   |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
| Timing Models   | Final                         |   |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
| Total logic elements  | 2,771 / 55,856 ( 5 % )        |   |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
| Total registers   | 430                           |   |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
| Total pins  | 36 / 325 ( 11 % )             |   |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
| Total virtual pins  | 0                             |   |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
| Total memory bits   | 0 / 2,396,160 ( 0 % )         |   |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
| Embedded Multiplier 9-bit elements  | 2 / 308 ( < 1 % )             |   |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
| Total PLLs  | 0 / 4 ( 0 % )                 |   |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |
| <b>Description of your design</b>   |                               |   |             |             |                               |                       |                               |               |     |                       |     |        |              |        |              |               |       |                      |                        |                 |     |            |                   |                    |   |                   |                       |                                    |                   |            |               |

MCH 模組會接收 20 個 (X, Y) 點，每點一個 clock cycle。

當接收第二個(X, Y)就可以開始比大小，目標是找到最右下的點(P0)。P0 搬到 array[0]。

S\_SORT，演算法：Bubble Sort + 使用 cross product 判斷角度大小。若 cross product (orient) < 0，表示需交換。這樣的結果就是剩餘的 19 個座標依照斜率排序。

S\_SCAN，維護 hull array 作為凸包堆疊。每當新的點進來：若 top-1, top, 新點形成的是右轉或共線 (orient ≤ 0)，就把 top pop 掉 (top--)，否則 push 新點 (top++)

S\_AREA，計算 hull array 面積。

當然，這裡的 S\_SORT，S\_SCAN，S\_AREA 都有使用一個 cross，而且不會同時使用使用 cross，所以把他們功能合併，減少乘法器。