NCTU-CS Digital System Lab.

Online Test (11/07)

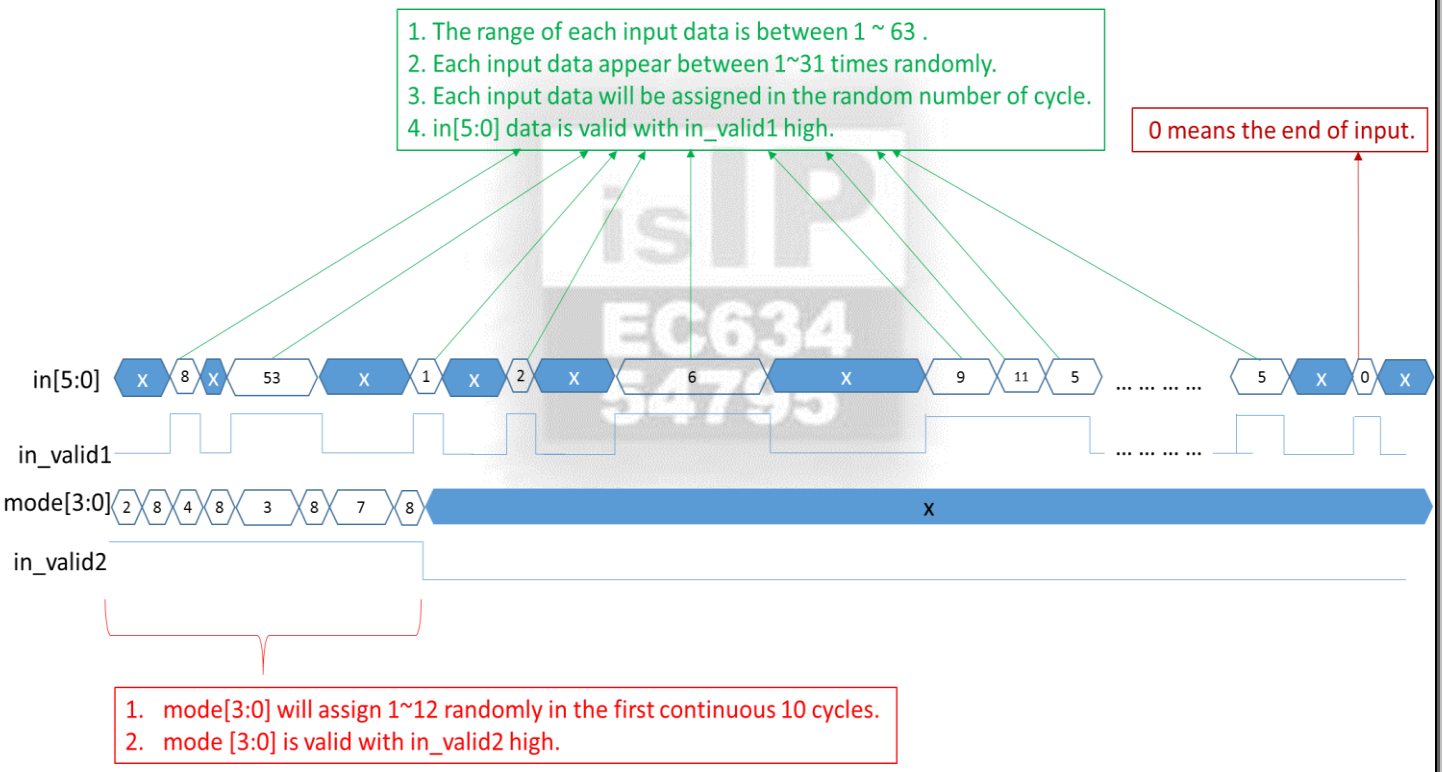
Data Preparation

1. Extract LAB data from TA's directory.
   % tar xvf ~2016dlabta02/Online_test2.tar

Design Description and Examples

Design this game:

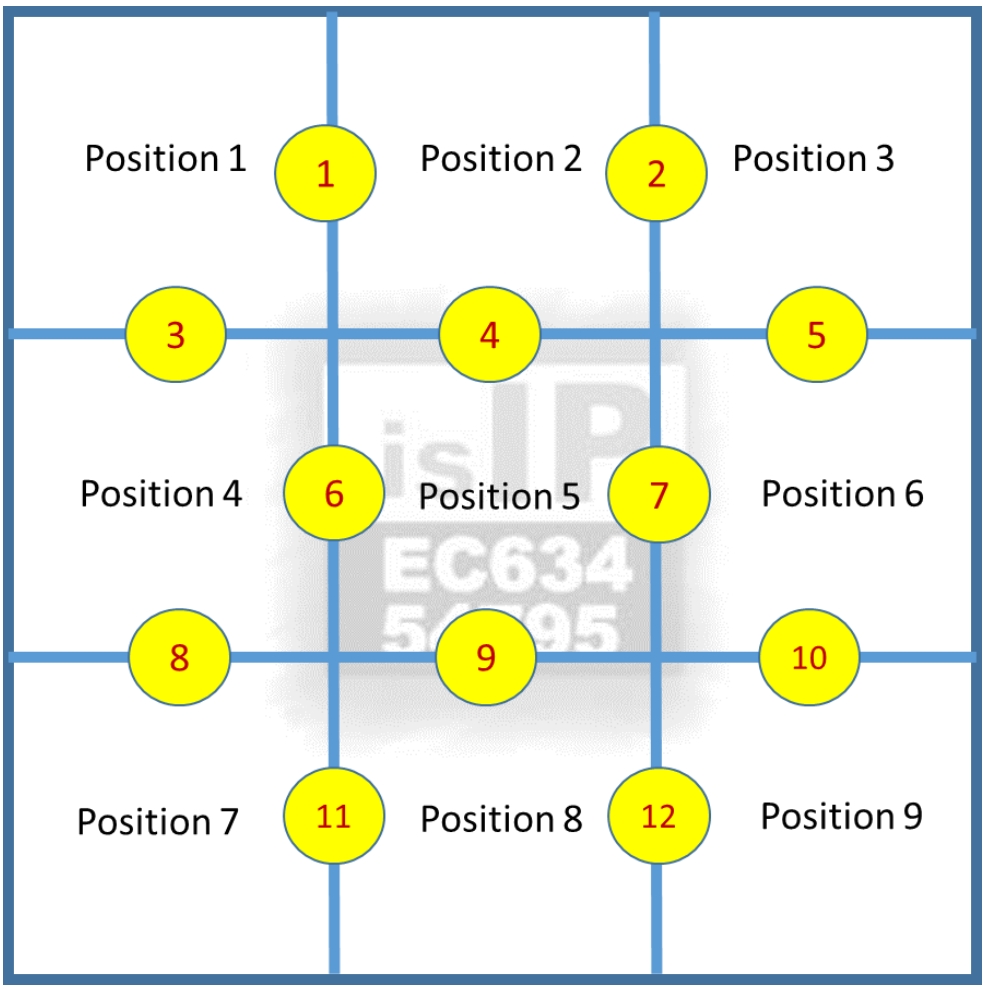
Input：



In **in[5:0]** channel you will receive a large number of inputs in random cycles between each input data. And the total number of them are unknown, but the number range of each input data is 1~63. Each of them may appear 1~31 times. When we assign 0, it means the end of **in[5:0]**. You need to store the different 9 numbers from **in[5:0]** channel and place 9 numbers to positions 1~9 sequentially. Another channel **mode[3:0]** assign the mode 1~12 randomly, and you must accomplish your design by following rule.

Game rule:

In the following graph, there are positions 1~9 and you place different 9 numbers sequentially. Yellow balls are the mode you get from pattern. According to the mode, change the position of each number sequentially. Finally, output the 9 numbers from position 1 to position 9 in continuous 9 cycles.

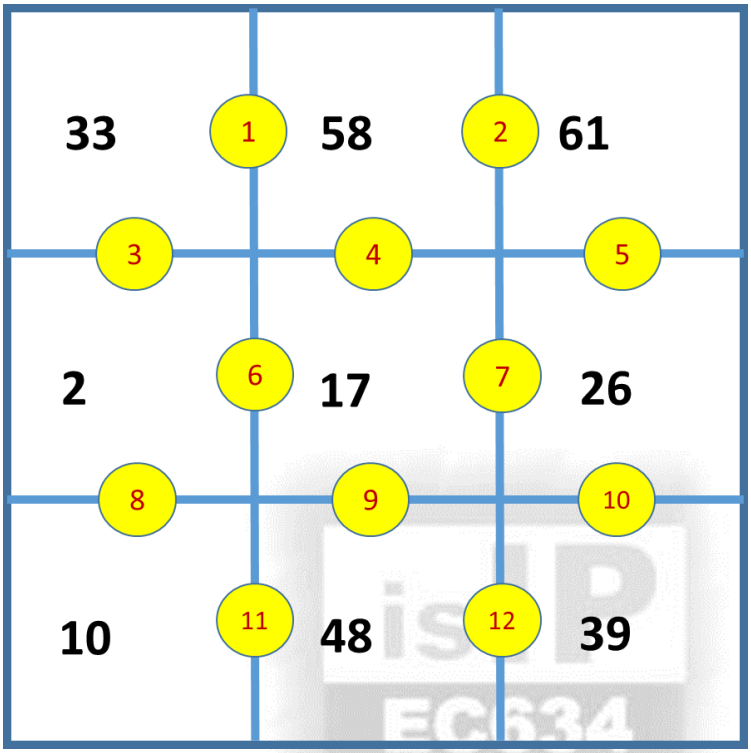


Ex:

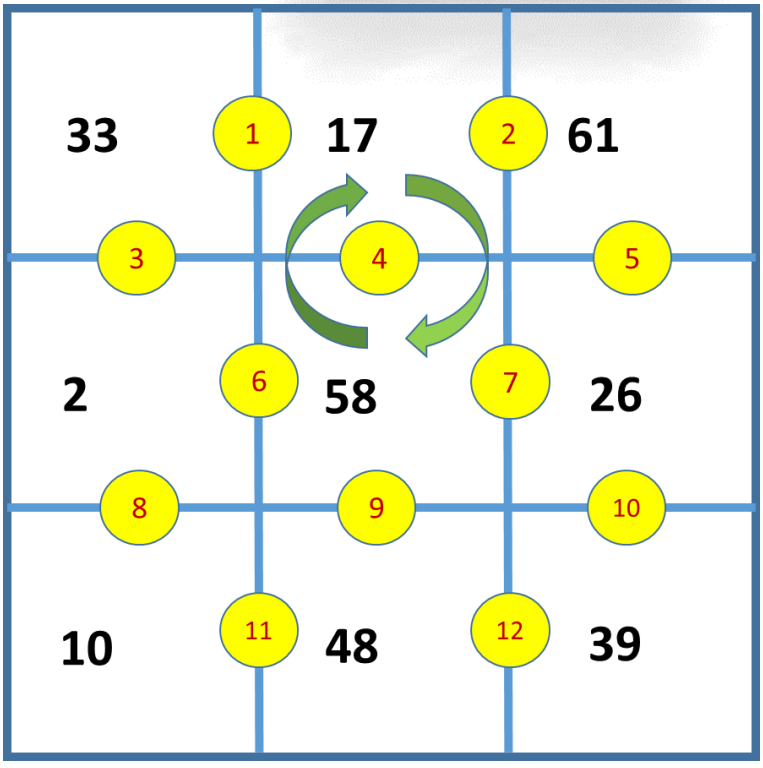
You get 9 different numbers from Pattern: 33, 58, 61, 2, 17, 26, 10, 48, 39

mode = 4, 7

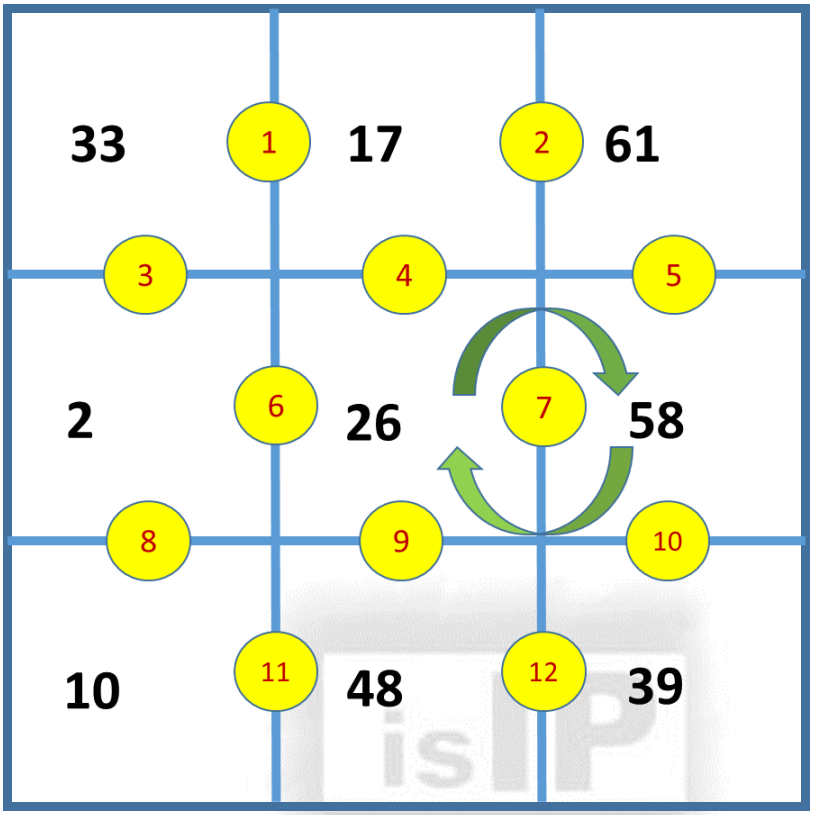
(There are only two mode in this example but Online_test will give you 10 mode!)



Mode = 4



Mode = 7



Output：

33 17 61 2 26 58 10 48 39

You should output 33 17 61 2 26 58 10 48 39 in 9 continuous cycle.

Your goal is to compute these operations by above rules and output the correct answer.

Inputs

1. Input data for **in[5:0]** will be assign in **random** cycles while **in_ valid1** is high.
2. **Mode[3:0]** will be assign in continuous 10 cycles while **in_ valid2** is high.
3. All inputs will be changed at clock ***negative*** edge.
4. All signals are unsigned integer.

Input Signals	Bit Width	Description
clk	1	clock
rst_n	1	asynchronous active-low reset
in	6	the range of data is 1~63
in_valid1	1	high when **in[5:0]** is valid
in_valid2	1	high when **mode[3:0]** is valid
mode	4	Change position of 9 number by rule discuss above. Range: 1~12mode

Outputs

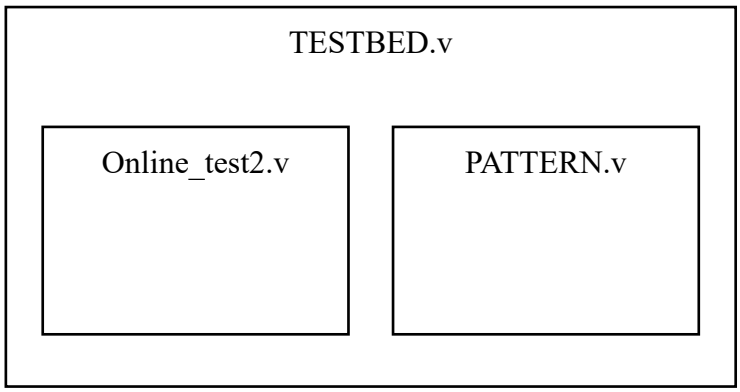
1. Your answer should be output at **out[5:0]** in **9 continuous cycle** .
2. **out_valid** should be low and **out** should be set to zero after initial reset.
3. **out_valid** should be set to high when output value is valid.
4. The latency of your design in each pattern should not be larger than 100 cycles.
5. All outputs are synchronized at clock ***positive*** edge.
6. Test pattern will check whether your answer is correct or not at clock **negative edge** when **out_valid** is high.

Output Signals	Bit Width	Description
out	6	output result
out_valid	1	high when **out** is valid

Specifications

1. Top module name : **Online_test2** (File name : **Online_test2.v**)
2. Input pins: **clk, rst_n, in_valid1, in_valid2, in[5:0], mode[3:0]**.
3. Output pins: **out_valid, out[5:0]**.
4. **out_valid** should not be raised when **in_valid** is high (when **in** data is transferring).
5. It is **active-low asynchronous** reset.
6. The latency of your design in each pattern should not be larger than 100 cycles.
7. Grading policy:
   - Design: 70%
   - Area: 10%
   - Time: 10%
   - Question: 10%

Block Diagram



Note

1. Simulation step:
   - Put your design in 01_RTL
   - Simulation to check design : ./01_run
   - Show wave to debug: nWave &
   - Go to folder 02_SYN/ and check synthesis：./01_run_dc
   - Go to folder 03_GATE/ and check s：./01_run.f
   - Clear up : ./09_clean_up
2. Please add your student ID and name to the file name of .v file before upload file on e3 platform:
   Online_test2_0556123_陳小明.v
3. Sample waveform: