NCTU-CS Digital System Lab.

Online Test (11/28)

Data Preparation

1. Extract LAB data from TA's directory.
   % tar xvf ~2016dlabta02/OT11_28.tar

Design Description and Examples

Design the 3X3 signed complex Matrix multiplication, A*B = C, and find real part and image part the fourth, fifth, sixth greatest number from the members of C:

A B C

$$\begin{bmatrix} 3+i & 0+3\text{i} & -2+2i \\ 1+\text{i} & 7 & 0 \\ 2 & 7+2\text{i} & 1+4i \end{bmatrix} * \begin{bmatrix} 4+3i & -7+2\text{i} & 1+i \\ 2-3\text{i} & 2 & 3-5\text{i} \\ 0+i & 1-\text{i} & 0 \end{bmatrix} = \begin{bmatrix} ? & ? & ? \\ ? & ? & ? \\ ? & ? & ? \end{bmatrix}$$

Input：

You will get 18 input numbers from in_real[5:0] and in_image[5:0] respectively, and place inputs into A , B sequentially by the following rule:

$$A=\begin{bmatrix} pos1 & pos2 & pos3 \\ pos4 & pos5 & pos6 \\ pos7 & pos8 & pos9 \end{bmatrix}$$

$$B=\begin{bmatrix} pos10 & pos11 & pos12 \\ pos13 & pos14 & pos15 \\ pos16 & pos17 & pos18 \end{bmatrix}$$

Output：

Ex:

After compute the matrix multiplication, answer is : $\begin{bmatrix} 24+3i & -27+20\text{i} & 31+i \\ 21-3\text{i} & 2 & 30-5\text{i} \\ 0+i & 1-3\text{i} & 0 \end{bmatrix}$ output

real part and image part the fourth, fifth, sixth greatest number, respectively.

out_real[13:0]: 21, 2, 1

out_image[13:0]: 1, 1, 0

You should output answer in continuous 3 cycles with out_valid high.

Your goal is to compute these operations by above rules and output the correct answer.

Inputs

1. input data for **in_real[5:0] and in_image[5:0]** is valid with **in_ valid** is high.
2. **in_real[5:0] and in_image[5:0] are singed.**
3. All inputs will be changed at clock ***negative*** edge.

Input Signals	Bit Width	Description
clk	1	clock
rst_n	1	asynchronous active-low reset
in_real	6	6 bit signed real inputs
in_image	6	6 bit signed image inputs
in_valid	1	high when **in_real[5:0], in_image[5:0]** is valid

Outputs

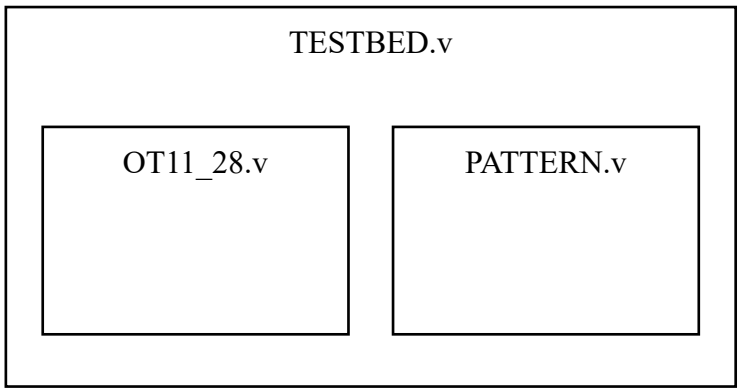
1. Your answer should output at **out_real[13:0] and out_image[13:0]** in continuous 3 cycles with ou_valid high.
2. **out_real[13:0]** & **out_image[13:0] are singed**
3. **out_valid** should be low and **out_real[13:0] and out_image[13:0]** should be set to zero after initial reset.
4. **out_valid** should be set to high when output value is valid.
5. The latency of your design in each pattern should not be larger than 100 cycles.
6. All outputs are synchronized at clock ***positive*** edge.
7. Test pattern will check whether your answer is correct or not at clock **negative edge** when **out_valid** is high.

Output Signals	Bit Width	Description
out_real	14	output result
out_image	14	output result
out_valid	1	high when **out_real[13:0] and out_image[13:0]** are valid.

Specifications

1. Top module name : **OT11_28** (File name : **OT11_28.v**)
2. Input pins: **clk , rst_n , in_valid , in_real[5:0], in_image[5:0]**.
3. Output pins: **out_valid , out_real[13:0], out_image[13:0]**.
4. **out_valid** should not be raised when **in_valid** is high.
5. It is **active-low asynchronous** reset.
6. Clock period: 3.5ns
7. The latency of your design in each pattern should not be larger than 100 cycles.
8. Grading policy:
   Design: 70%
   Area: 10%
   Time: 10%
   Question: 10%

Block Diagram



Note

1. Simulation step:
   - Put your design in 01_RTL
   - Simulation to check design : ./01_run
   - Show wave to debug: nWave &
   - Go to folder 02_SYN/ and check synthesis：./01_run_dc
   - Go to folder 03_GATE/ and check s：./01_run.f
   - Clear up : ./09_clean_up
2. Please add your student ID and name to the file name of .v file before upload file on e3 platform:
   OT11_28_0556123_陳小明.v
3. Sample waveform: