```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity usr1tb is
end usr1tb;

architecture Behavioral of usr1tb is

    signal clk,clk_div : STD_LOGIC := '0';
    signal rst : STD_LOGIC := '0';
    signal load : STD_LOGIC := '0';
    signal mode : STD_LOGIC_VECTOR(1 downto 0) := "00";
    signal si : STD_LOGIC := '0';
    signal pi : STD_LOGIC_VECTOR(3 downto 0) := (others => '0');
    signal so : STD_LOGIC;
    signal po : STD_LOGIC_VECTOR(3 downto 0);

    component usr1

        Port (
            clk : in  STD_LOGIC;
            clk_div : inout std_logic;
            rst : in  STD_LOGIC;
            load: in  STD_LOGIC;
            mode : in  STD_LOGIC_VECTOR(1 downto 0);
            si : in  STD_LOGIC;
            pi : in  STD_LOGIC_VECTOR(3 downto 0);
            so : out  STD_LOGIC;
            po : out  STD_LOGIC_VECTOR(3 downto 0)
        );
    end component;
begin
    uut : usr1
        Port Map (
            clk => clk,
            clk_div => clk_div,
            rst => rst,
            load => load,
            mode => mode,
            si => si,
            pi => pi,
            so => so,
            po => po
        );

    clk_process : process
    begin
        clk <= '0';
        wait for 10 ns;
        clk <= '1';
        wait for 10 ns;
    end process;
```

```
    stim_proc : process
    begin
        -- Reset the UUT
        rst <= '1';
        wait for 20 ns;
        rst <= '0';

        -- Test SISO mode
        mode <= "00";
        si <= '1';
        wait for 200 ns;
        si <= '0';
        wait for 200 ns;


        -- Test SIPO mode
        mode <= "01";
        si <= '1';
        wait for 100 ns;
        si <= '0';
        wait for 200 ns;

        -- Test PISO mode
        mode <= "10";
        load<='0';
        pi <= "1110";
        wait for 100 ns;
        load<='1';
        wait for 300 ns;

        -- Test PIPO mode
        mode <= "11";
        pi <= "1010";
        wait for 50 ns;
        pi <= "1100";
        wait for 50 ns;

        wait;
    end process;
end Behavioral;
```