Layer Minimization in Escape Routing for Staggered-Pin-Array PCBs *

Yuan-Kai Ho[1], Xin-Wei Shih[1], Yao-Wen Chang[1,2], and Chung-Kuan Cheng[3]
[1]Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan
[2]Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan
[3]Department of Computer Science and Engineering, University of California, San Diego, La Jolla, CA, USA
yuankai@eda.ee.ntu.edu.tw; raistlin@eda.ee.ntu.edu.tw; ywchang@cc.ee.ntu.edu.tw; ckcheng@ucsd.edu

Abstract

As the technology advances, the pin number of a high-end PCB design keeps increasing. The staggered pin array is used to accommodate a larger pin number than the grid pin array of the same area. Nevertheless, escaping a large pin number to the boundary of a dense staggered pin array, namely multilayer escape routing for staggered pin arrays, is significantly harder than that for grid pin arrays. This paper addresses this multilayer escape routing problem to minimize the number of used layers in a staggered pin array for manufacturing cost reduction. We first present an escaped pin selection method to assign a maximal number of escaped pins in the current layer and also to increase useful routing regions for subsequent layers. Missing pins are also modeled in our routing network to utilize the routing resource effectively. Experimental results show that our approach can significantly reduce the required layer number for escape routing.

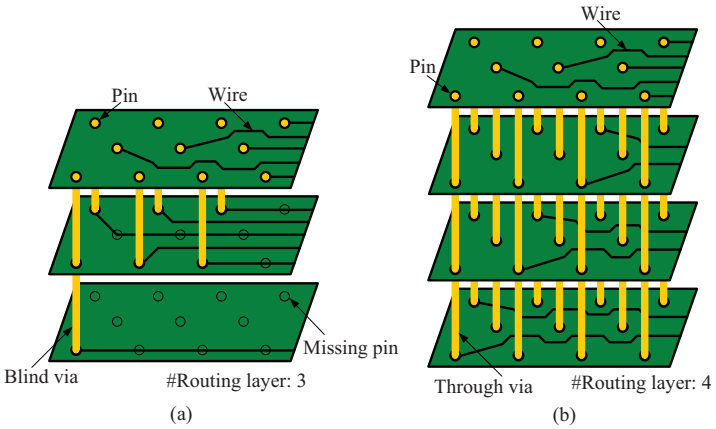

Figure 1: An illustration of multilayer escape routing. (a) Multilayer escape routing considering missing pins. (b) Multilayer escape routing without considering missing pins. Only three layers are needed in (a) while four layers are required in (b).

1 Introduction

As the technology advances, the pin number of a high-end PCB design keeps increasing. To accommodate the fast growing number of pins in modern PCB designs, the staggered pin array is introduced to provide high pin density solution [1, 2]. The staggered pin array is formed by shifting specific columns of the traditional square grid pin array and further packing pins. Compared with the grid pin array, the staggered one can accommodate more pins under the same pitch constraint and same area usage [3].

Escape routing, which is to route nets from pins in a pin array to the array boundary, is a key problem in PCB routing. Many recent works have addressed the PCB routing for grid pin arrays [4]. However, escape routing in a staggered pin array is more difficult than that in a grid pin array. Some special constraints need to be considered to satisfy design rules because the non-square structure and higher pin density incur more stringent constraints [5].

To escape more pins to the boundary of a dense staggered pin array, multilayer escape routing is desirable. To reduce the manufacturing cost, it is of particular importance to minimize the number of used layers for multilayer escape routing. The *blind-via technology* is introduced for modern PCB designs to increase routable regions; this technology is to connect only required layers, rather than pass through the entire PCB. With this technology, the routed pins in the current layer can be removed/ignored in routing subsequent layers. Figure 1(a) shows multilayer escape routing. The *escaped pins* in the first layer become the *missing pins* in the subsequent layers, and their located space can thus be utilized to route more wires. In other words, the escape routing for the selected escaped pins in the current layer would significantly affect the escape routing in the subsequent layers, thus also the maximum pin number that can be escaped.

The network-flow formulation is a popular method to solve the single-layer escape routing problem [5, 6, 7, 8, 9, 10, 11]. Ho et al. [5] considered the single-layer escape routing in staggered pin arrays. For the single-layer escape routing in grid pin arrays, Fang et al. [8] applied Delaunay triangulation and Voronoi diagrams to construct a routing network, and Yan and Wong [10] presented a precise network-flow model to characterize the routing capacity of a grid tile. However, these network-flow based escape routing algorithms cannot directly extend to multiple layers by building a flow network for each layer and then interconnecting them together. The reason is that the locations of the missing pins in another layer cannot be predicted during routing one layer. As a result, a multi-layer network-flow model cannot model the routing resources provided by the missing pins well, and thus some important solution space may be lost. Therefore, we should consider the escaped pins layer by layer so that the missing pins can be identified, and their resulting routing spaces can be further utilized [13]. As illustrated in Figures 1(a) and (b), only three layers are needed for routing the given wires by considering the missing pins for multilayer escape routing. In contrast, if we concurrently solve the routing for all layers based on the aforementioned multilayer network-flow model, four layers are needed to complete the routing. Therefore, it desirable to develop an effective routing algorithm for the multilayer escape routing problem.

Most of multilayer escape routing works focused on grid pin ar-

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rays. Horiuchi et al. [12] proposed a routing strategy with parallel triangular indents pattern to create regions of specific shapes that allow more wires to pass through them. Wang et al. [13] presented a central triangular pattern to distribute pins to different layers. However, since these patterns are specifically designed for grid pin arrays, they might not be suitable for staggered pin arrays. Shi and Cheng [3] proposed some properties for staggered pin arrays, but they did not actually perform routing, due to the high complexity of routing in a staggered pin array. The multilayer escape routing problem in a staggered pin arrays is intrinsically more difficult than that in a grid pin array, due to the higher pin density and more restricted routing resources in a staggered pin array.

In this paper, we propose an effective multilayer escape routing algorithm for staggered pin arrays to minimize the number of layers required for routing. We first present an escaped pin selection method to select a maximal set of escaped pins in the current layer and also try to reserve the largest routing region for subsequent layers. A maximal set of escaped pins, which are evenly distributed in the staggered pin array, are selected. Since these pins disperse in the whole staggered pin array and thus avoid forming congested regions, these escaped nets can minimize the blockage for other pins. We continue to select remaining evenly distributed pins and missing pins for subsequent layers until all layers are processed. In this way, we can reduce congested regions and route more escaped pins in each layer without violating design rules. In particular, we also model the missing pins into our routing network; in other words, the extra routing space produced by the missing pins can be fully utilized in our routing network to increase the number of routed escaped pins. We summarize our contributions as follows.

- We explore the properties of staggered pin arrays and propose conditions to determine whether a set of selected pins can be successfully escaped.
- Our proposed method can escape a maximal number of selected pins to the array boundary in the current layer and increase useful routing regions for subsequent layers to route more remaining pins to the array boundary.
- We consider missing pins in our routing network to identify the available routing regions produced by the pins to fully utilize the given routing resource.
- Compared with the column-by-column horizontal escape routing strategy for staggered pin arrays proposed in [3], our algorithm can significantly reduce the layer number by 48%.

The rest of this paper is organized as follows. Section 2 explores the properties of staggered pin arrays and then provides our observations and problem formulation. Section 3 proposes our multilayer escape routing algorithm for staggered pin arrays. Section 4 reports our experimental results, and Section 5 gives the conclusion.

2 Preliminaries

In this section, we first introduce the structure of a staggered pin array in Section 2.1. Then, we present some observations of multilayer escape routing for staggered pin arrays in Section 2.2. The problem is then formulated in Section 2.3.

2.1 Staggered Pin Array

The staggered pin array is introduced to accommodate the increasing number of pins in a fixed area. An $m \times n$ staggered pin array has m rows with n pins in each odd row and $n-1$ pins in each even row. The angle between a line joining any adjacent two pins is always a multiple of 60-degree [3]. Compared with a grid pin array, a staggered pin array can accommodate more pins of the same pitch and same area. Figure 2 shows an example. With the same area and same pitch, Figure 2(a) gives an 8×8 grid pin array with 64 pins, while Figure 2(b) gives a 9×8 staggered pin array with 68 pins.

Due to the non-square structure of a staggered pin array, traditional routing methods for grid pin arrays cannot directly apply to staggered ones. For example, to maximize the number of wires passing through the space between two adjacent pins, the passing routing wires should be orthogonal to a line joining two adjacent pins. Traditional horizontal and vertical wiring style cannot achieve the maximum number of passing wires in this space. Different from the square tile models in a grid pin array for routing network construction, a triangular tile model considering adjacent tiles together is required for a staggered one [5].

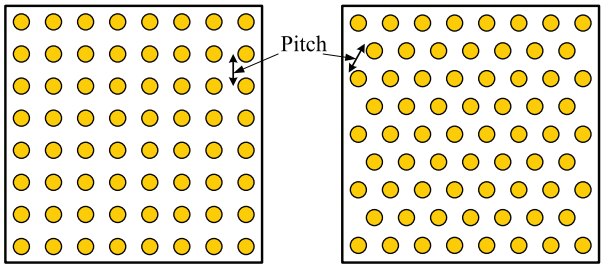

Figure 2: Two kinds of pin arrays: (a) the grid pin array and (b) the staggered pin array. Under the same area and same pith, the grid pin array in (a) only accommodates 64 pins, while the staggered pin array in (b) can accommodate 68 pins.

2.2 Observations

In multilayer escape routing, the *escaped pin order* of a staggered pin array affects the total number of routing layers. The escaped pin order is a layer-by-layer order of pins that are decided to escape. We observe that improper order might degrade the routability and thus would increase the resulting number of routing layers. We observed three drawbacks of an improper escaped pin order as follows:

- The smallest enclosing region of unrouted pins, called the *outline*, shrinks quickly if we assign improper escaped pins in a layer. Since the outline limits the number of pins to be escaped, quick shrinking would degrade the routability.
- An improper escaped pin order would make the routing resource produced by missing pins to be utilized less effectively.
- An improper escaped pin order would make the unrouted pins be clustered locally into groups. These groups might incur congested routing regions which might reduce routability.

Figure 3 illustrates the above situations. The peripheral pins are assigned to escaped pins in the first layer. As a result, in the second layer, the outline of unrouted pins is shrunk accordingly. The locations of the missing pins are all outside the outline; the routing space incurred by the missing pins cannot be fully utilized since the number of to-be-escaped pins is limited by the outline. Moreover, the remaining pins in the second layer are also clustered. The strict spacing constraint in the congested region affects the number of escaped pins in the subsequent layers.

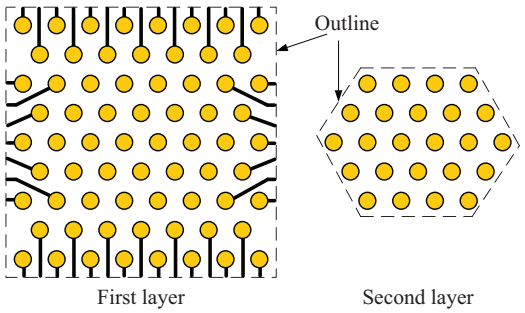

Figure 3: The improper escaped pin order shrinks the outline of remained pins. The number of escaped pins in the second layer is limited by the outline.

2.3 Problem Formulation

The problem of layer minimization in escape routing for staggered pin arrays can be defined as follows:

- Given an $m \times n$ staggered pin array and design rules, including wire width, wire spacing, the pin diameter, and the pitch, the objective is to escape all pins in the staggered pin array to the array boundary so that no constraint is violated, and the required layer number is minimized.

3 Our Proposed Algorithm

In this section, we present our multilayer escape routing algorithm for staggered pin arrays. Figure 4 shows the overall flow of the algorithm. For each layer, we perform *escaped pin selection* followed by *routing on a staggered pin array*.

In the stage of escaped pin selection, we first determine the maximum number of escaped pins that can escape to the array boundary. Then, we make the pins which help the routability as the escaped pins. The escaped pins consist of two types: *critical pins* and *evenly distributed pins*. The critical pins are selected based on the staggered-array structure, while the evenly distributed pins are selected based on the pin distribution.

In the stage of routing on a staggered pin array, we first construct a routing network based on our proposed missing pin model to utilize the increased routing region generated by missing pins. Then, we solve the routing network to get a global routing result. Finally, detailed routing is performed according to the global routing result.

After the escape routing on a single layer is completed, we check whether all pins in a staggered pin array are routed to the array boundary. If there is any unrouted pin, we add a new layer to route the unrouted pins. Note that the pins which have been routed in the previous layers become missing pins for the new layer. The process continues until all pins are routed, and we have the final routing result.

The detailed algorithms are presented in the following sections.

3.1 Escaped Pin Selection

3.1.1 Escaped Pin Number Determination

Before we present how to decide the escaped pin number for each layer, we introduce the *ring structure* for a staggered pin array. A staggered pin array is composed of a set of rings, $R = \{r_1, r_2, ..., r_{|R|}\}$, as shown in Figure 5. The innermost ring is denoted by r_1, and the rings are indexed increasingly outwards.

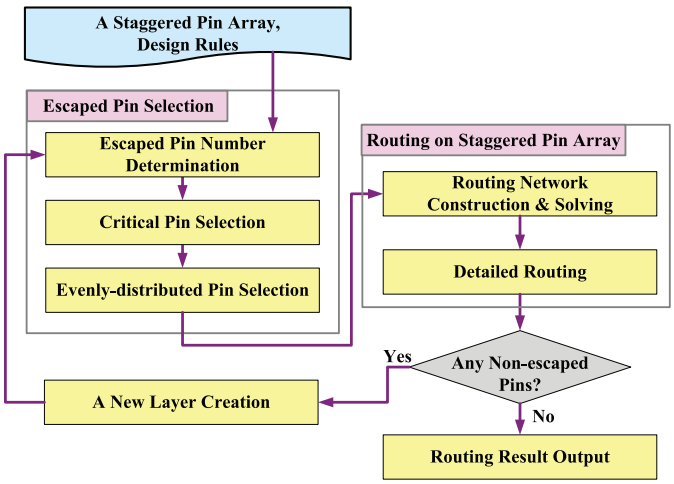

Figure 4: The flowchart of our proposed approach.

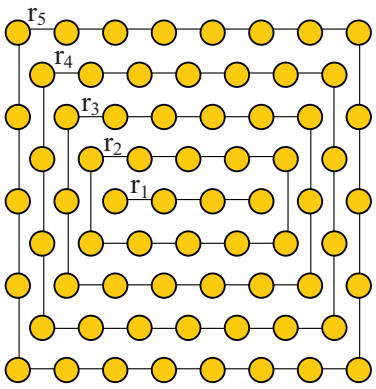

Figure 5: An illustration of the ring structure of the staggered pin array.

Now we consider the ring structure of a staggered pin array to derive the escaped pin number. In general, the escaped pin number can be derived according to the capacity and the unrouted pin number of the outermost ring. However, for the routing layers except the first routing layer, the capacity of inner rings should also be considered for more accurate estimation since the distribution of missing pins may affect the routability.

We derive the escaped pin number based on the maximum numbers of passing wires for rings. Equation (1) gives a recursive formulation of w_i, the variable that denotes the maximum number of passing wires within ring i.

$$w_i = \begin{cases} w_{i-1} + p_{i-1}, & \text{if } w_{i-1} + p_{i-1} < c_i \\ c_i, & \text{otherwise,} \end{cases} \quad (1)$$

where p_i is the known number of unrouted pins on the ring r_i, and c_i is the known capacity of the ring r_i. Note that w_1 is 0. In Equation (1), the maximum numbers of passing wires within r_i could be the maximum passing-wire number w_{i-1} plus the unrouted pin number p_{i-1} of the ring r_{i-1}, or constrained by the capacity c_i of the ring r_i. As the routing escapes the pins to the array boundary, escaped pin number is $w_{|R|} + p_{|R|}$. According to the recursion, the escaped pin number could be bounded by the capacity of inner rings.

Figure 6 illustrates that the escaped pin number is bounded by the capacity of inner rings. Assume that the pitch can accommodate only

one wire. We can see that, for the outermost ring r_9, the total capacity is 60 and the pin number is 44. If there are no missing pins on the outermost ring r_9, the ideal escaped pin number is $60 + 44 = 104$. However, the maximum number of wires that can pass through the inner ring r_4 is 30, and the number of unrouted pins between the rings r_9 and r_4 is 14. As a result, the escaped pin number is $30 + 14 + 44 = 88$, which is constrained by the inner ring r_4. It is worth mentioning that the situation is caused by improper escaped pin selection in the previous routing layers. If the selected pins are evenly distributed in the pin array for escaping, we can avoid the escaped pin number to decrease quickly.

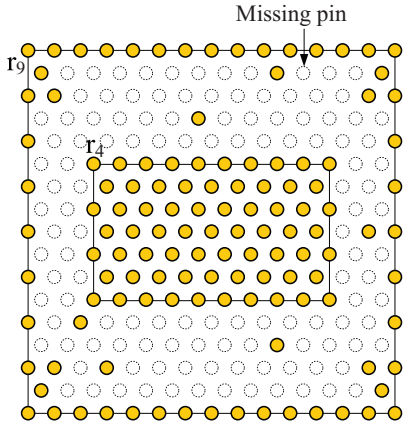

Figure 6: The escaped pin number is constrained by the inner ring. The capacity of the ring r_9 cannot be fully utilized since most pins are constrained by the ring r_4

3.1.2 Critical Pin Selection

To achieve the determined escaped pin number, we first select critical pins as the escaped pins. The critical pins are for better routing space utilization and routability improvement in a staggered pin array. There are two types of critical pins: *boundary pins* and *diagonal pins*.

The *boundary pins* are denoted as the pins that are nearest to the boundaries. Since no other pins can utilize the escape routing space of the boundary pins, the boundary pins should be always selected as the critical pins.

The *diagonal pins* in the first routing layer are defined as the corner pins of each ring. In each subsequent layer, the diagonal pins are horizontally shifted one pitch from the diagonal pins of the previous layer toward the array center. We select the diagonal pins as the critical pins based on the two following observations. (1) The routing space near the corners of a staggered pin array is harder to be utilized by other non-diagonal pins. (2) Once the diagonal pins are escaped, the indented shapes, formed by the corresponding missing pins, allow more pins to escape to the left and right boundaries. Figure 7 gives an example for the two types of pins.

3.1.3 Evenly-distributed Pin Selection

We further select evenly distributed pins as escaped pins after critical pins are selected. The evenly distributed pins are the pins which are evenly distributed in a staggered pin array. Escaping evenly distributed pins can provide two benefits. (1) As these pins are evenly located in a pin array, the routes of the pins would not compete with each others. It is not difficult to escape all these pins. (2) After these pins are escaped, the unrouted pins and the corresponding missing pins are also evenly distributed in the following layer. In other words, in the following layer,

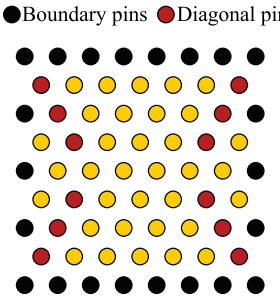

Figure 7: The two kinds of critical pins: boundary pins and diagonal pins.

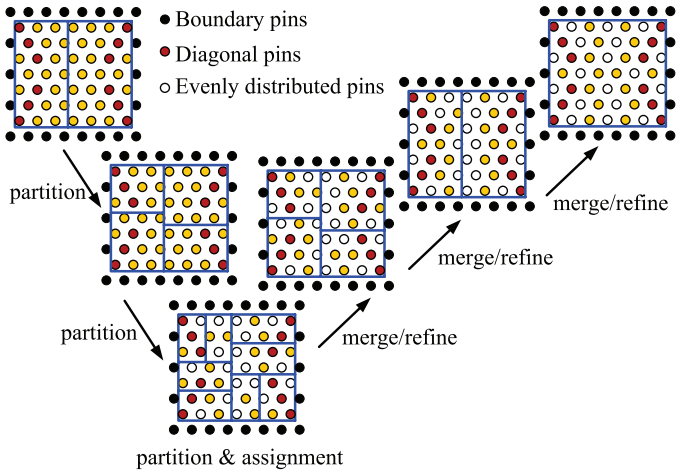

Figure 8: The multilevel framework for selecting the evenly distributed pins.

the congestion in local regions also can be reduced, and we can get larger escaped pin number without any violation.

A multilevel partition-based framework is proposed to select evenly distributed pins as shown in Figure 8. We iteratively partition a staggered pin array without boundary pins into a set of sub-regions. In each sub-region, we identify a small number of evenly distributed pins, say not larger than three; the identified pins are evenly distributed by trying all combinations of pins in the corresponding sub-region. Then, we iteratively merge two adjacent sub-regions into one larger region. During merging, we refine the evenly distributed pin assignment in a larger region. For each identified pin in the larger region, we pick one identified pin at a time and consider swapping the location of the identified pin with the locations of non-identified pins to get a more evenly distributed result. The merging is performed until the region size is equal to the size of the staggered pin array with no boundary pins.

To verify that our selected escaped pins can successfully escape to the array boundary, we derive an inequality to characterize the routability. The selected escaped pins should satisfy the following inequality:

$$w_{|R|} - w_i \leq \sum_{j=i}^{|R|-1} (s_j), \qquad \text{for } i = 1, 2, ..., |R| - 1, \qquad (2)$$

where s_j is the number of selected escaped pins on the ring r_j. This inequality provides a necessary condition for routability. Considering a certain ring r_i, if the selected pin number outside the ring r_i is less than the difference between the passing wire numbers of the outmost

ring $r_{|R|}$ and that of the ring r_i, it implies that too many selected pins are inside the ring r_i and thus cannot go through r_i.

Although the necessary condition cannot guarantee 100% routability of selected pins, it is still a good criterion to guide the selection. During the multilevel selection, once Inequality (2) is not satisfied, we cancel some selected escaped pins inside the ring r_i and select new escaped pins outside the ring r_i. Using Figure 6 as an example, w_9 is 44 and w_4 is 30. Therefore, according to Inequality (2), the number of selected escaped pins outside the ring r_4 should be at least 14. Otherwise, some selected pins inside the ring r_4 cannot be escaped.

3.2 Routing on Staggered Pin Array

3.2.1 Routing Network Construction and Solving

As aforementioned in the flow of our algorithm, we perform routing for selected escaped pins. According to the suggestion from the work [5], the pins of a staggered pin array and corresponding locations are formulated into a routing network, and the routing problem can be solved by LP/ILP formulation. In addition, different from the single-layer escape routing, we also model missing pins into our routing network for multilayer escape routing.

The routing network uses the *triangular tile model* to formulate the staggered structure [5]. In the model, three adjacent pins form a tile which encloses a triangular region. Figure 9(a) gives an example of a triangular tile. A triangular tile model comprises three *pin nodes* and three *internal nodes*. A pin node represents a pin, while an internal node represents a tile side. To formulate the relations between nodes, there is a directed edge from each pin node to its opposite internal node, and there are undirected edges between each two internal nodes. Furthermore, to model the routing information, each edge has a capacity. The capacity represents the feasible number of wires that can go through the corresponding edge. There are three capacity settings: (1) The capacity of the edge between a pin node and an internal node is always one since the pin can only be routed by one wire. (2) The capacity of the edge between two internal nodes within one tile is the maximum number of wires allowed in the triangular tile. (3) The capacity of the edge between two internal nodes from two adjacent tiles is the maximum number of passing wires on the tile side based on design rules. Figure 9(b) shows the whole routing network.

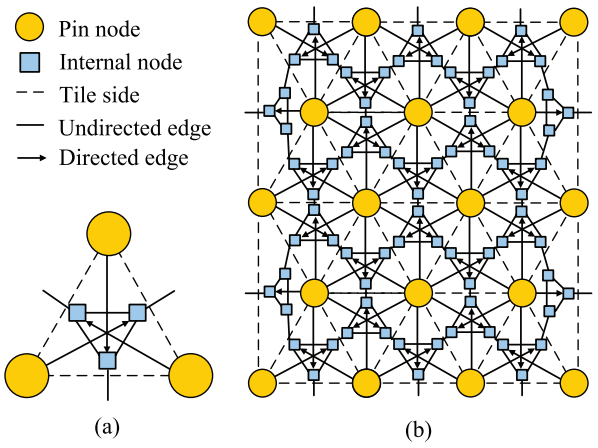

Figure 9: (a) A triangular tile model. (b) The routing network for the staggered pin array.

However, missing pins are not modeled in the mentioned routing network. As an example shown in Figure 10(a), the routing space of the missing pin is not formulated. The formulated maximum number of wires, which can pass through the side between node A and node C, is two. In fact, the maximum number of the wires can be three if the routing space of the missing pin is considered. Therefore, we must develop a new missing pin model to utilize the extra routing space. For example, as shown in Figure 10(b), the routing space produced by the missing pin B is well-considered.

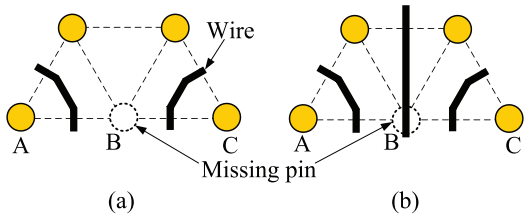

Figure 10: (a) Routing without considering the missing pin B. (b) Routing with considering the missing pin B.

A missing pin model is introduced in our routing network. As a pin has been routed in the previous layers, we remove all edges connected to the corresponding pin node. A *missing pin node* is then created to replace the pin node. New undirected edges are added between the missing pin node and internal nodes surrounding the missing pin node. The capacity of each new edge is set to infinite. In particular, the missing pin node has a capacity constraint, which is the maximum number of wires that can pass through the region of the missing pin. Note that, in our routing network, only the missing pin nodes have capacity constraints, while other nodes have no constraints. Figure 11 shows our missing pin model.

After the routing network is modeled as LP/ILP formulation [5], we can then use CPLEX library [14] to solve it.

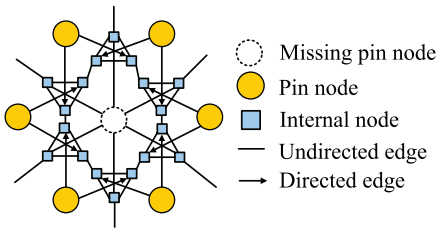

Figure 11: A missing pin model in our routing network. The capacity of the missing pin node is the maximum number of wires that can pass through the region produced by the missing pin.

3.2.2 Detailed routing

After solving our routing network, the number of wires in each tile is determined. Based on the wire-number information, we then preform detailed routing to realize the physical wiring. The routing style described in [5] is adopted to complete the detailed routing.

4 Experimental Results

We implemented our multilayer escape routing algorithm in the C++ programming language and performed experiments on a 2.6GHZ AMD Opteron Linux workstation with 6GB memory. The CPLEX [14] library was used to solve the LP/ILP formulation for our routing network. Ten testcases with the staggered style were generated to evaluate

our approach. Different from the single-layer escape routing problem that routes only some specific pins to the array boundary, the multilayer escape routing problem routes all pins to the array boundary.

We compared with previous works. Although the method in [13] is also for multilayer escape routing problem, their proposed routing pattern is for grid pin arrays, and thus cannot be applied to staggered pin arrays directly. The work [3] provided three escape routing strategies for staggered pin arrays as follows: (1) the column-by-column horizontal escape routing strategy, (2) the two-sided horizontal/vertical escape routing strategy, and (3) the multi-direction hybrid channel escape routing strategy. However, these strategies did not perform real routing, due to the high complexity of routing in a staggered pin array. Further, the two-sided horizontal/vertical escape routing strategy is mainly for manual designs because it does not have unified routing rules. Although the multi-direction hybrid channel escape routing strategy can be performed automatically in the second layer and the subsequent layers, routing in the first layer is still performed manually because the first-layer routing needs to carefully route specific pins with various capacities and high complexity of staggered pin arrays to produce hybrid channels. As a result, only the column-by-column horizontal escape routing strategy can be performed automatically. Therefore, we compared our approach with the column-by-column horizontal strategy proposed in [3].

Table 1 shows our experimental results. Column "Size" gives the size of the staggered pin array in $m \times n$ format, which is defined in Section 2.1. Column "Capacity" lists the maximum number of wires that can pass through the given pitch. The number of routing layers derived from the column-by-column horizontal strategy and from our proposed algorithm are listed in Columns "Column-by-Column" and "Ours", respectively. Column "Difference" gives the difference of the layer number between the two methods.

Table 1: Experimental Results

Circuits	Size	Capacity	Number of Layers		
			Column-by-Column [3]	Ours	Difference
case1	15x15	1	4	3	1
case2	21x17	1	6	4	2
case3	31x29	1	8	6	2
case4	15x15	2	3	2	1
case5	21x17	2	4	2	2
case6	23x23	2	4	3	1
case7	31x29	2	6	4	2
case8	35x35	2	6	4	2
case9	47x47	2	8	6	2
case10	65x65	3	9	6	3
			1.48	1.00	

Compared with the column-by-column horizontal strategy, our proposed algorithm can reduce the number of routing layers for all testcases. This is because our proposed algorithm can avoid improper escaped pin orders as discussed in Section 2.2. Specifically, the column-by-column horizontal strategy requires 48% more layers than our method. Note that each additional layer incurs significant manufacturing cost [15], so the 48% reductions in layers lead to very substantial cost reductions. The routing result of case8 is shown in Figure 12.

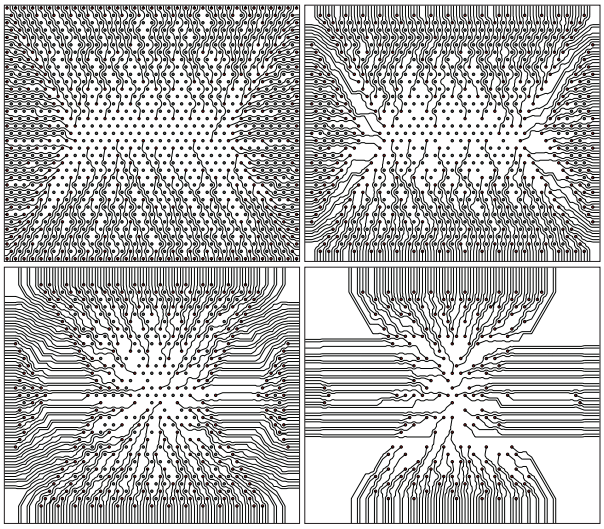

Figure 12: The layout of case8.

5 Conclusions

In this paper, the multilayer escape routing algorithm for staggered pin arrays has been proposed. To avoid an improper escaped pin order that might significantly degrade the routability for subsequent routing layers, our algorithm has selected critical escaped pins and evenly distributed pins to escape a maximal number of pins to the array boundary in the current layer and thus has increased useful routing region for subsequent routing layers. We have also developed a scheme to verify whether the selected pins can be successfully escaped. Further, missing pins have been also modeled in our routing network so that our routing network can effectively use the extra routing resource produced by the missing pins. Experimental results have shown that our proposed algorithm can significantly reduce the number of required layers for escape routing, compared to the column-by-column horizontal strategy.

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