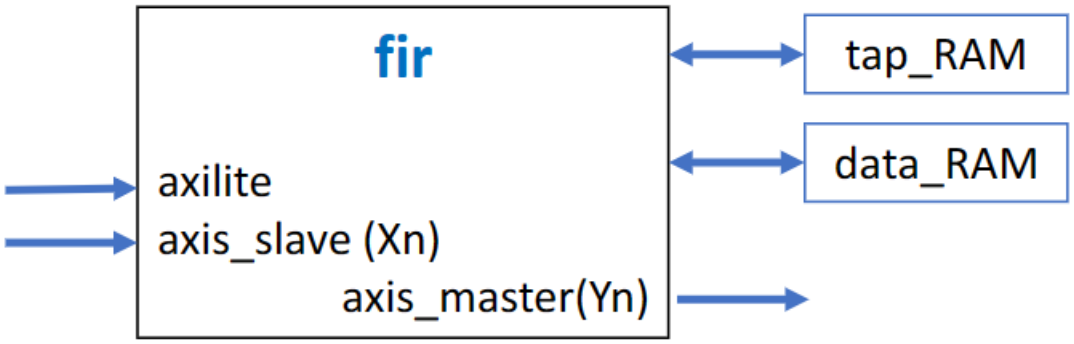
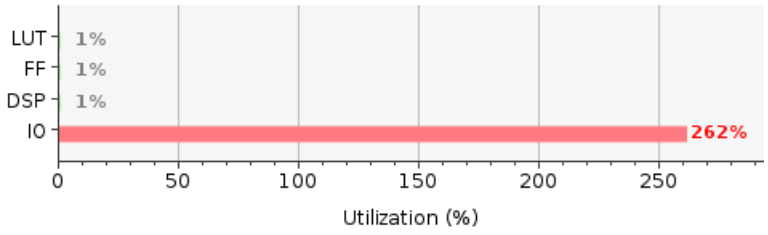
- Block Diagram



- Resource usage

Name	Slice LUTs (53200)	Slice Registers (106400)	DSPs (220)	Bonded IOB (125)	BUFGCTRL (32)
N fir	201	118	3	328	1

Resource	Utilization	Available	Utilization %
LUT	201	53200	0.38
FF	118	106400	0.11
DSP	3	220	1.36
IO	328	125	262.40



- Timing Report

Name	Waveform	Period (ns)	Frequency (MHz)
axis_clk	{0.000 1.945}	3.890	257.069

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.001 ns	Worst Hold Slack (WHS):	0.137 ns	Worst Pulse Width Slack (WPWS):	1.445 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	152	Total Number of Endpoints:	152	Total Number of Endpoints:	116

All user specified timing constraints are met.

Summary	
Name	Path 1
Slack	0.001ns
Source	genblk1.MAC_reg[1]/C (rising edge-triggered cell FDCE clocked by axis_clk {rise@0.000ns fall@1.945ns period=3.890ns})
Destination	genblk1.MAC_reg[31]/D (rising edge-triggered cell FDCE clocked by axis_clk {rise@0.000ns fall@1.945ns period=3.890ns})
Path Group	axis_clk
Path Type	Setup (Max at Slow Process Corner)
Requirement	3.890ns (axis_clk rise@3.890ns - axis_clk rise@0.000ns)
Data Path Delay	3.753ns (logic 2.638ns (70.290%) route 1.115ns (29.710%))
Logic Levels	10 (CARRY4=8 LUT2=2)
Clock Path Skew	-0.145ns
Clock Un...rtainty	0.035ns

- **Simulation Waveform**