



Computer-Aided VLSI System Design (EEE5022)

台大電機系/電子所

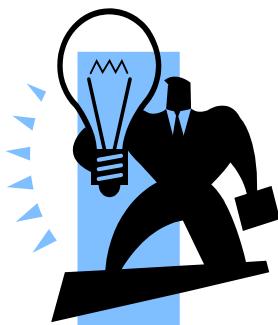
楊家驥教授

2024.9.3

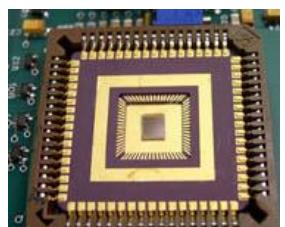
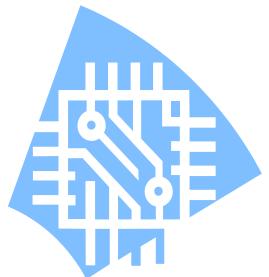


IC Design and Implementation

Idea



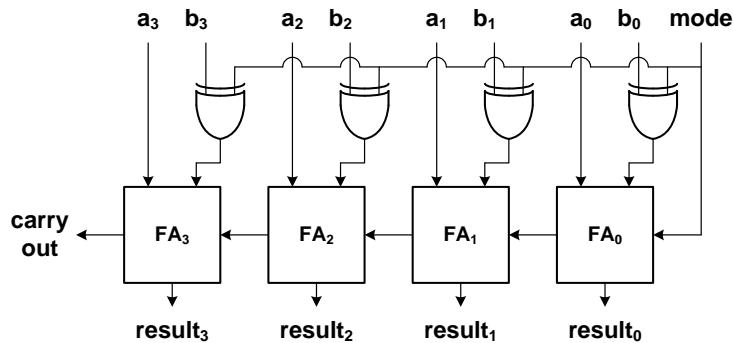
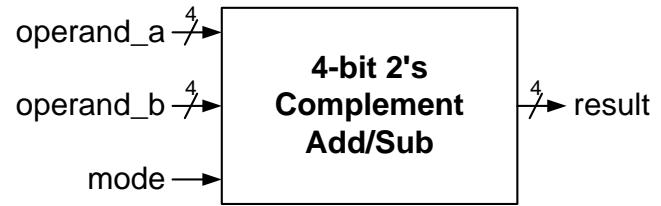
Design





Digital IC Design Flow

1. Concept/Application
2. Function/Spec. definition
3. Algorithm exploration
4. Architecture design
 - ❖ Divide-and-conquer
 - ❖ Sub-module design
 - ❖ Design verification
5. System prototyping
 - ❖ RTL design
 - ❖ Verilog Coding
 - ❖ Cell-based IC design flow



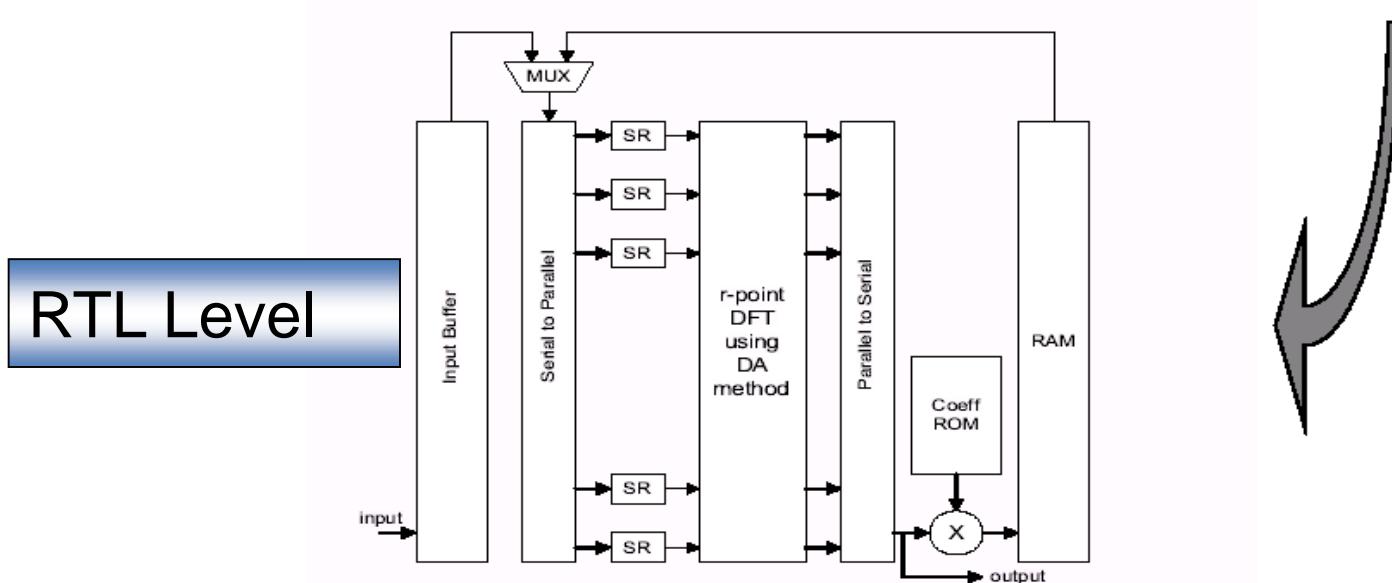
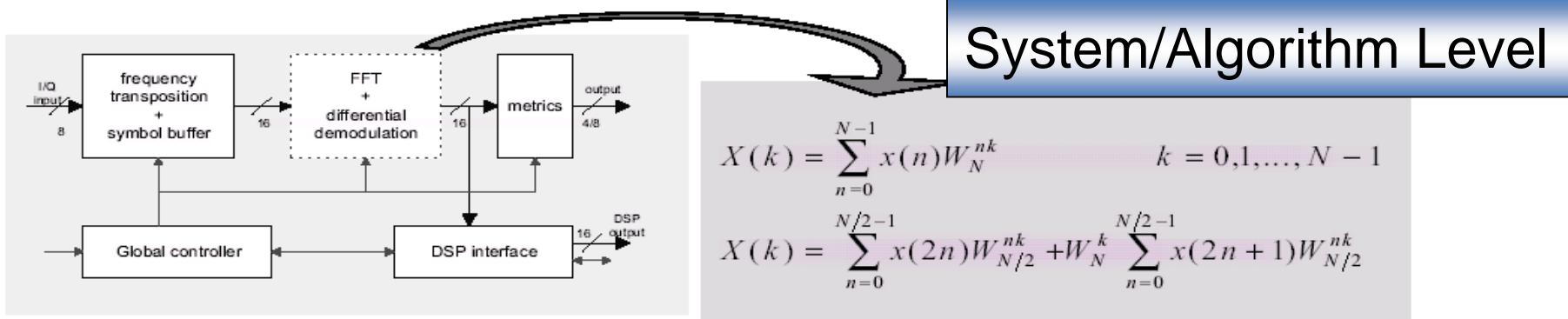
```
module Add_Sub_Unit( result, operand_a, operand_b, mode, detect );
  input [3:0] operand_a, operand_b;
  input mode;
  output [3:0] result;
  output detect; // for question 3
  wire [3:0] xor_b;

  xor g0 ( xor_b[0], operand_b[0], mode );

```

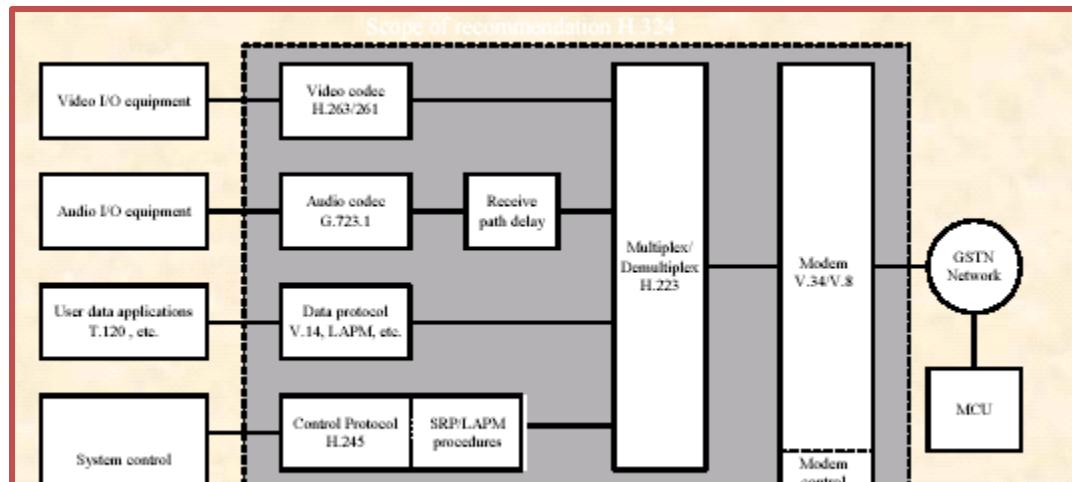


Algorithm Mapping





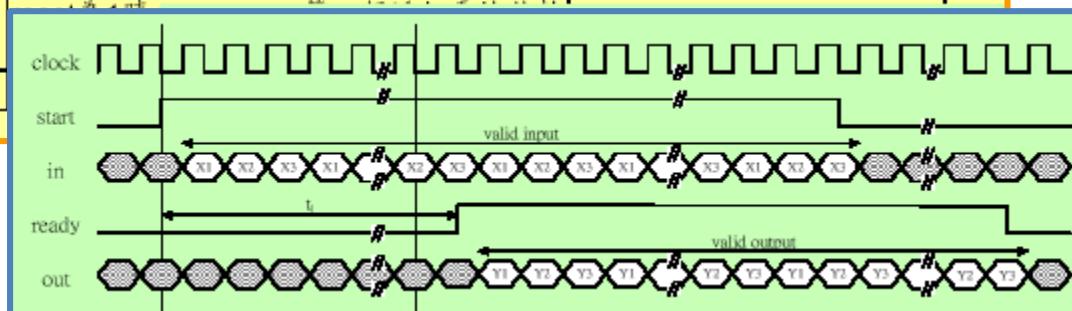
System Specifications



Partition

腳位名稱		描述	Drive Strength/Output Load
clk	輸入	系統時脈	assume infinite
reset	輸入	系統重置訊號，high active	1 ns/pf
din	輸入	每個clock cycle輸入一個16-bit 正整數	1 ns/pf
ready	輸出		
dout	輸出		

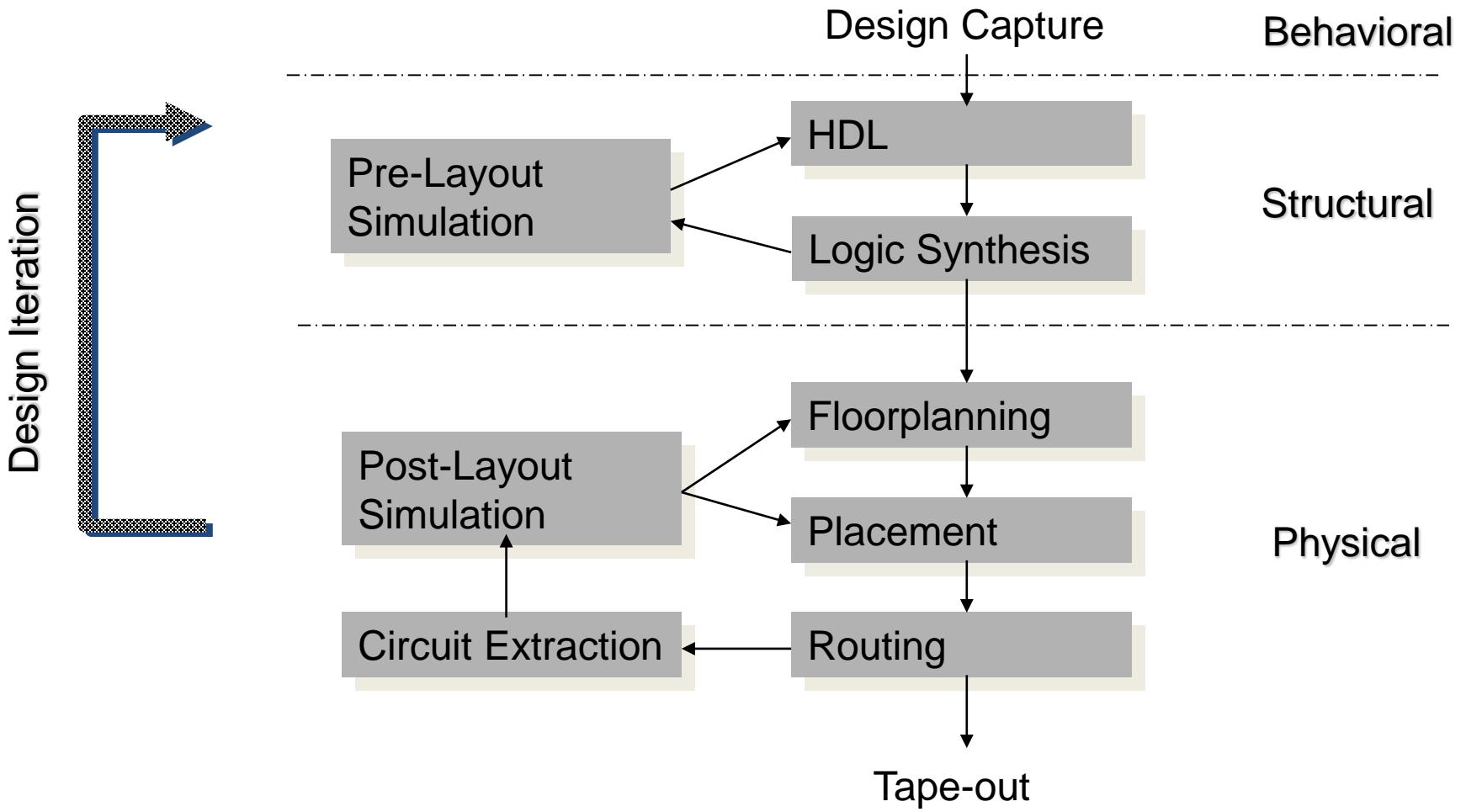
IO Spec.



IO Timing Spec.

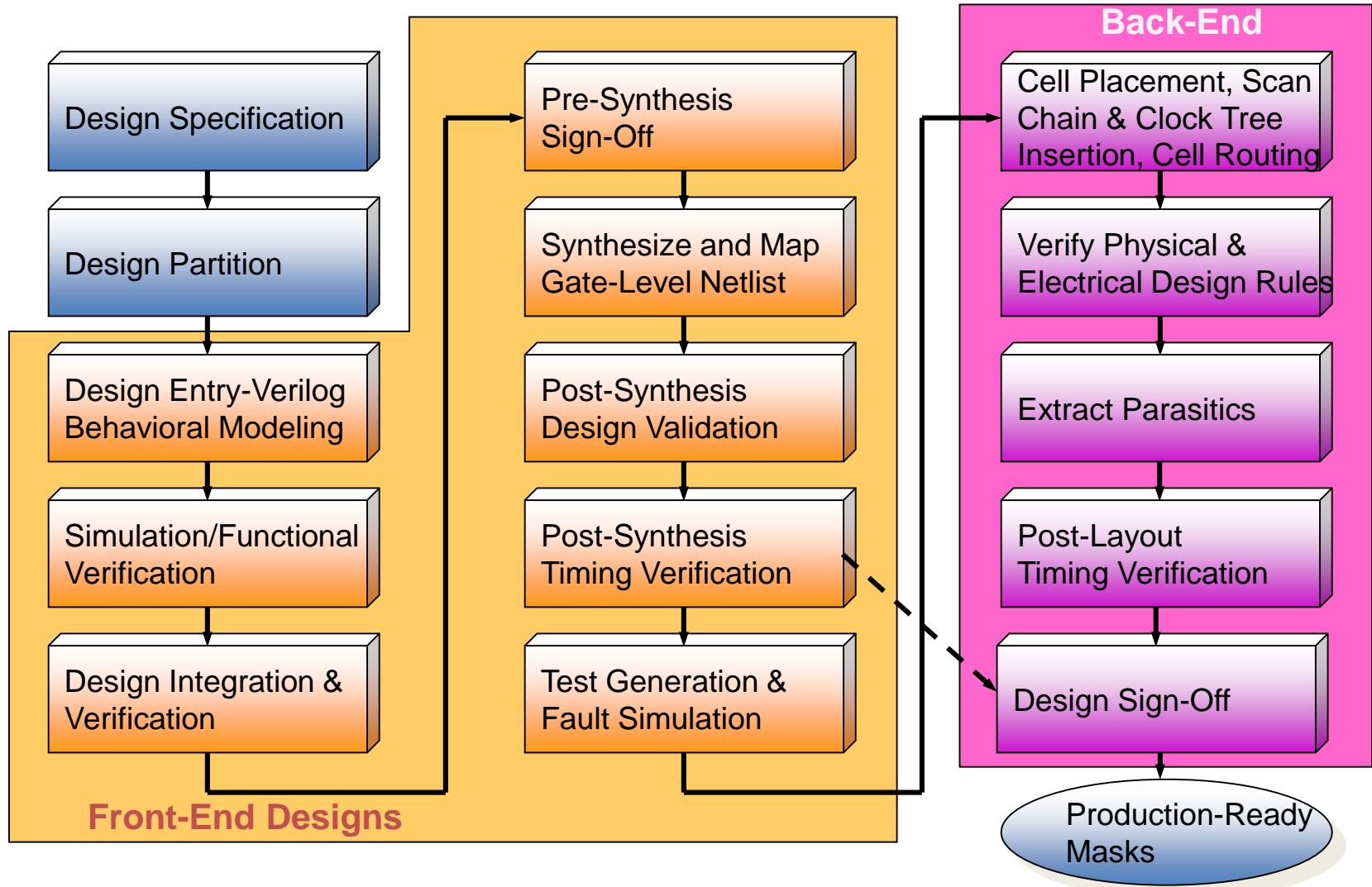


Cell-based Design Flow





Digital IC Design Flow





Introduction

❖ Objective

❖ Students will learn how to design VLSI circuits and systems following a **standard VLSI system design flow**, where various **electronic design automation (EDA) tools** will be used extensively in the semester

❖ Course content

1. Verilog-HDL
2. Synthesis
3. Static Timing Analysis
4. Placement and Routing
5. Verification
6. High-level synthesis
7. Design Rule Check, Layout versus Schematic, Layout Parasitic Extraction



Course Schedule (1)

Week	Date	Lecture	Speaker	Place	Lab	HW assign	HW due
01	09/03	Introduction	楊家驥教授	MD205	Lab0		
02	09/10	Verilog-HDL (1)	張惇宥	Online			
03	09/17	Verilog-HDL (2)	張惇宥	Video	Lab1	HW1	
04	09/24	Verilog-HDL (3)	張均豪	Online			
05	10/01	Verilog-HDL (4)	張均豪	Online	Lab2	HW2	HW1
06	10/08	Synthesis (1)	江承恩	Online	Lab3	HW3	
07	10/15	Synthesis (2)	江承恩	Online			HW2
08	10/22	Static Timing Analysis	莊承霖	Online	Lab4		
09	10/29	Midterm		MD205			
10	11/05	Midterm Review/ Project Announcement	TA	MD205		HW4	HW3



Course Schedule (2)

Week	Date	Lecture	Speaker	Place	Lab	HW assign	HW due
11	11/12	APR (1)	蔡岳峰	Online	Lab5		
12	11/19	APR (2)	蔡岳峰	Online	Lab6	HW5	HW4
13	11/26	APR (3)	蔡岳峰	Online	Lab7		
14	12/03	Cadence Formal Verification	Cadence	Online	Lab8		HW5
15	12/10	High-Level Synthesis	Cadence	Online	Lab9		
16	12/17	PVS/DRC/LVS	Cadence	Online	Lab10		
17	12/24	Project Presentation	-	Online			

Acknowledgment:

- Formal verification, HLS, PVS: 益華科技

cadence®



NARLabs 國家實驗研究院
台灣半導體研究中心
Taiwan Semiconductor Research Institute



Online Course Link

- ❖ Webex:

<https://ntucc.webex.com/ntucc/j.php?MTID=mfaa38ceceb6472a9a9076617bee06c6e>

- ❖ Please log in using “[StudentID]-[Name]” for TA to verify your identity.
- ❖ Your microphone is set to be muted by default. If you have any questions, please use the chatroom to ask.



TA Contact

Lead TA	林祐丞	d10943005@ntu.edu.tw
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Lecture: Verilog-1	張惇宥	r11943017@ntu.edu.tw
Lecture: Verilog-2	張均豪	r12k41024@ntu.edu.tw
Lecture: Synthesis	江承恩	r13943008@ntu.edu.tw
Lecture: STA	莊承霖	r12943017@ntu.edu.tw
Lecture: APR	蔡岳峰	f12943014@ntu.edu.tw
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HW3	張力元	r11943006@ntu.edu.tw
HW4	陳泰融	r11943024@ntu.edu.tw
HW5	廖苡鈞	r13943007@ntu.edu.tw



Course Information

- ❖ Course materials
 - ❖ Lecture notes
 - ❖ Technical documents

- ❖ Course website
 - ❖ <https://cool.ntu.edu.tw/courses/39321>



Grading Policy

- ❖ Participation (Lab): 5%
- ❖ Homework: 30%
 - ❖ Submission to NTU COOL
 - ❖ Deadline: **Tuesday afternoon (13:59 pm)**
- ❖ Midterm Exam: 30%
 - ❖ Closed-book written test
- ❖ Final Project: 35%
 - ❖ A team of 2 students
 - ❖ VLSI design
- ❖ **No late submissions (unless for special cases)**



Enrollment Announcement

Course Registration Priority:

- 1. GIEE ICS/EDA and GSAT ICDA Students:** You can directly get an authorization code for enrollment
 - 2. Research Requirement:** If this course is required for your research, please email us and copy your advisor
 - 3. Other Students with Verilog Experience:** If there are any remaining seats, authorization codes will be allocated through lottery
 - 4. Other Students New to Verilog:** Please take prerequisite courses (e.g., Digital Circuit Lab, Digital System Design, Computer Architecture, Integrated Circuit Design Lab) before taking this course
- ❖ **Auditing:** The course is open for auditing. To be added to the audit list, please email the lead TA
- ❖ **Next Course Offering:** Fall 2025



TSRI Membership Application (for Enrolled Students)

❖ <https://www.tsri.org.tw/main.jsp>

Deadline: 9/9 23:59

The screenshot shows the official website of the Taiwan Semiconductor Research Institute (TSRI). At the top left is the logo 'TSRI' with 'NARLabs 國家實驗研究院' and '台灣半導體研究中心 Taiwan Semiconductor Research Institute'. To the right are language and font size options (EN, A-, A+, A+), and a red-bordered box highlights the '會員服務平台' (Member Service Platform) button. Below the header is a navigation bar with links: 關於中心, 會員服務, 設計服務, 晶片製作, 製程服務, 量測服務, 教育訓練, 技術推廣, 國際合作, 資訊公開, and a search icon. A large banner image of a modern building is on the left, and the text 'INTEGRATION TRANSCENDS LIMITATION' is on the right.

Important Notice:

需於會員資料中填寫指導教授並確認通過

You must fill in your advisor's information in the membership profile and ensure approval.



EE2-231 Server Account (for Enrolled Students)

❖ <https://reurl.cc/Ny1kk9>

Deadline: 9/9 23:59



IC設計實驗室伺服器帳號申請表

實驗室規則：

1. 請勿任意 reboot 主機，破壞系統或做出對系統有害之行為，或將帳號借予他人使用，否則
若經查獲，立即刪除帳號，並交由教授處理。
2. 硬碟使用空間以大學部 1G、碩士班 5G、博士班 10G 為限。
3. 個人資料請隨時自行備份，並於隔年9/1前將個人目錄下的檔案清理乾淨，不保證檔案完整性。
4. 帳號預設期限為一學年，每年9/1將停止上學年申請之帳號，新的學年度請重新申請。
5. 其它注意事項請參閱本實驗室內的實驗室公布欄與實驗室網頁 <http://cad.ee.ntu.edu.tw>。
6. 本伺服器帳號需使用"校內IP"登入，如果是校外IP，請參考 <https://ccnet.ntu.edu.tw/vpn>。

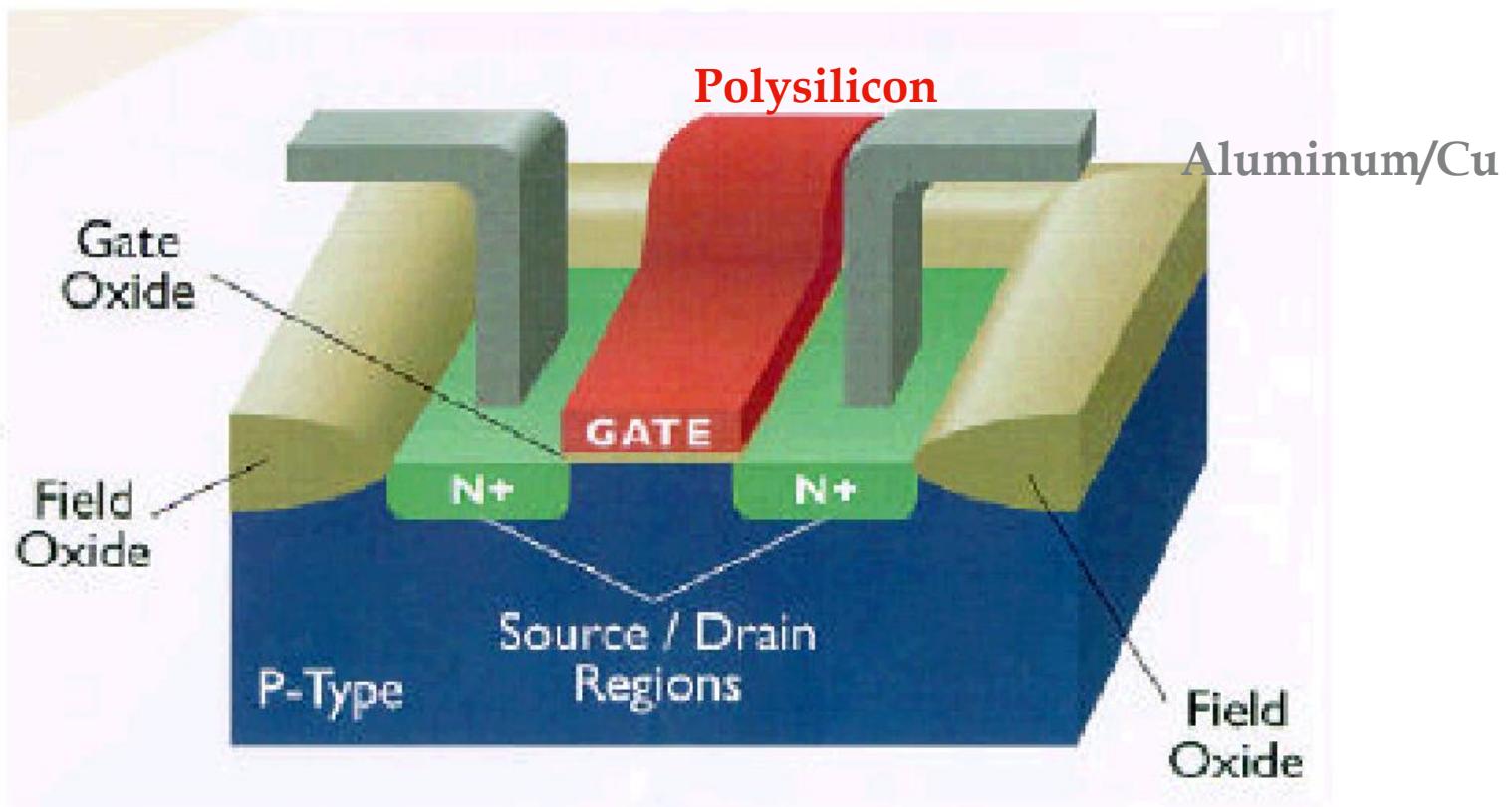


Digital Design Using Integrated Circuits (IC)

& Very Large-Scale IC (VLSI)

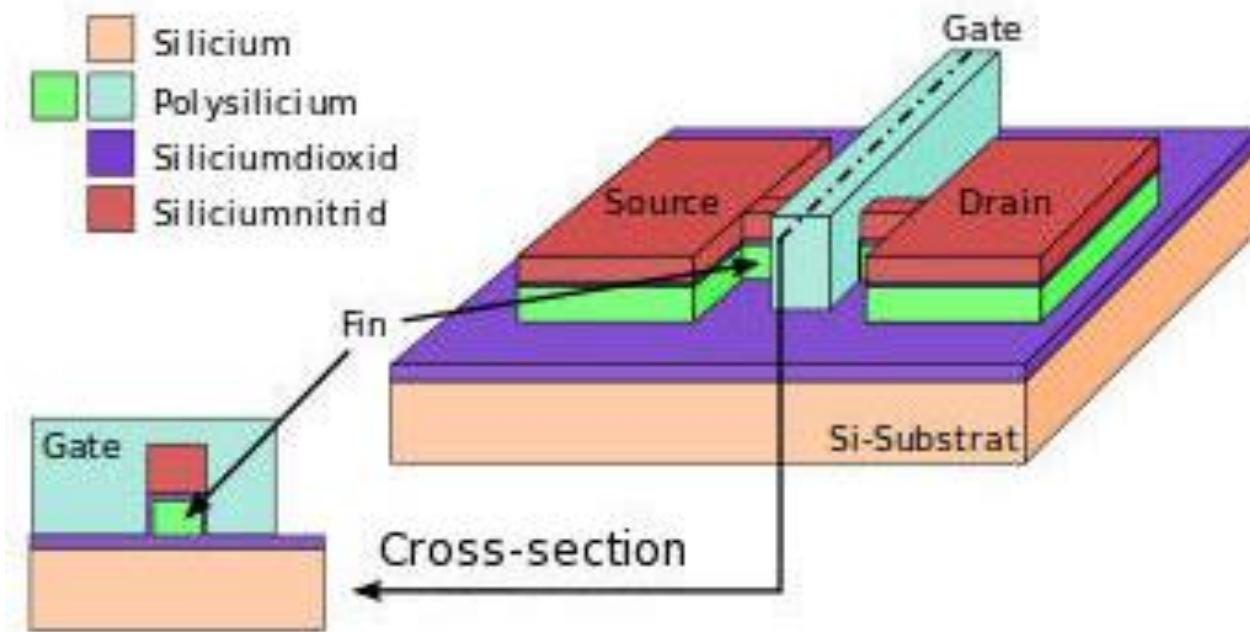


MOS Transistor





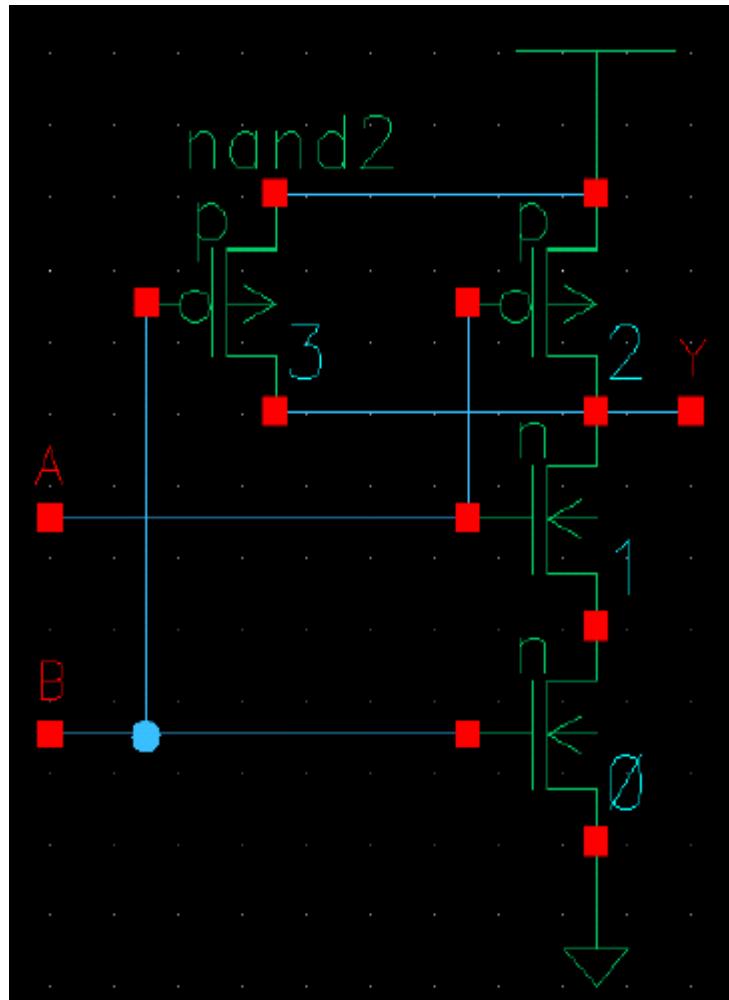
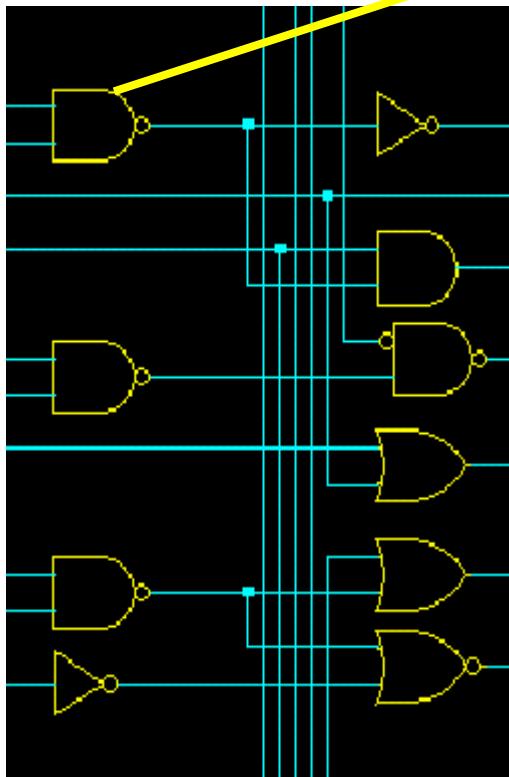
FinFET Transistor



ComputerHope.com

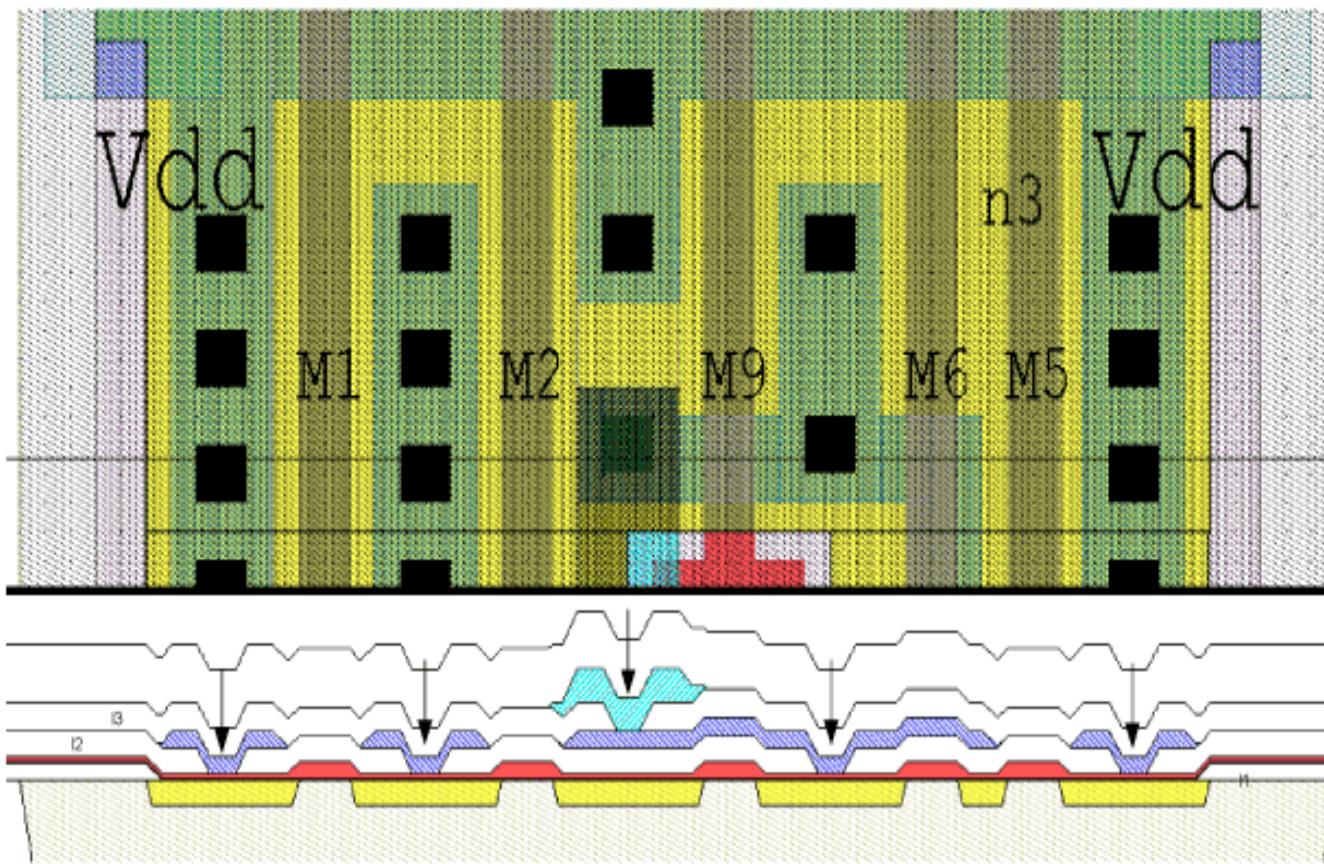


Gate and Circuit Level Design



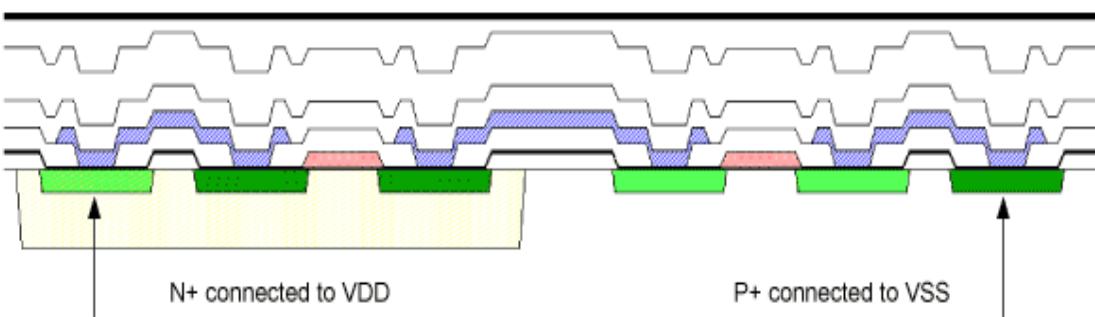
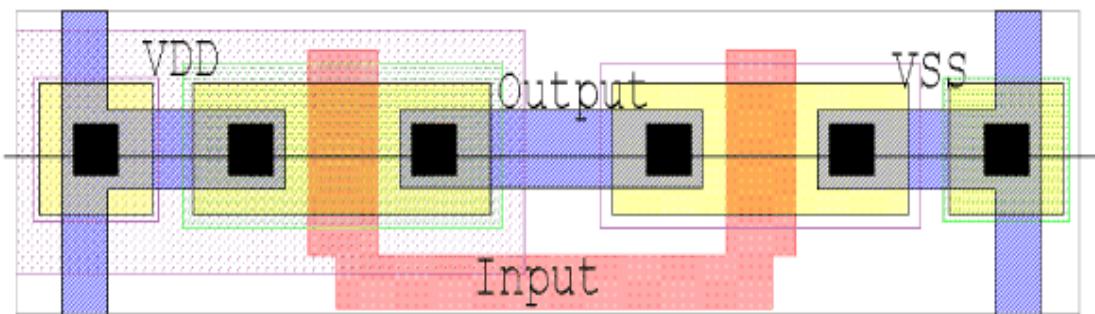
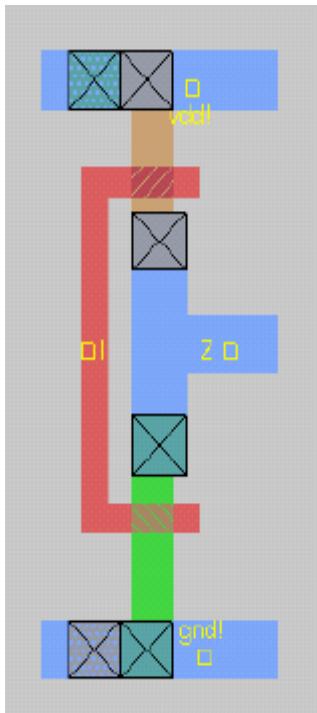


Mapping of Layout to IC Layers



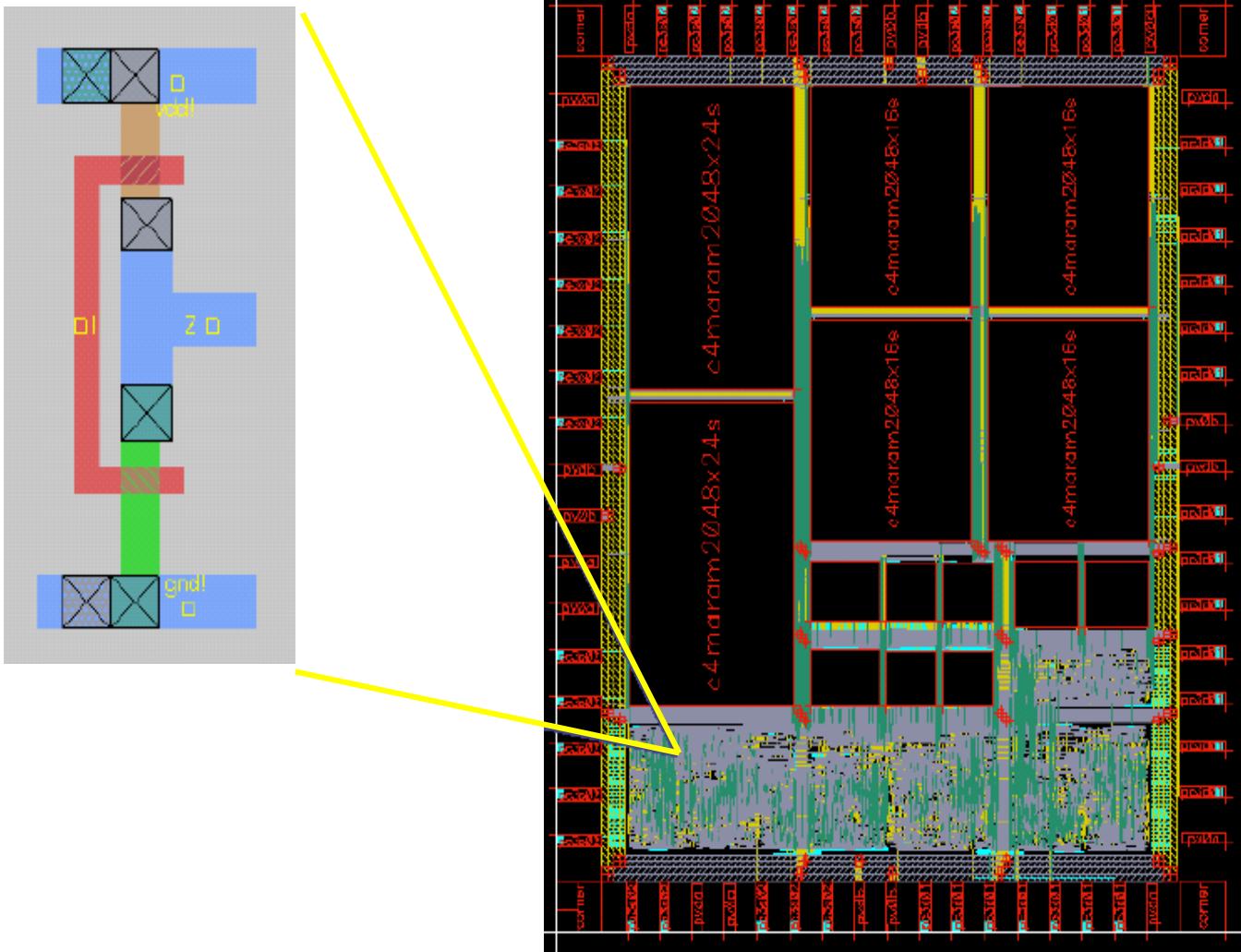


Layout of an CMOS Inverter



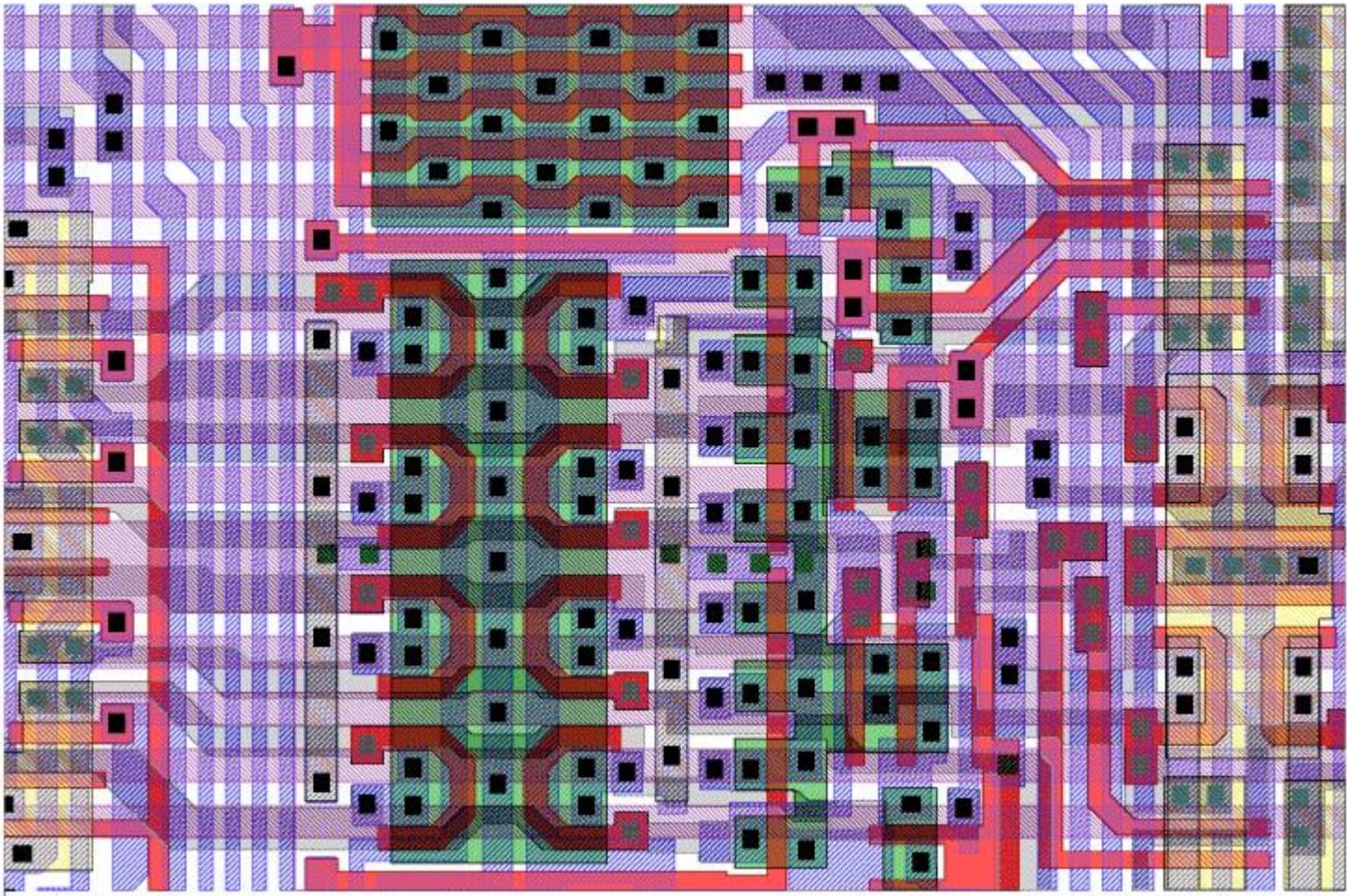


Physical Design



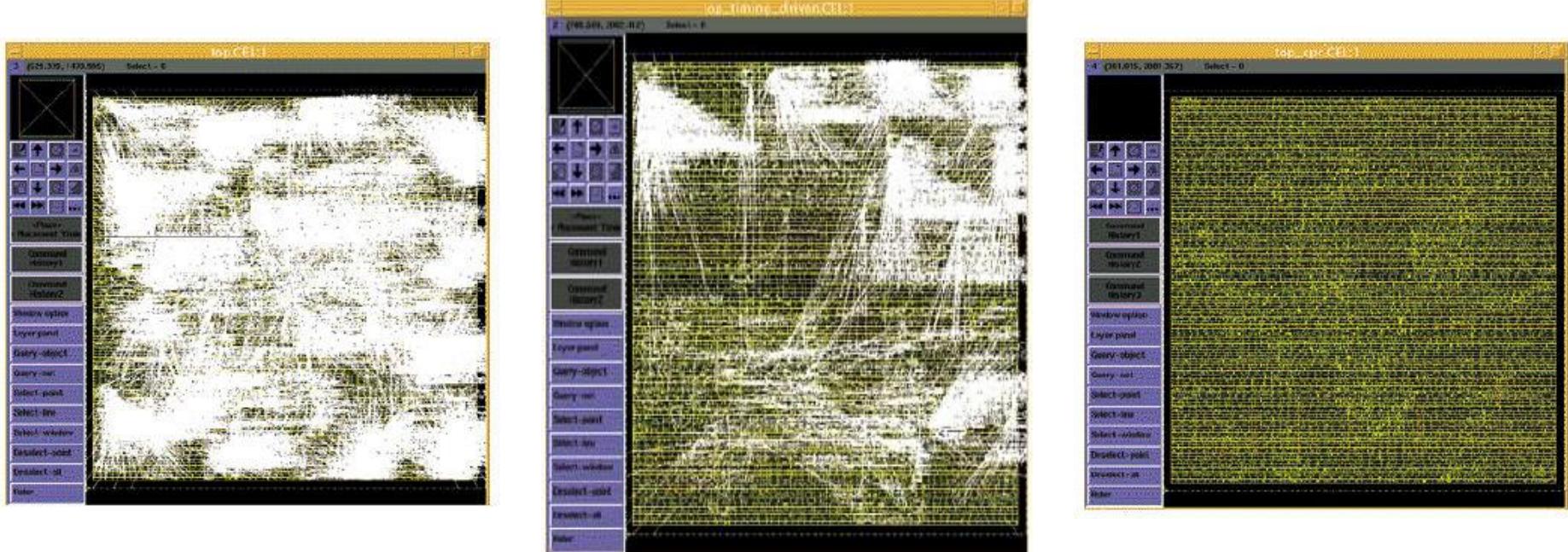


Physical Layout of your design





The “Timing Closure” Problem

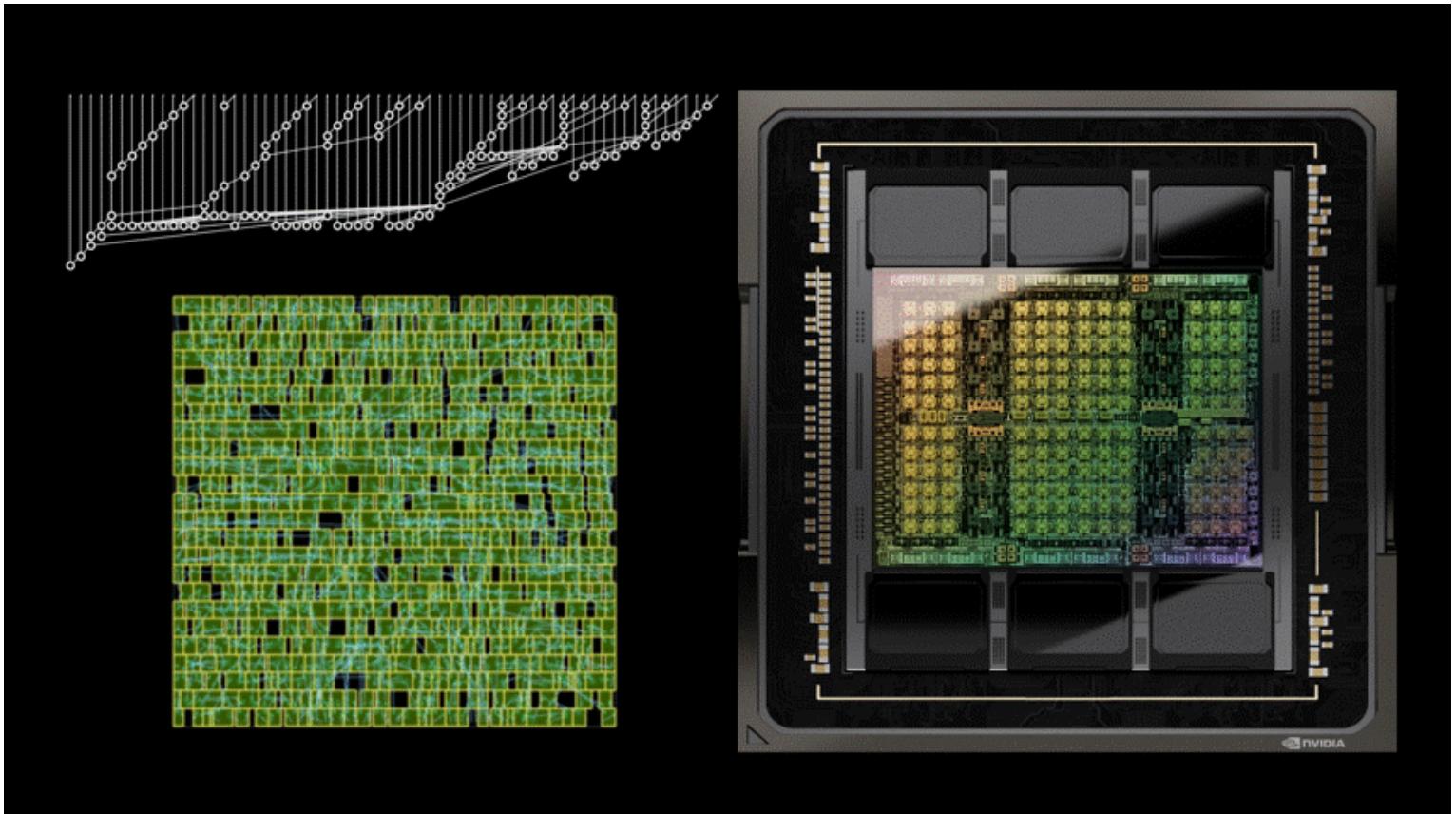


Iterative Removal of Timing Violations (white lines)

Courtesy Synopsys

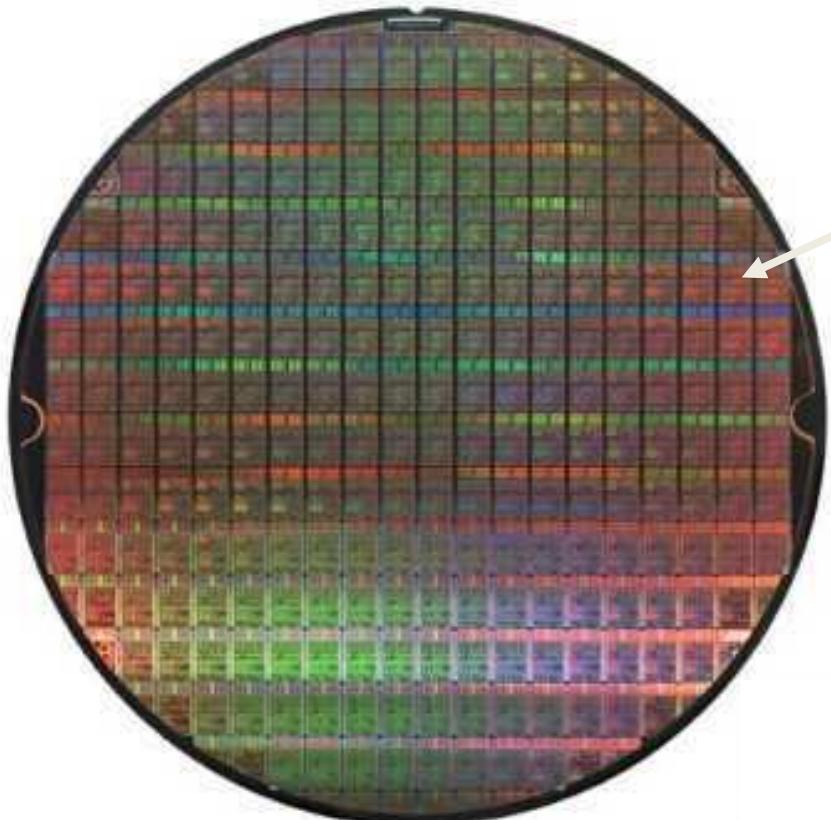


Chip Layout





Die Cost



Single die

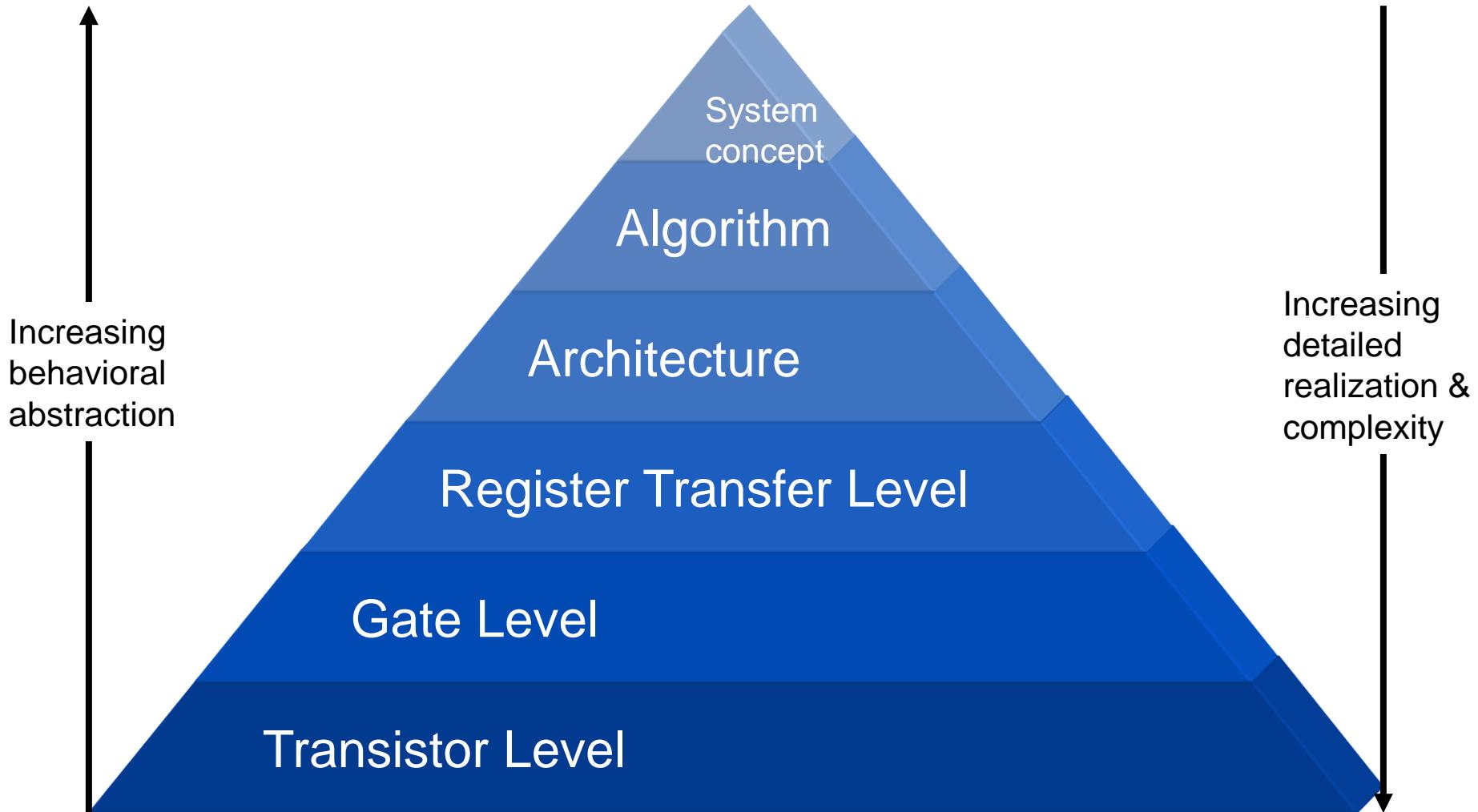
Wafer

Going up to 18"

From <http://www.amd.com>



Behavioral Model





Moore's Law vs. HDL

Issue : Design Productivity



Moore's Law

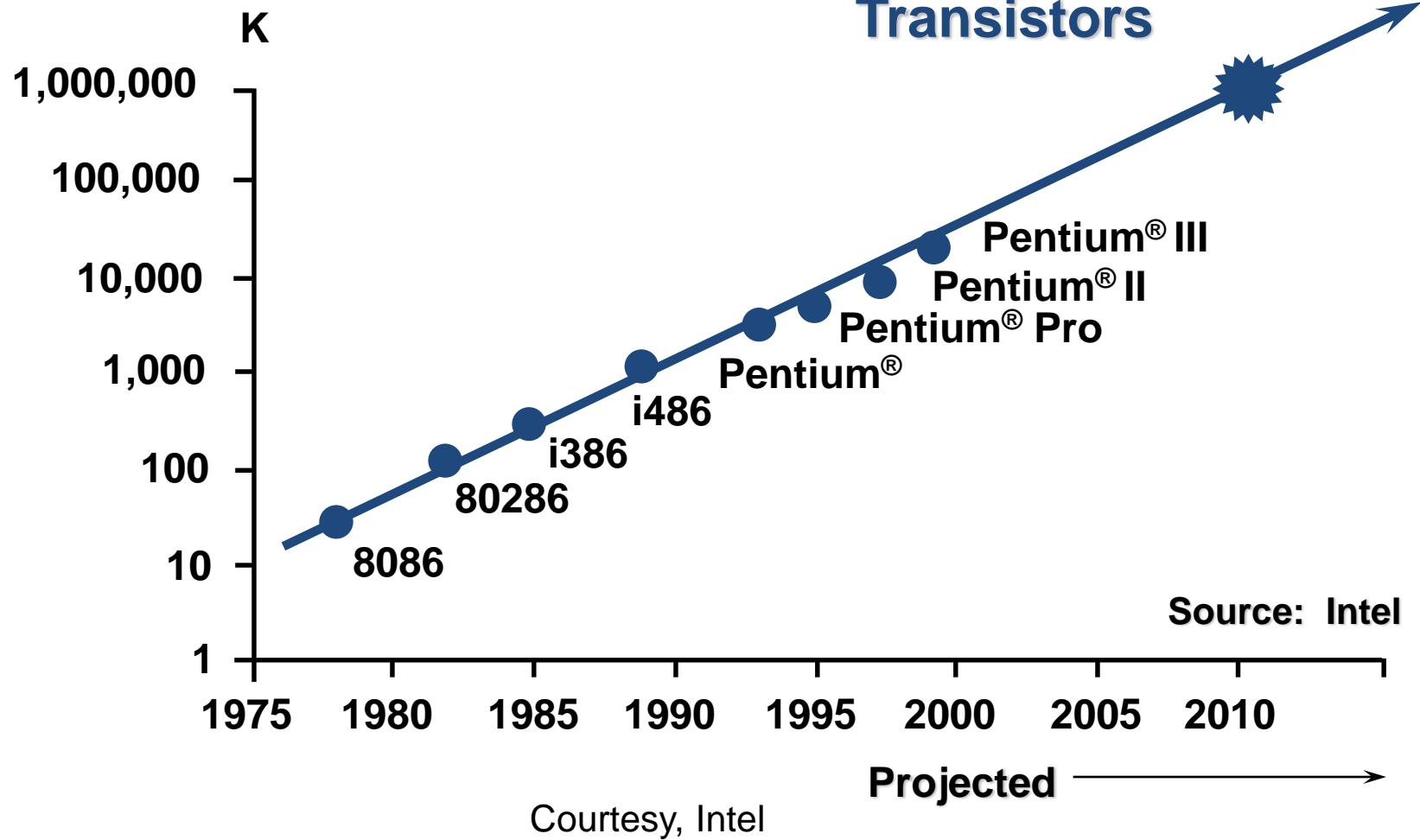
In 1965, *Gordon Moore* noted that the number of transistors on a chip doubled every 18 to 24 months.

He made a prediction that semiconductor technology will **double** its effectiveness **every 18~24 months**



Increased Transistor Count

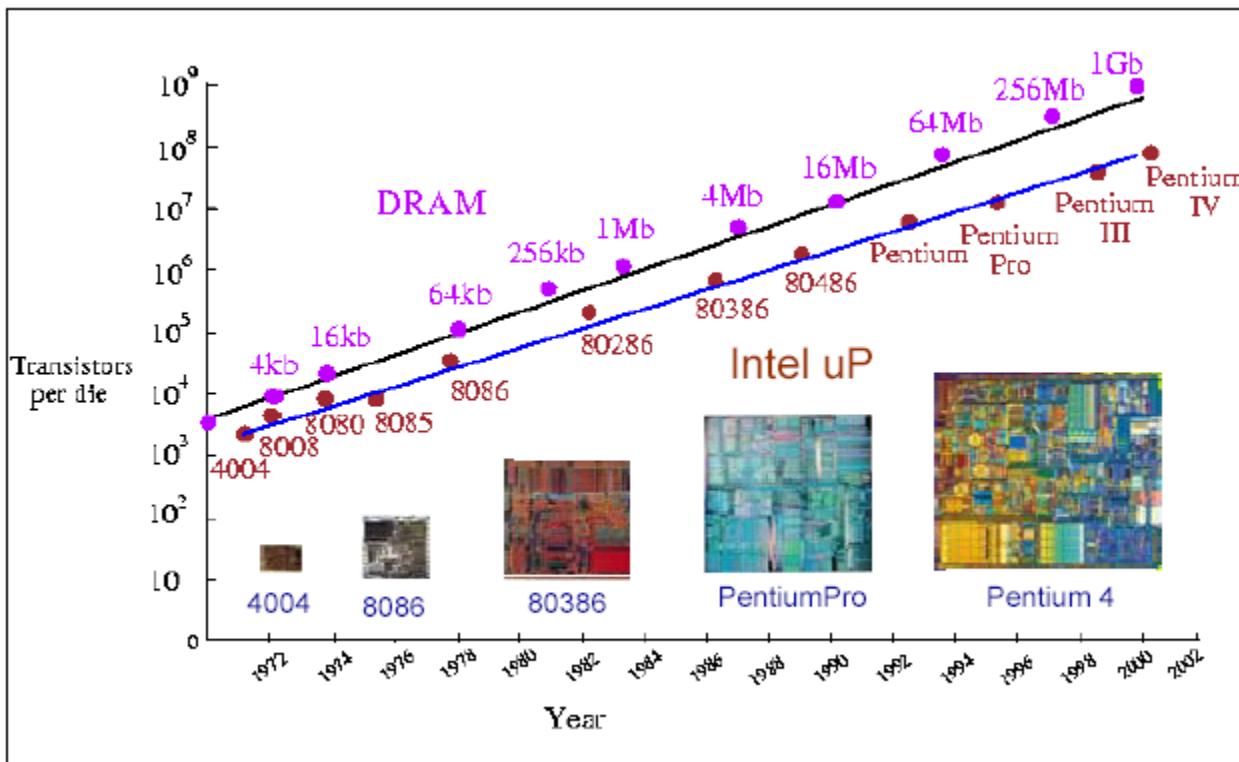
500M~ 1Billion
Transistors





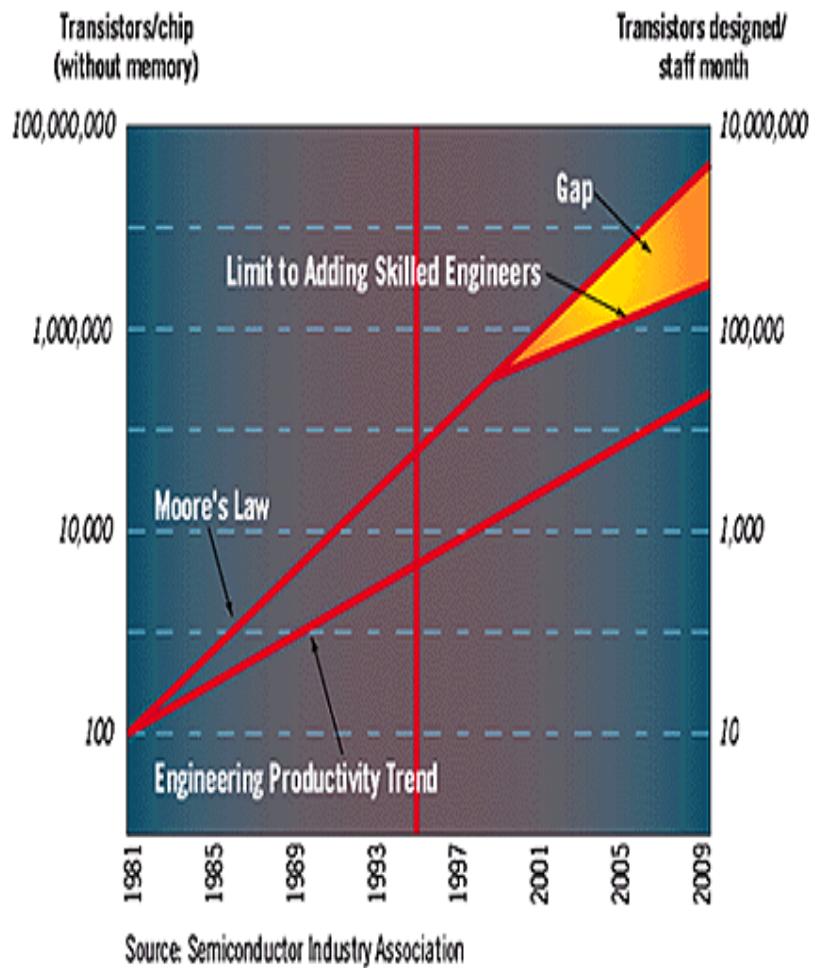
Moore's Law: Driving Technology Advances

- ❖ Logic capacity doubles per IC at regular intervals (1965).
- ❖ Logic capacity doubles per IC every 18 months (1975).





Engineering Productivity Gap

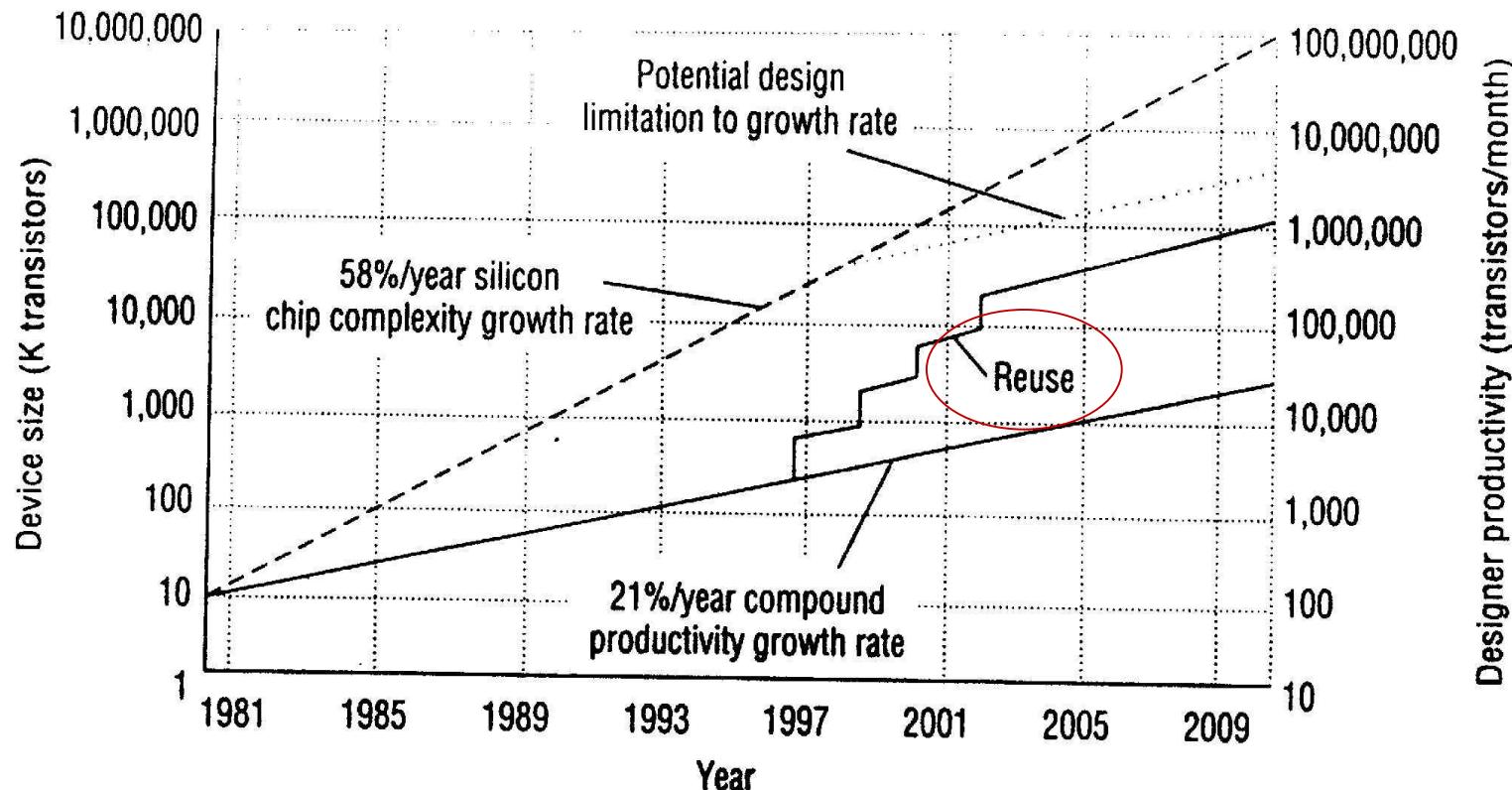


- Engineering productivity has not been keeping up with silicon gate capacity for several years.

- Companies have been using larger design teams, making engineers work longer hours, etc., but clearly the limit is being reached.



Why Must HDL Tools & IP Reuse?



Design productivity crisis:

Divergence of potential design complexity
and designer productivity



HDL and Moore's Law

- ❖ HDL – Hardware Description Language
- ❖ Why use an HDL ?
 - ❖ Unify design entries.
 - ❖ Easy for synthesis:
 - Hardware is becoming very difficult (and too big!) to design directly
 - HDL is easier and cheaper to explore different design options
 - Reduce time and cost to verify your digital designs in VLSI implementations



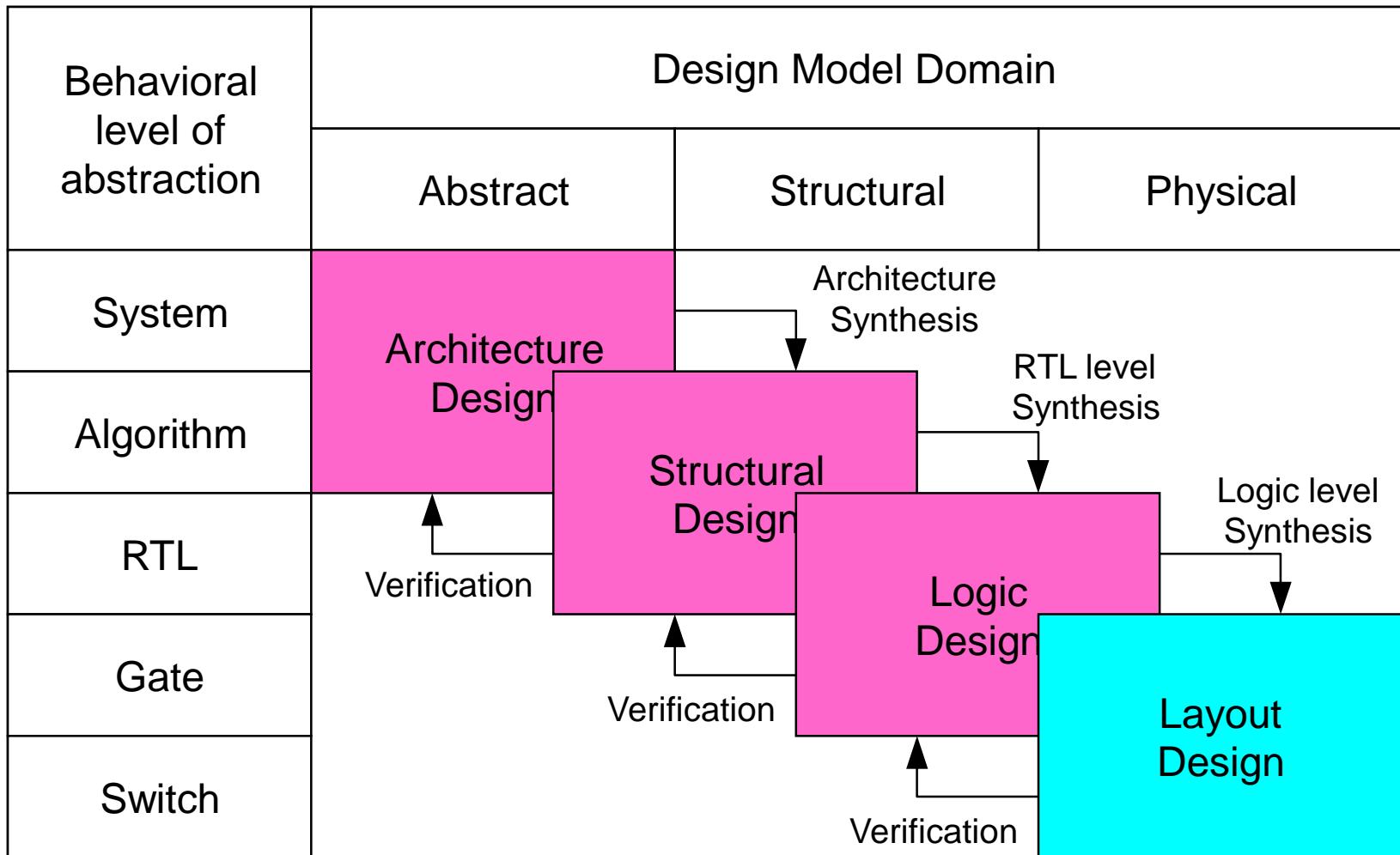
Verilog HDL

❖ Feature

- ❖ HDL has high-level programming language constructs and constructs to describe the connectivity of your circuit.
- ❖ Ability to mix different levels of abstraction freely
- ❖ One language for all aspects of design, test, and verification
- ❖ Functionality as well as timing
- ❖ Concurrency perform target functions
- ❖ Support timing simulation for your design



Verilog HDL in Different Design Domains





Digital IC Design Flow for Better Design Productivity

