**Computer-Aided VLSI System Design**

**Homework 5 Report**

**Due Tuesday, Dec. 3, 13:59**

**Student ID:**

**Student Name:**

**APR Results**

1. Fill in the blanks below.

|  |  |  |
| --- | --- | --- |
| Design Stage | Description | Value |
| P&R | Number of DRC violations (ex: 0)  (Verify -> Verify Geometry…) |  |
| Number of LVS violations (ex: 0)  (Verify -> Verify Connectivity…) |  |
| Die Area (um2) |  |
| Core Area (um2) |  |
| Post-layout  Simulation | Clock Period for Post-layout Simulation (ex. 10ns) |  |
| Follow your design in HW3?  (If not, specify student ID of the designer or ‘from TA’) | |  |

**Questions and Discussion**

1. Attach the snapshot of CCOpt Clock Tree Debugger result (5%).
2. Attach the snapshot of DRC and LVS checking after routing. (5%)
3. Attach the snapshot of the timing report for **setup time and hold time** with no timing violation (post-route). (5%)
4. Show the critical path after post-route optimization. What is the path type? (10%)

(The slack of the critical path should match the smallest slack in the timing report)

1. Attach the snapshot of GDS stream out messages. (10%)
2. Attach the snapshot of the final area result. (5%)
3. Attach the snapshot of your final layout **after adding core filler**. (Remember to switch to **Physical view** and make Pin Shapes visible) (10%)
4. What is your strategy for floorplanning (especially for placing the SRAMs)? What is the reason behind it? (10%)