Image Filter Lab/Homework

This lab implements a simple 2D image filter design. For each pixel in the image, the design will construct a 5x5 pixel matrix with a current focus pixel in the center of the 5x5 matrix. Stratus HLS provides built-in line buffer IP to construct pixel matrix. Once a 5x5 matrix is ready, a filter function (e.g. edge detection) will be called to process the pixel matrix. Eventually, a new image with filter processing will be generated.

**I expect you can experience 1) design productivity (particularly for computation-intensive design) Stratus HLS can achieve, 2) architecture exploration is very easy in Stratus HLS.**

You can get the lab from TA or download it in the welcome mode of Stratus IDE.

Let’s get started. Assume your **Stratus HLS** and **Xcelium** environment is ready. Please execute following instructions and answer the questions (in red).

1. Re-build line buffer and memory model

* image\_filters/> **bdw\_memgen memlib/\*.bdm**
* image\_filters/> **bdw\_ifgen project.tcl iflib/\*.bdl**

2**.** Re-generate Makefile.prj

* image\_filters/> **bdw\_makegen**

3. Have a look for **filter.h** and **filter.cc**

4. Run SystemC simulation in Konsole

* image\_filters/> **make sim\_B**
* **Question 1: What image do you see? Please capture and paste it.**

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| **Your Answer:** |

5. Run Verilog simulation (Stratus will do HLS automatically) for EDGE\_BASIC configuration

* image\_filters/> **make sim\_EDGE\_BASIC\_V**
* **Question 2: What is throughput you see in the Konsole?**

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| **Your Answer:** |

* **Question 3: Please verify the throughput in waveform view? Please capture and paste it.**
  + **HINT:**
    - **cd bdw\_work/sims/EDGE\_BASIC\_V**
    - **simvision &**
    - ***File* → *Open Database…* → EDGE\_BASIC\_V.shm/EDGE\_BASIC\_V.trn**
    - **Click Open & Dismiss**
    - **the number of cycles between two valid sc\_main/system/dout\_vld**

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| **Your Answer:** |

6. Invoke Stratus HLS IDE

* **image\_filters/> stratus\_ide &**

7. Check Resource Sharing

* **double-click EDGE\_BASIC🡪 Dashboard 🡪 Resources**
* Search **filter\_Mul\_\* and filter\_Add\_\*** byfilter
  + 
* **Question 4: How many multipliers and adder are allocated?**

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| **Your Answer:** |

* **Question 5: How many multiplication operations are bound/shared to the multiplier?**
  + **HINT:**
    - Search **filter\_Mul\_\*** byfilter, and check the attribute “# Ops” of the multiplier

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| **You Answer:** |

8. Run Verilog simulation (Stratus will do HLS automatically) for EDGE\_LAT configuration

* image\_filters/> **make sim\_EDGE\_LAT\_V**
* **Question 6: What is throughput you see in the Konsole?**

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| **Your Answer:** |

* **Question 7: How many multipliers and adder are allocated?**

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| **Your Answer:** |

9. Run Verilog simulation (Stratus will do HLS automatically) for EDGE\_PIPE configuration

* image\_filters/> **make sim\_EDGE\_PIPE\_V**
* **Question 8: What is throughput you see in the Konsole?**

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| **Your Answer:** |

* **Question 9: How many multipliers and adder are allocated?**

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| **Your Answer:** |

10. QoR overview for all architecture implementation

* **In IDE🡪double click ‘filter’**
* **Question 10: What do you see? Please capture and paste it.**

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| **Your Answer:** |