Lab4: Automatic Place & Route

Adviser: Prof. Tzi-Dar Chiueh
TA : Ti-Yu Chen
Mar 15 2024

Derived from slides by Chung-Hao Wu

Outline

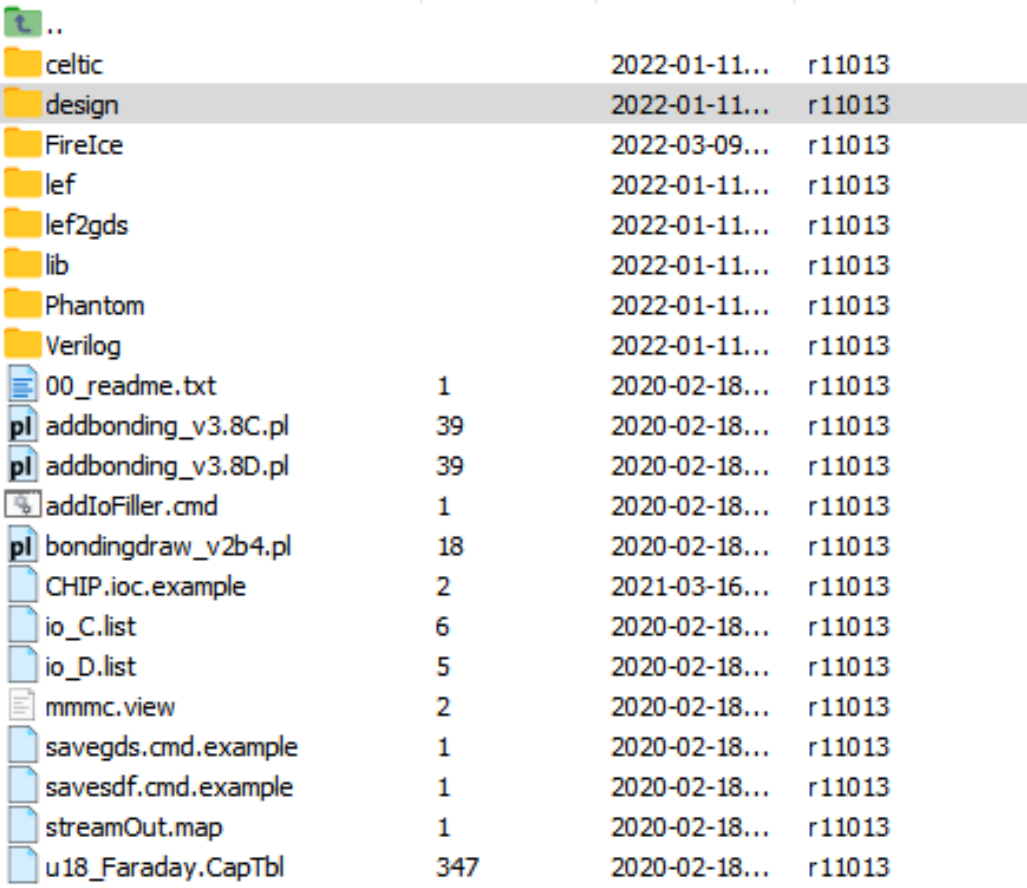
- Prepare Data
- Automatic Place & Route - Innovus
- Stream Out Data

Design Setup

- Library Data
  - Technology File
  - Reference Libraries
- Design Data
  - Gate-level Netlist (.v) with pad definitions
  - Timing Constraints (.sdc)
  - IO constraints (.ioc)

Design Setup (cont.)

- Put .v, .sdc, and .ioc into folder “design”
- Simulation lib in folder “Verilog”
  - Core and io pad lib



Pad definitions

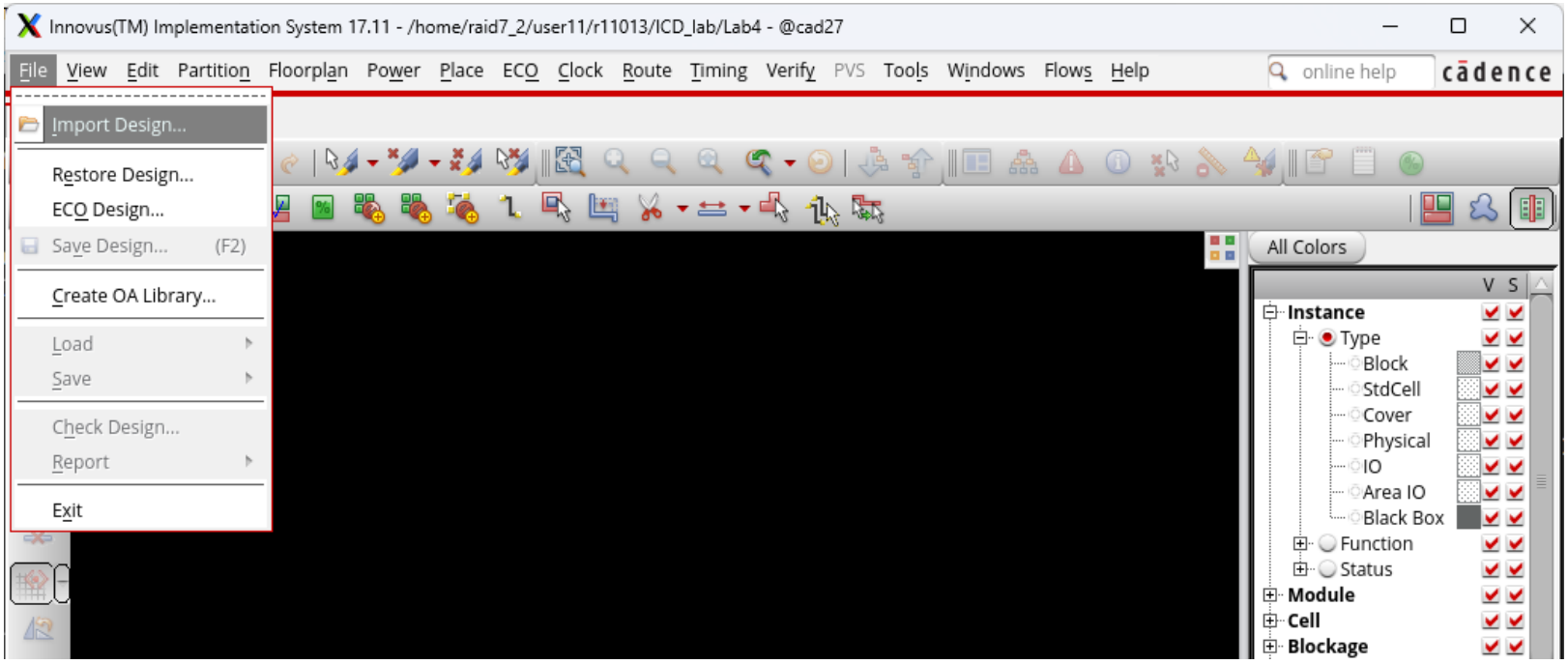
- Instantiate your design in module “CHIP”
- XMD is input pad and YA2GSD is output pad
- Using “TIE” module to assign 0/1

```
module CHIP ( clk_p_i, reset_n_i, data_a_i, data_b_i, inst_i, data_o );
  input [7:0] data_a_i;
  input [7:0] data_b_i;
  input [2:0] inst_i;
  output [15:0] data_o;
  input clk_p_i, reset_n_i;

  wire [7:0] i_data_a_i;
  wire [7:0] i_data_b_i;
  wire [2:0] i_inst_i;
  wire [15:0] i_data_o;
  wire i_clk_p_i, i_reset_n_i;
  wire n_logic0,n_logic1;
  alu alu_in( .clk_p_i(i_clk_p_i), .reset_n_i(i_reset_n_i), .data_a_i(i_data_a_i), .data_b_i(i_data_b_i), .inst_i(i_inst_i), .data_o(i_data_o) );

  TIE0 ipad_n_logic0(.O(n_logic0));
  TIE1 ipad_n_logic1(.O(n_logic1));
  XMD ipad_clk_p_i (.O(i_clk_p_i), .I(clk_p_i), .PU(n_logic0), .PD(n_logic0), .SMT(n_logic0));
  XMD ipad_reset_n_i (.O(i_reset_n_i), .I(reset_n_i), .PU(n_logic0), .PD(n_logic0), .SMT(n_logic0));
  XMD ipad_inst_i_0  (.O(i_inst_i[0]), .I(inst_i[0]), .PU(n_logic0), .PD(n_logic0), .SMT(n_logic0));
  XMD ipad_inst_i_1  (.O(i_inst_i[1]), .I(inst_i[1]), .PU(n_logic0), .PD(n_logic0), .SMT(n_logic0));
  XMD ipad_inst_i_2  (.O(i_inst_i[2]), .I(inst_i[2]), .PU(n_logic0), .PD(n_logic0), .SMT(n_logic0));
  XMD ipad_data_a_i_0 (.O(i_data_a_i[0]), .I(data_a_i[0]), .PU(n_logic0), .PD(n_logic0), .SMT(n_logic0));
```

```
YA2GSD ipad_data_o_0 (.O(data_o[0]), .I(i_data_o[0]), .E(n_logic1), .E2(n_logic0), .E4(n_logic0), .E8(n_logic0), .SR(n_logic0));
YA2GSD ipad_data_o_1 (.O(data_o[1]), .I(i_data_o[1]), .E(n_logic1), .E2(n_logic0), .E4(n_logic0), .E8(n_logic0), .SR(n_logic0));
YA2GSD ipad_data_o_2 (.O(data_o[2]), .I(i_data_o[2]), .E(n_logic1), .E2(n_logic0), .E4(n_logic0), .E8(n_logic0), .SR(n_logic0));
```

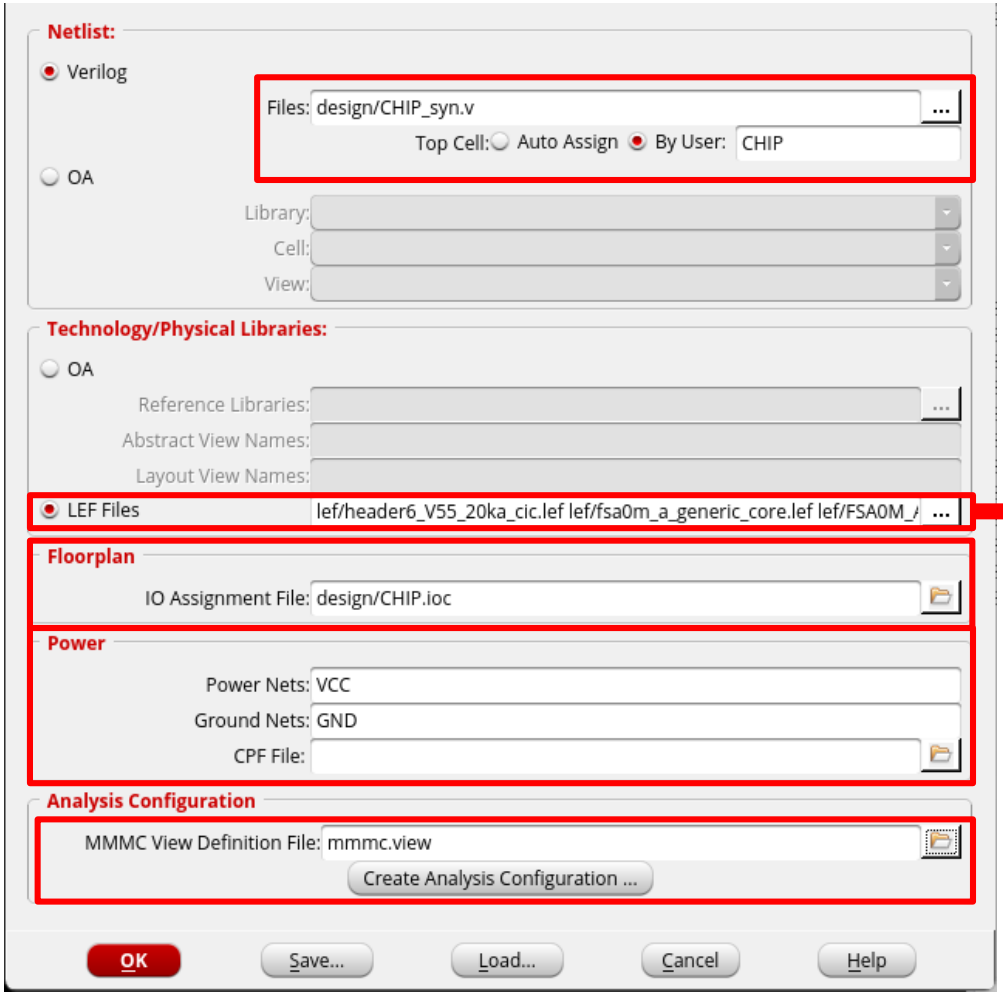
Start Innovus

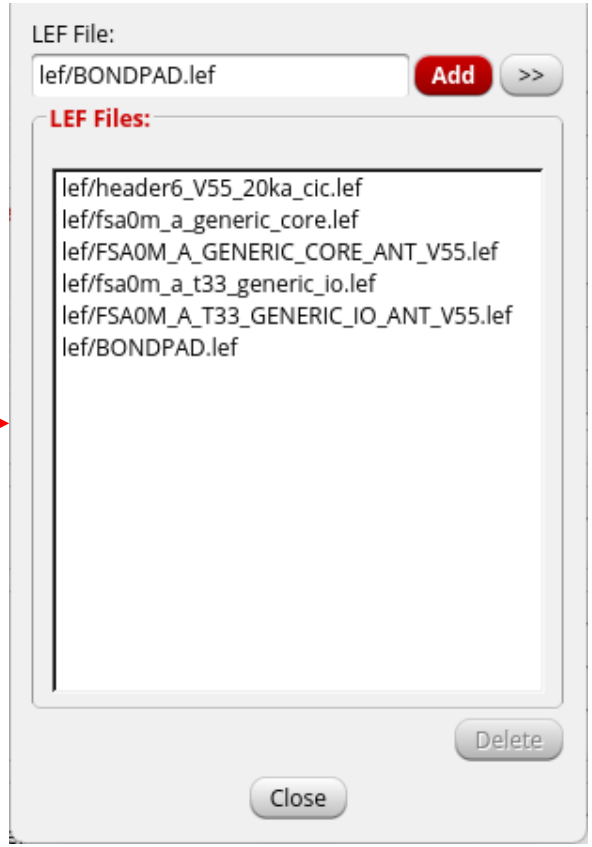
- source innovus.cshrc
- File → Import Design…



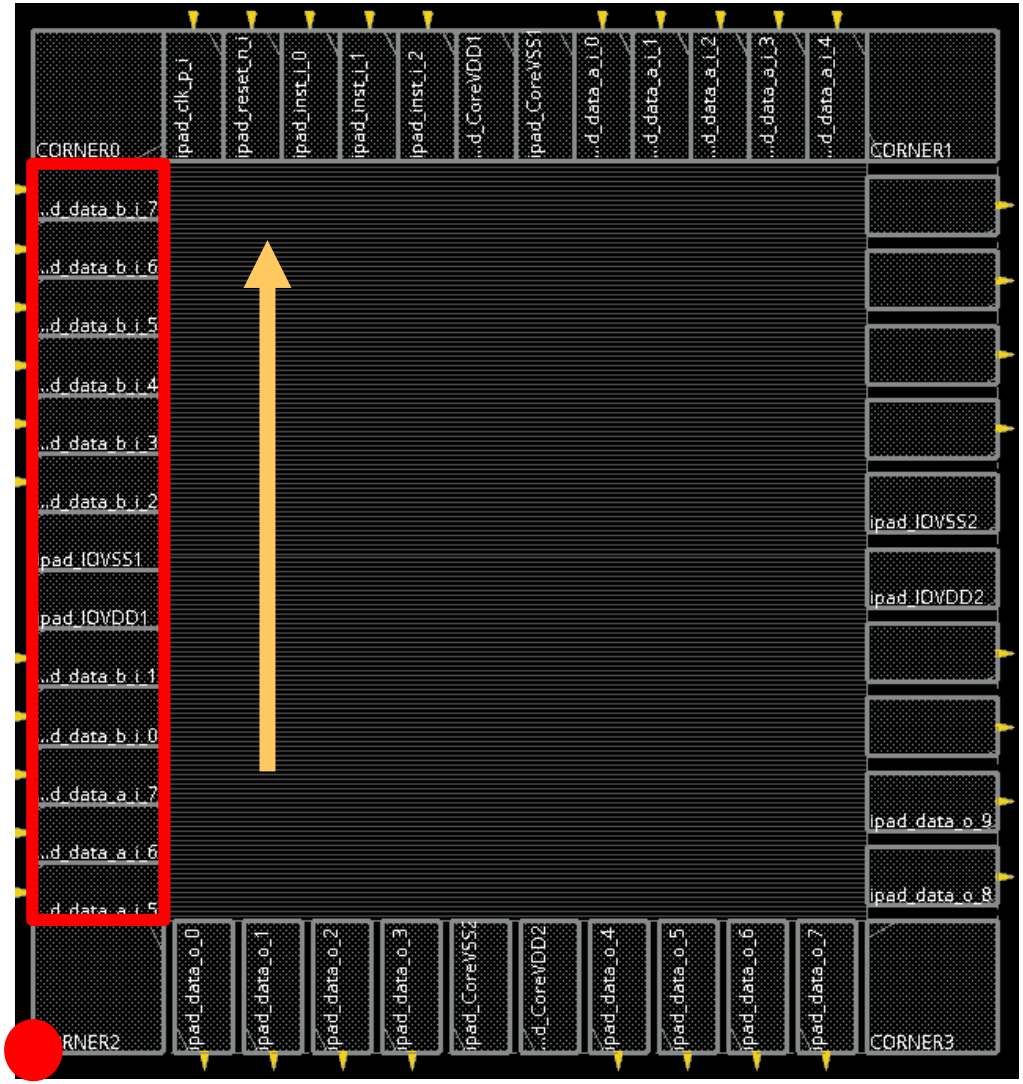
Import Design

- Be careful with order of LEF files





IOC file and chip view

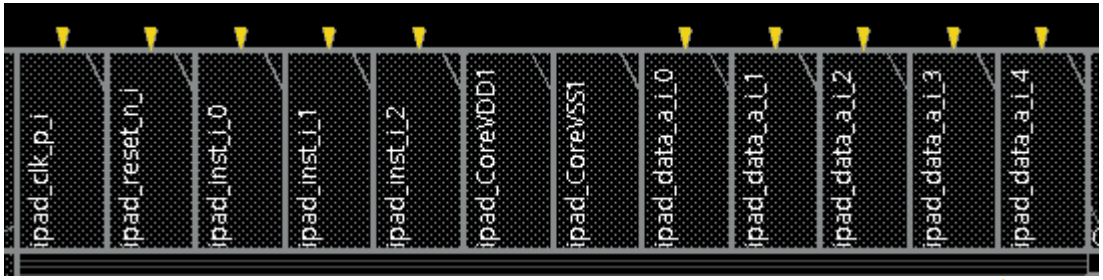



```
Orient: R0
Pad: CORNER1          NE  CORNERD
Pad: ipad_data_a_i_5  W
Pad: ipad_data_a_i_6  W
Pad: ipad_data_a_i_7  W
Pad: ipad_data_b_i_0  W
Pad: ipad_data_b_i_1  W
Pad: ipad_IOVDD1      W   VCC3IOD
Pad: ipad_IOVSS1      W   GNDIOD
Pad: ipad_data_b_i_2  W
Pad: ipad_data_b_i_3  W
Pad: ipad_data_b_i_4  W
Pad: ipad_data_b_i_5  W
Pad: ipad_data_b_i_6  W
Pad: ipad_data_b_i_7  W
```

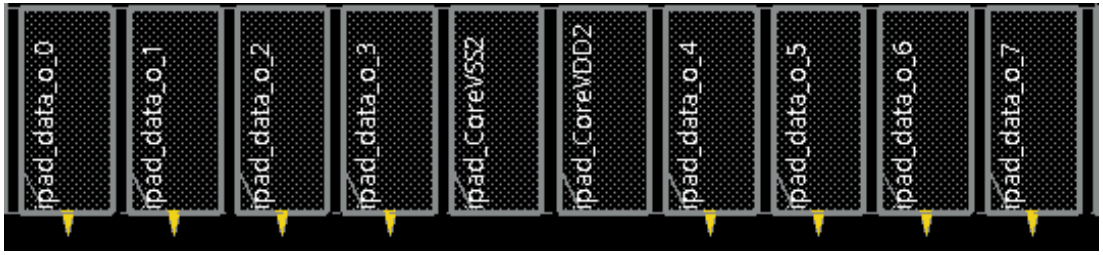
```
Orient: R270
Pad: CORNER3          SE  CORNERD
Pad: ipad_data_o_8    E
Pad: ipad_data_o_9    E
Pad: ipad_data_o_10   E
Pad: ipad_data_o_11   E
Pad: ipad_IOVDD2      E   VCC3IOD
Pad: ipad_IOVSS2      E   GNDIOD
Pad: ipad_data_o_12   E
Pad: ipad_data_o_13   E
Pad: ipad_data_o_14   E
Pad: ipad_data_o_15   E
```

IOC file and chip view (cont.)

N



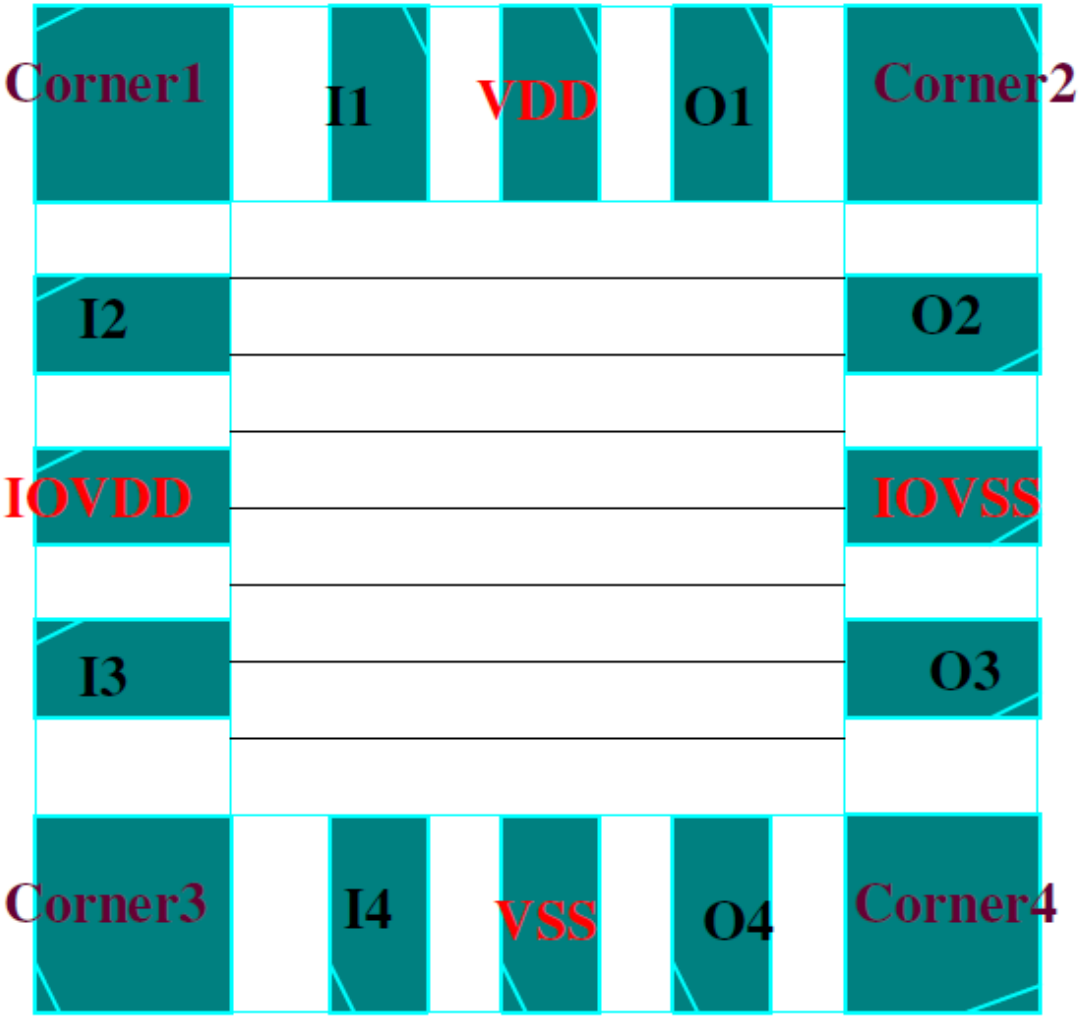
S




```
Orient: R90
Pad: CORNER0           NW   CORNERD
Pad: ipad_clk_p_i      N
Pad: ipad_reset_n_i    N
Pad: ipad_inst_i_0     N
Pad: ipad_inst_i_1     N
Pad: ipad_inst_i_2     N
Pad: ipad_CoreVDD1     N    VCCKD
Pad: ipad_CoreVSS1     N    GNDKD
Pad: ipad_data_a_i_0   N
Pad: ipad_data_a_i_1   N
Pad: ipad_data_a_i_2   N
Pad: ipad_data_a_i_3   N
Pad: ipad_data_a_i_4   N
```

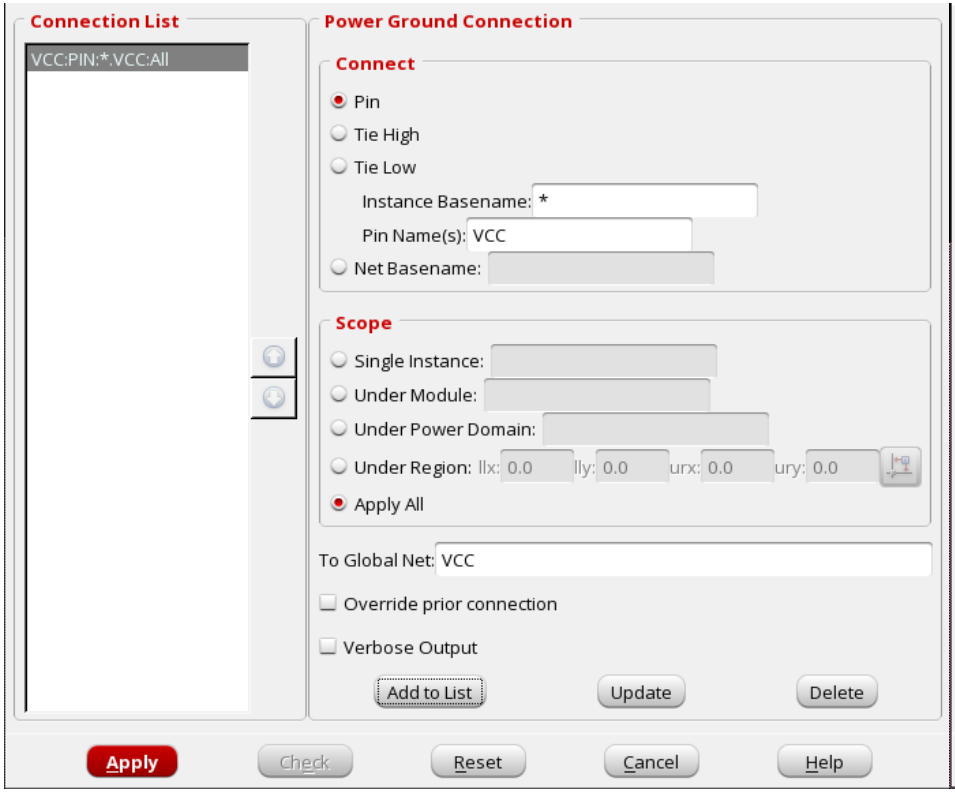
```
Orient: R180
Pad: CORNER2           SW   CORNERD
Pad: ipad_data_o_0     S
Pad: ipad_data_o_1     S
Pad: ipad_data_o_2     S
Pad: ipad_data_o_3     S
Pad: ipad_CoreVSS2     S    GNDKD
Pad: ipad_CoreVDD2     S    VCCKD
Pad: ipad_data_o_4     S
Pad: ipad_data_o_5     S
Pad: ipad_data_o_6     S
Pad: ipad_data_o_7     S
```

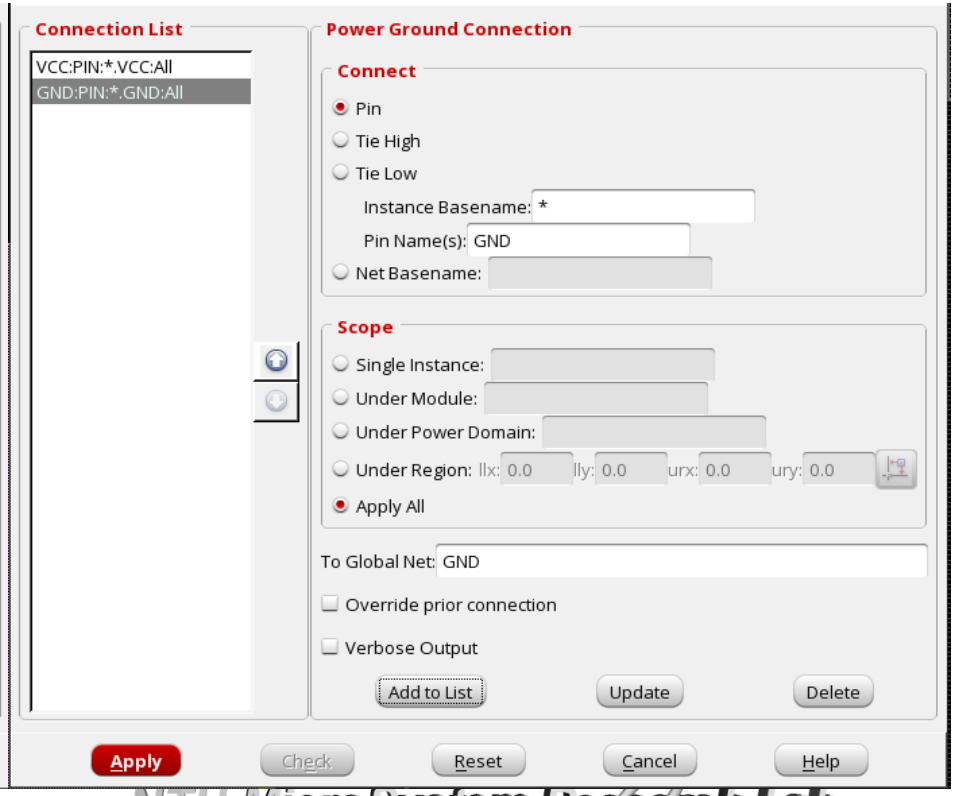
IOC file and chip view (cont.)



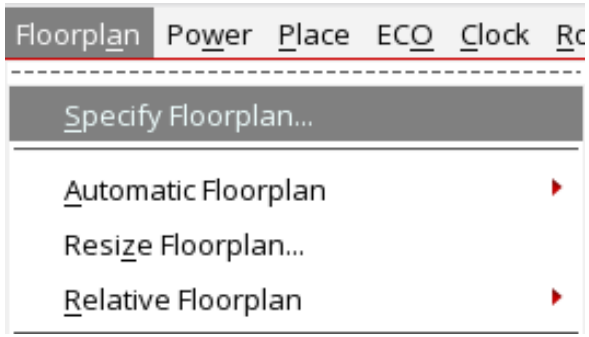
Global Net Connect

- Power → Connect Global Nets
  - Connect cells' power/ground pin to VCC/GND

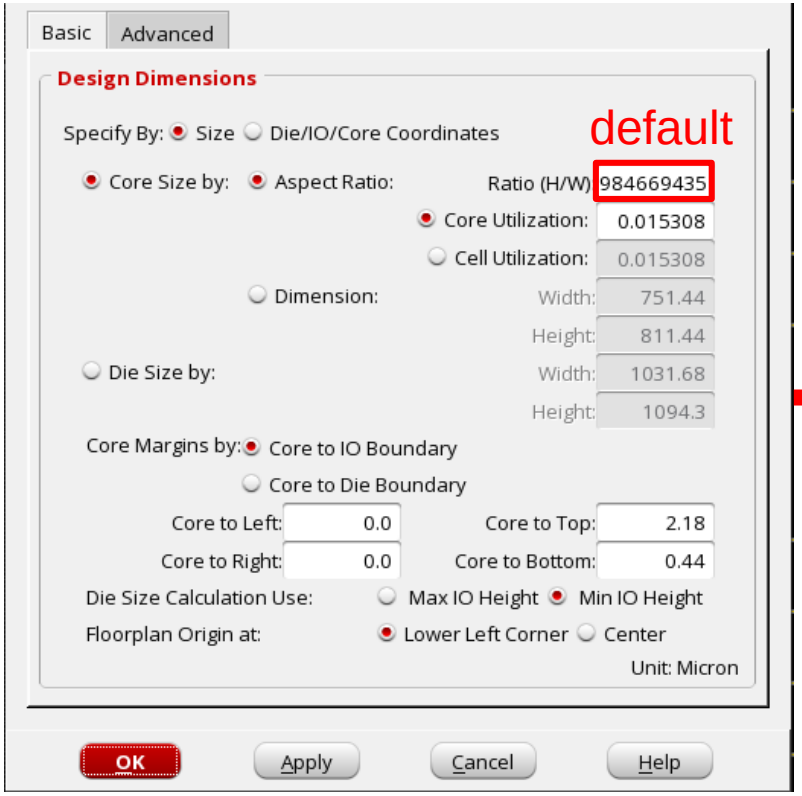


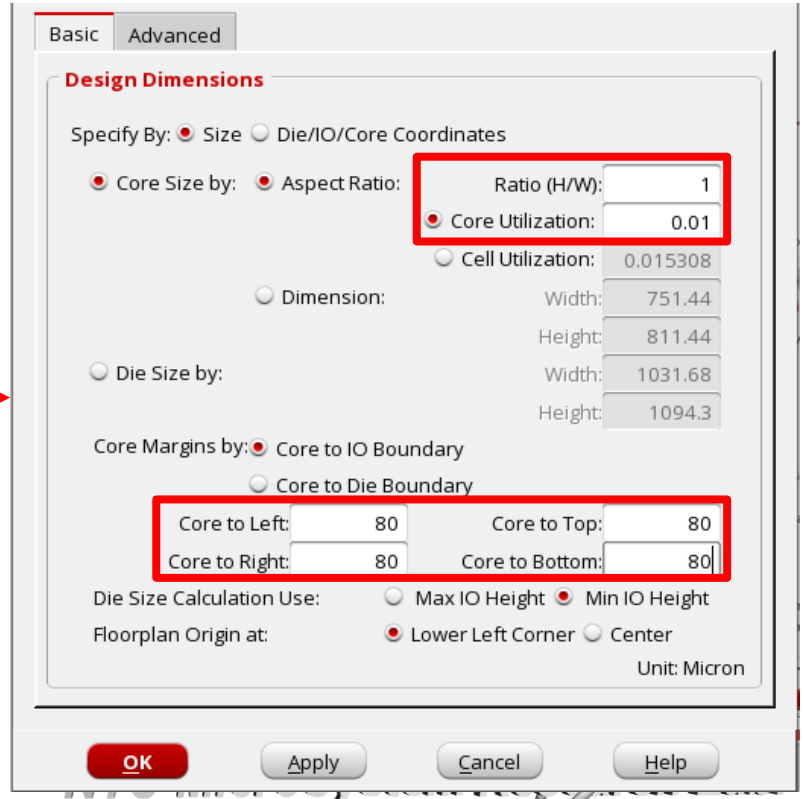


Specify Floorplan

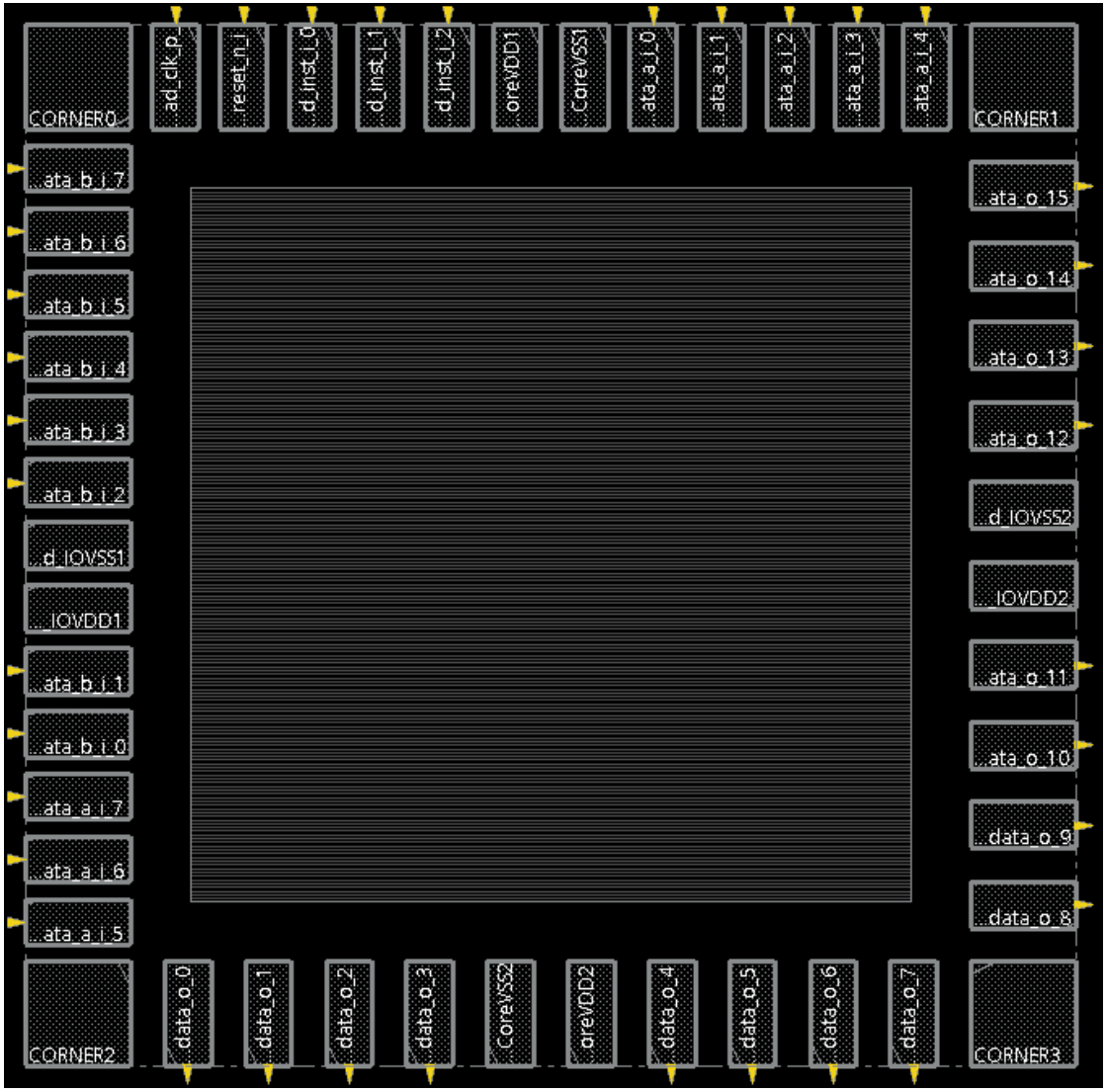


- Floorplan → Specify Floorplan
  - Core ult. should be smaller than default value
  - Be careful with space between pads



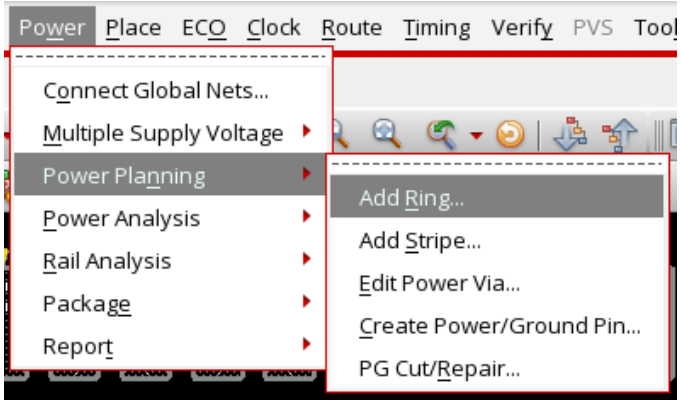


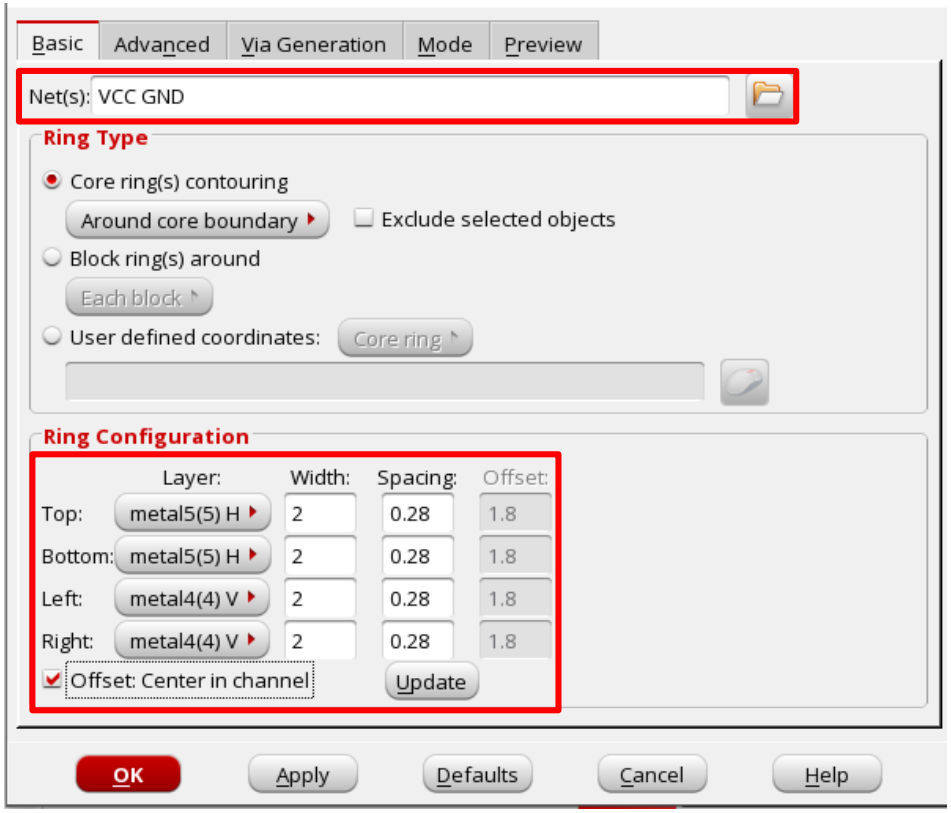
Specify Floorplan (cont.)

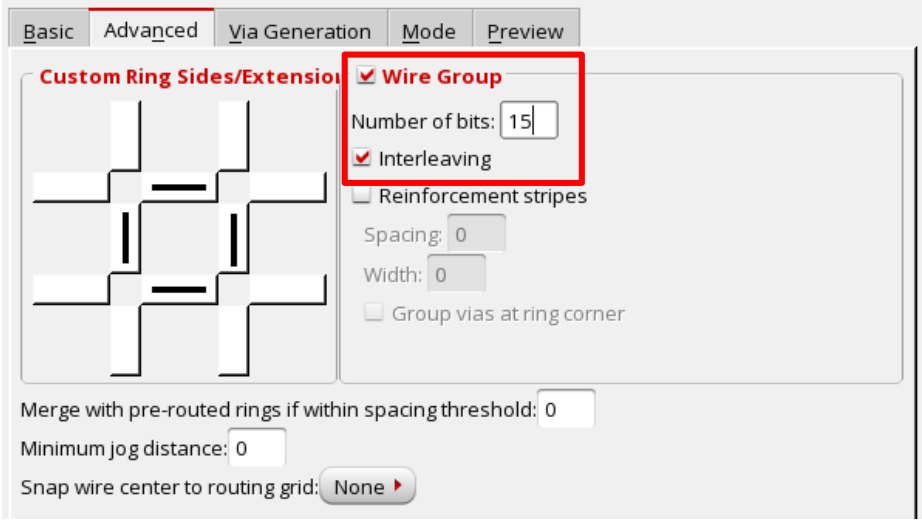


Create Power-ring

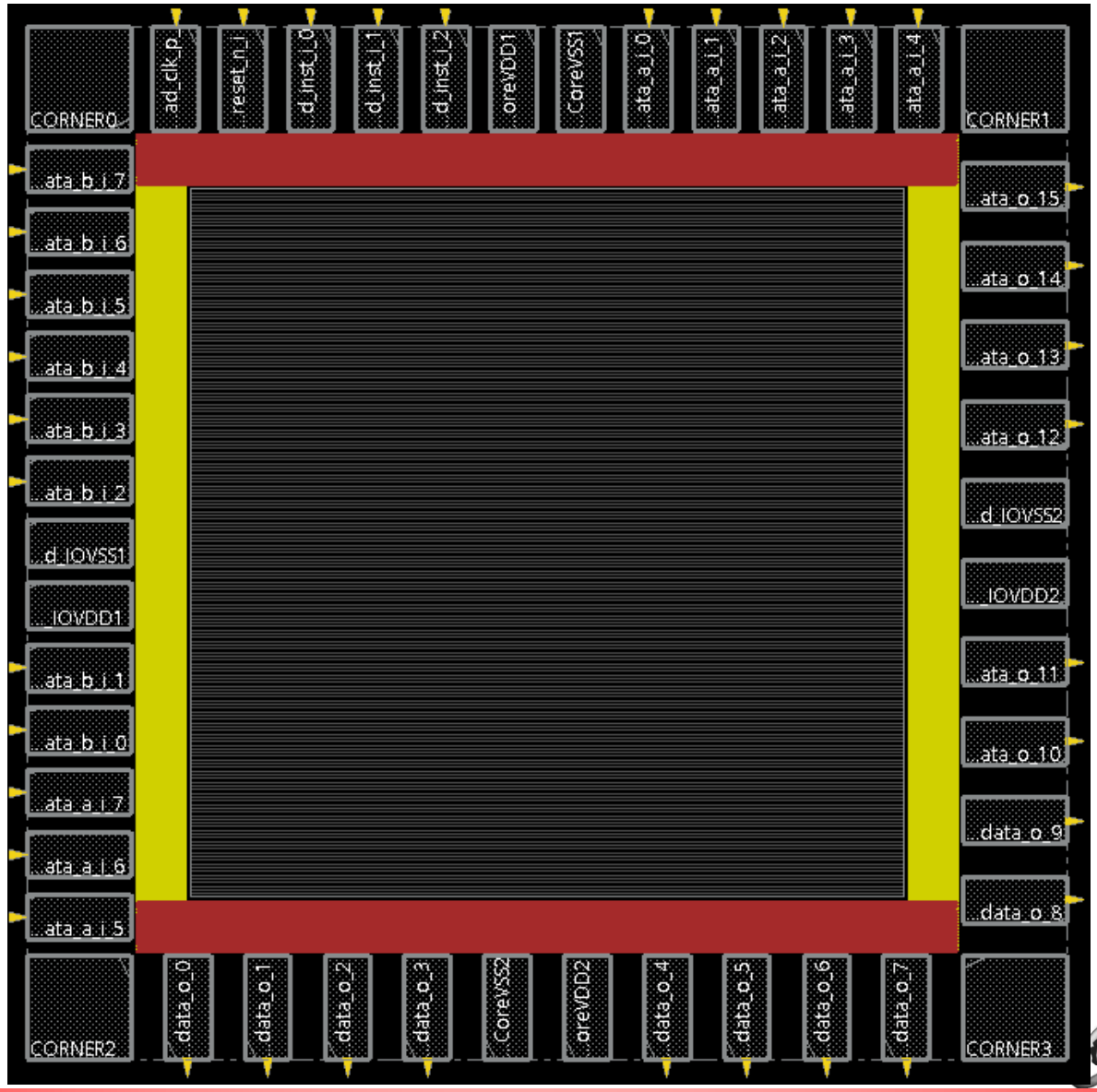
- Power → Power Planning → Add Rings





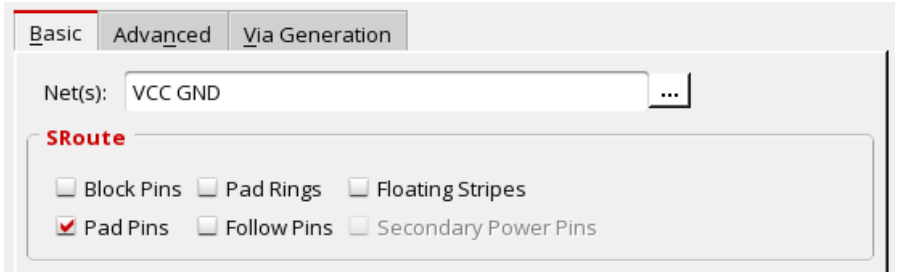


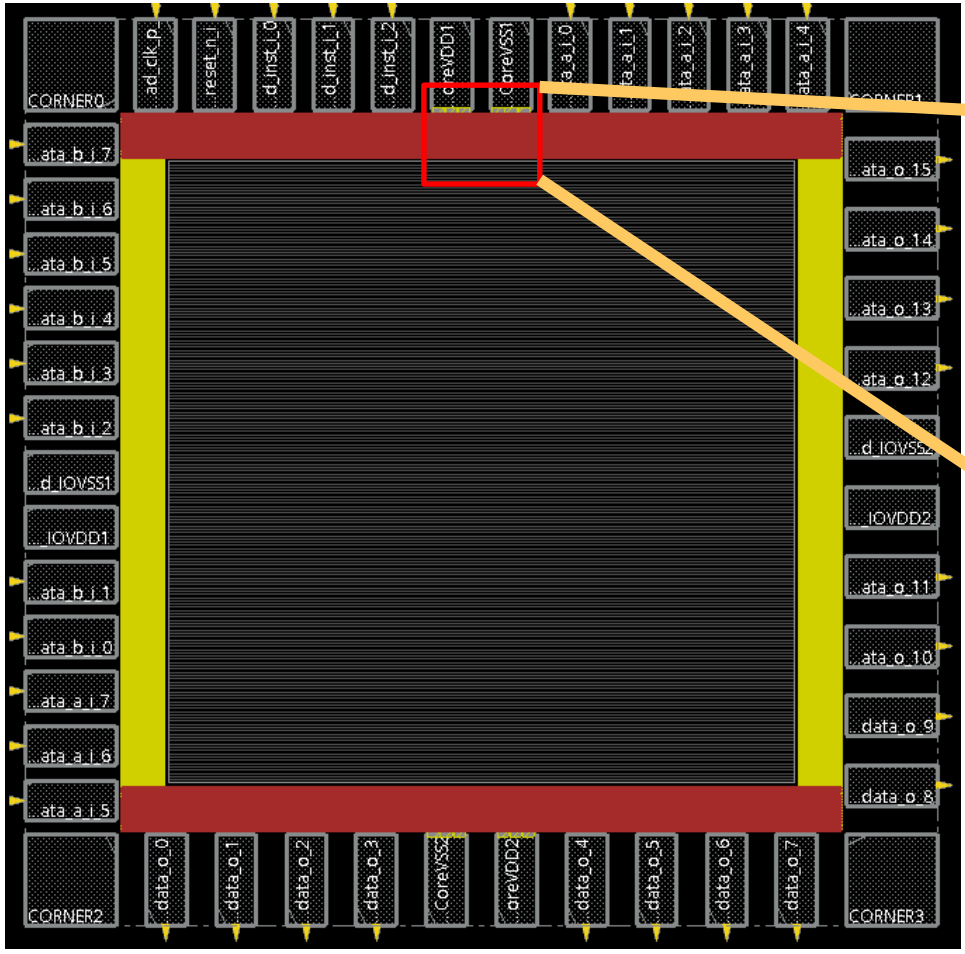
Create Power-ring (cont.)

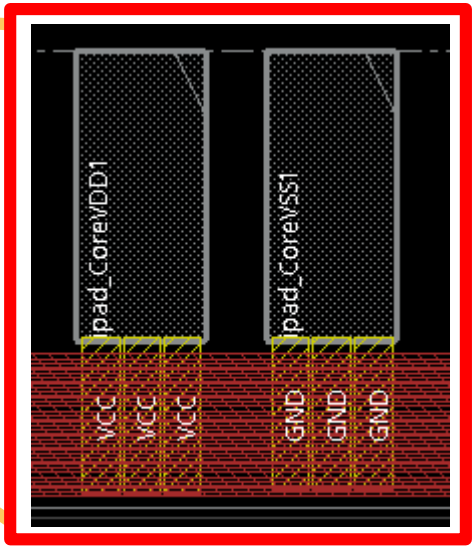


Connect power pad

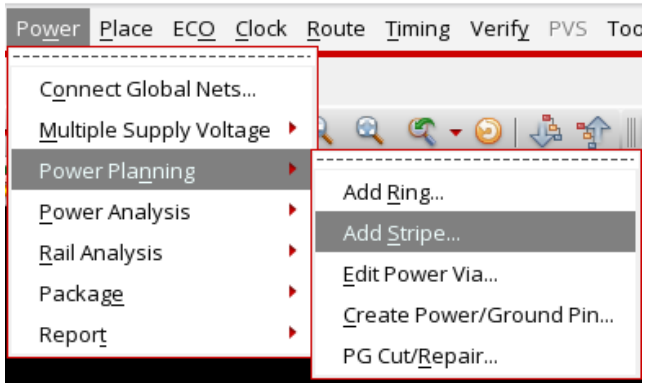
- Route → Special Route



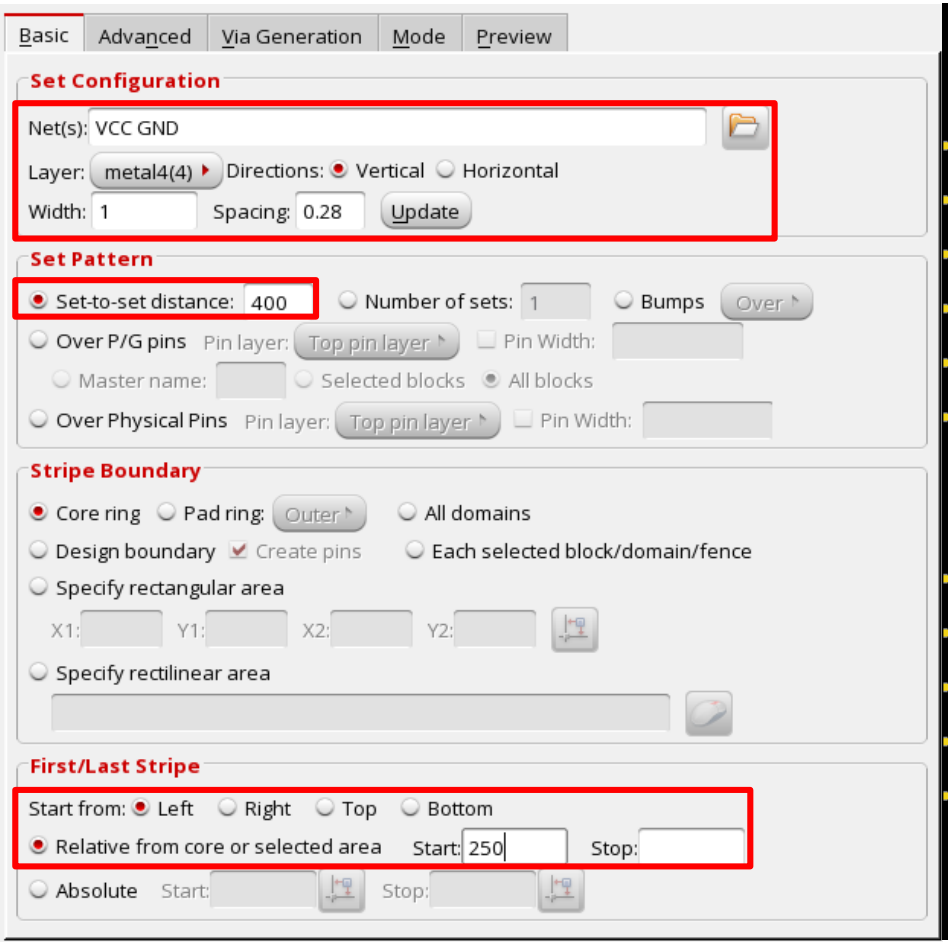


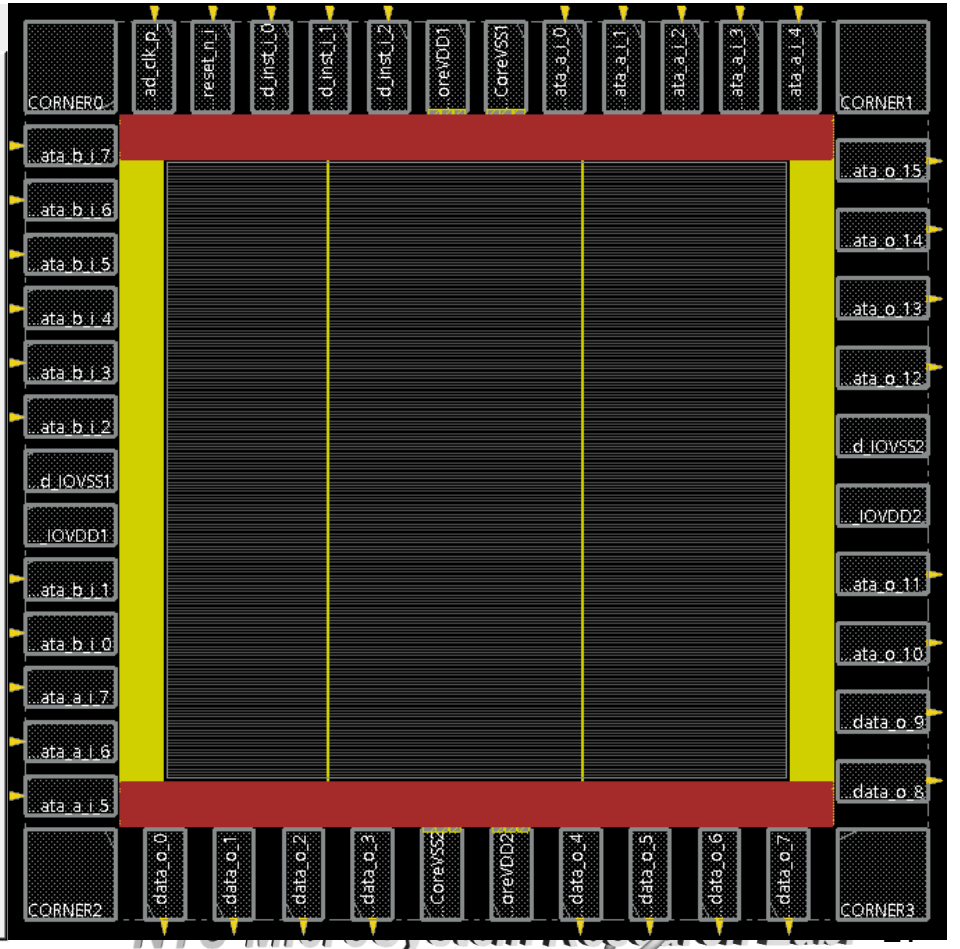


Create Power-stripe



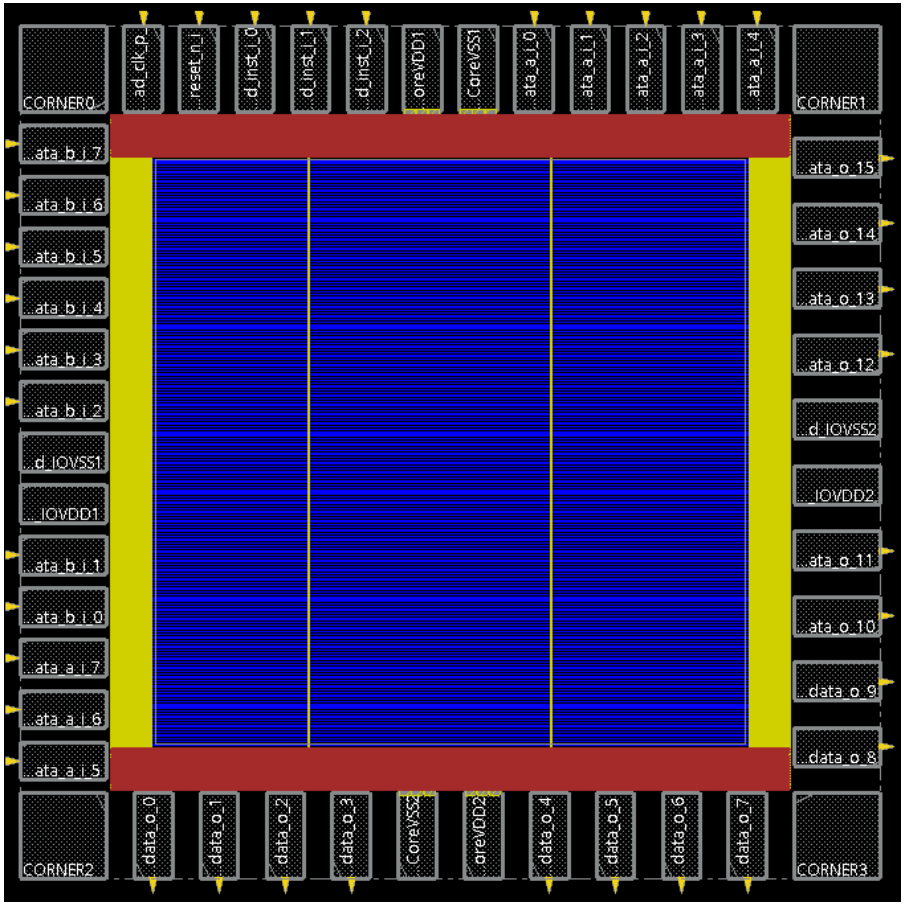
- Power → Power Planning → Add Stripes

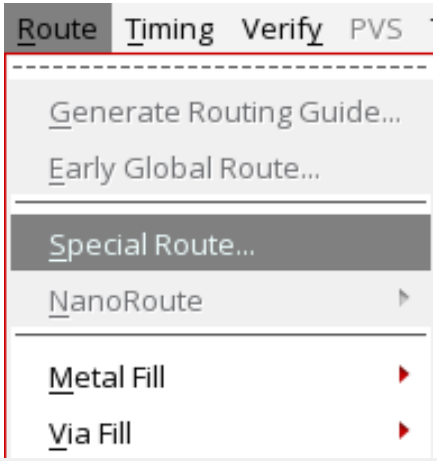


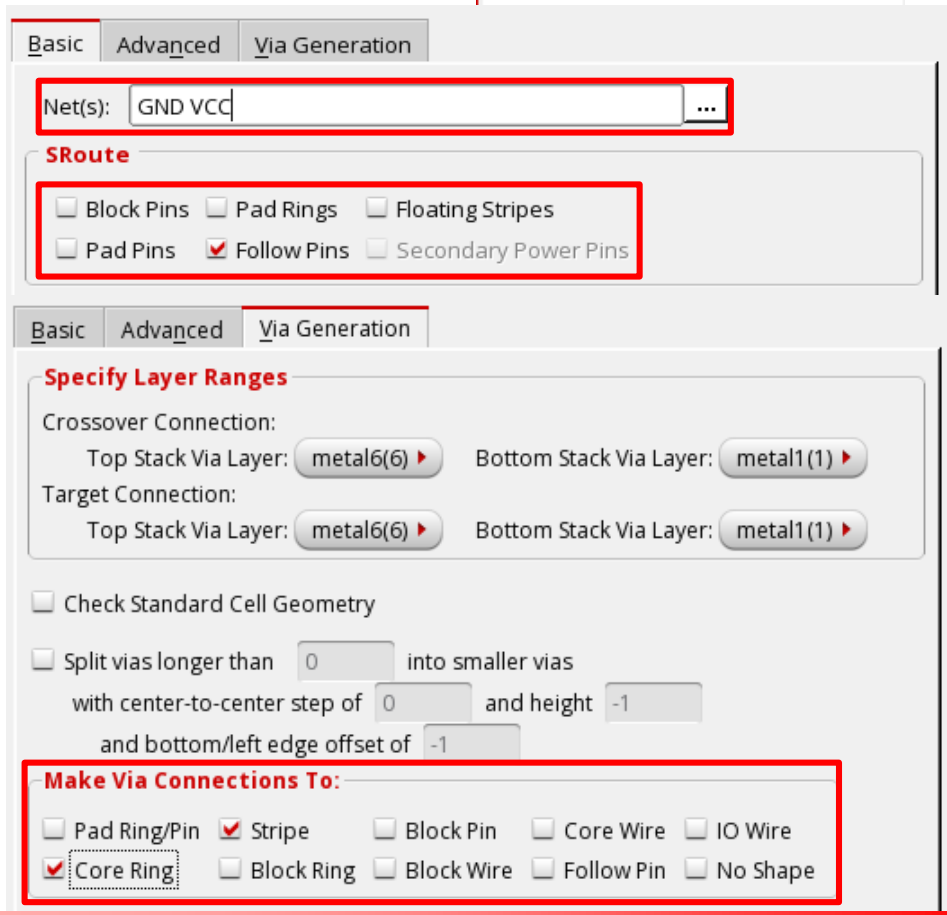


Connect Powerpin

- Route → Special Route



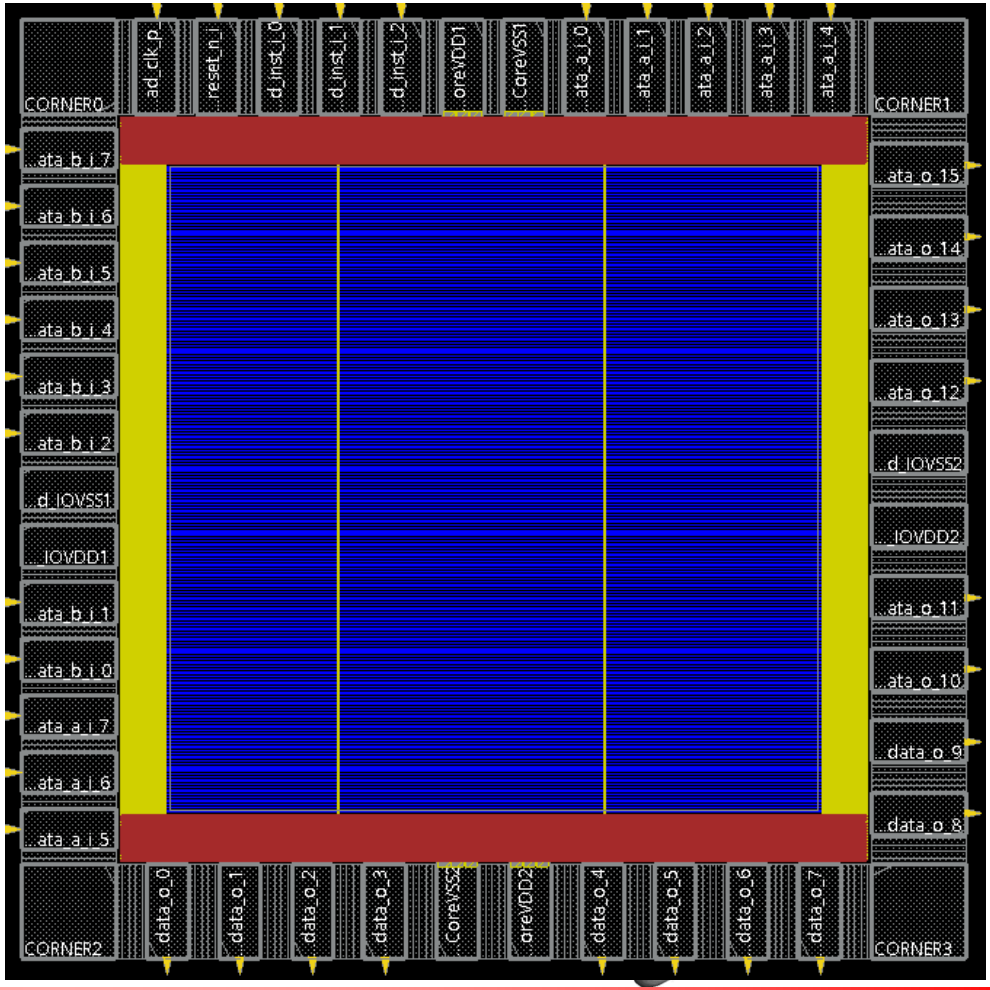




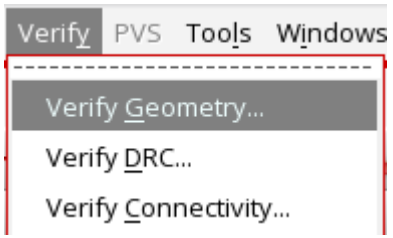
Add IO Filler

- innovus> source addIoFiller.cmd

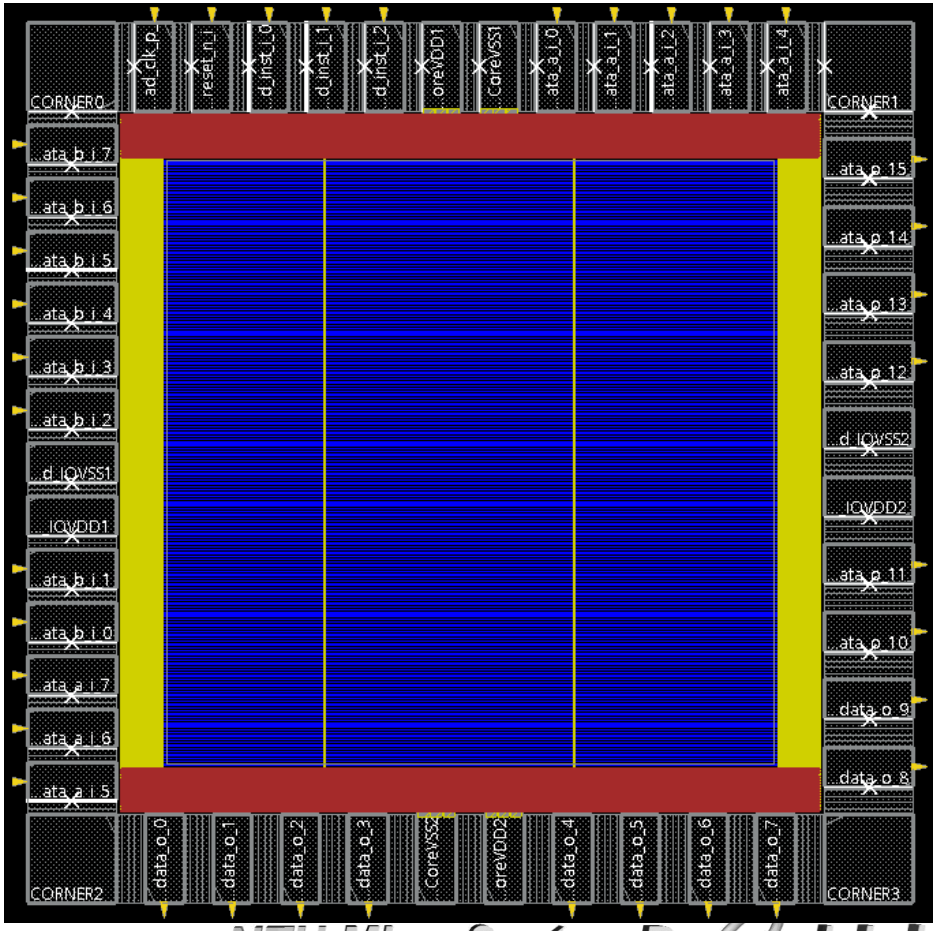
```
innovus 1> source addIoFiller.cmd
Added 13 of filler cell 'EMPTY16D' on top side.
Added 0 of filler cell 'EMPTY16D' on left side.
Added 22 of filler cell 'EMPTY16D' on bottom side.
Added 22 of filler cell 'EMPTY16D' on right side.
Added 13 of filler cell 'EMPTY8D' on top side.
Added 14 of filler cell 'EMPTY8D' on left side.
Added 11 of filler cell 'EMPTY8D' on bottom side.
Added 11 of filler cell 'EMPTY8D' on right side.
Added 0 of filler cell 'EMPTY4D' on top side.
Added 14 of filler cell 'EMPTY4D' on left side.
Added 11 of filler cell 'EMPTY4D' on bottom side.
Added 11 of filler cell 'EMPTY4D' on right side.
Added 0 of filler cell 'EMPTY2D' on top side.
Added 14 of filler cell 'EMPTY2D' on left side.
Added 11 of filler cell 'EMPTY2D' on bottom side.
Added 0 of filler cell 'EMPTY2D' on right side.
Added 13 of filler cell 'EMPTY1D' on top side.
Added 14 of filler cell 'EMPTY1D' on left side.
Added 22 of filler cell 'EMPTY1D' on bottom side.
Added 22 of filler cell 'EMPTY1D' on right side.
```



Check Violation by far

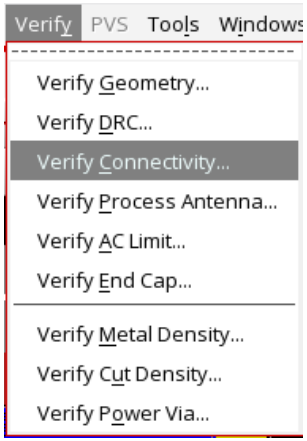


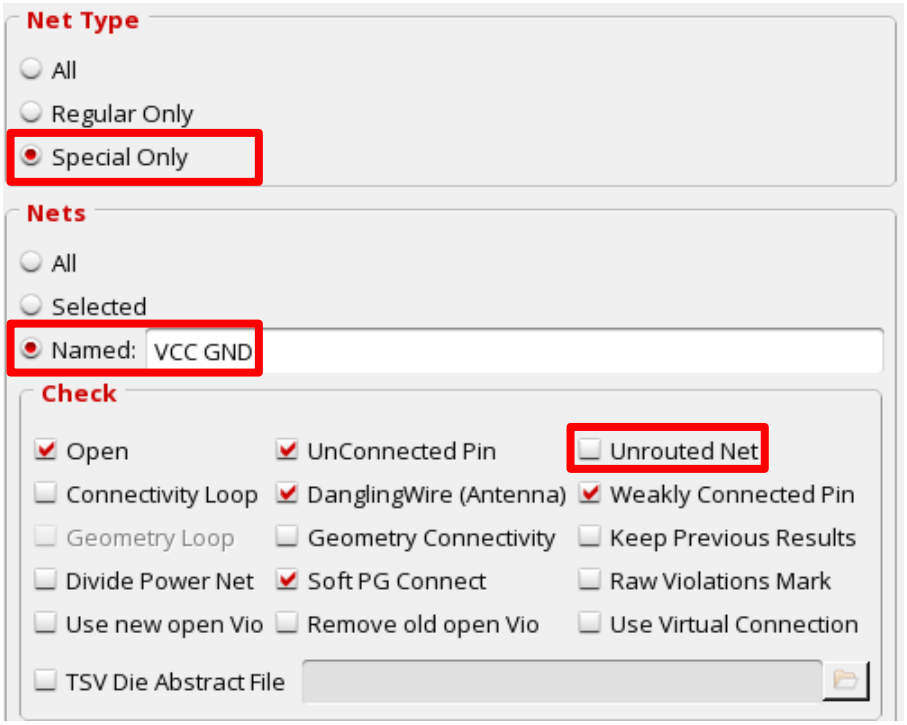
- Verify DRC (ignore xx between pad)



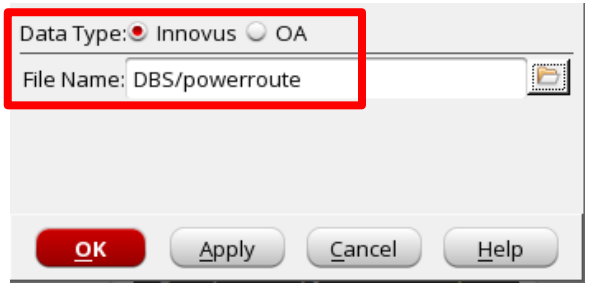
Check Violation by far (cont.)

- Verify Connectivity





- Save your design by now.

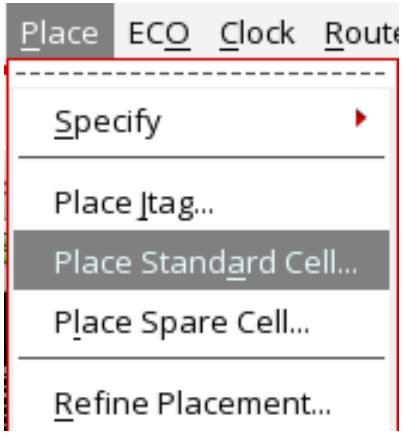


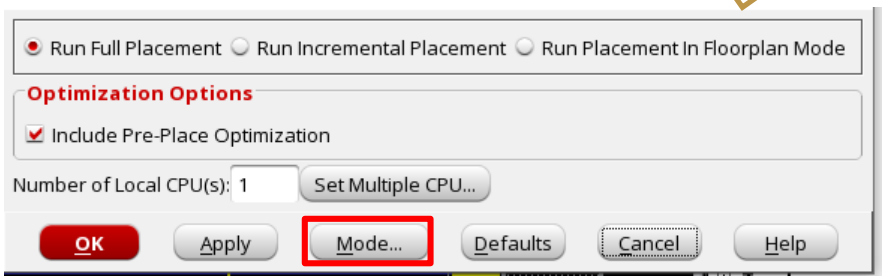
Message shows in terminal.

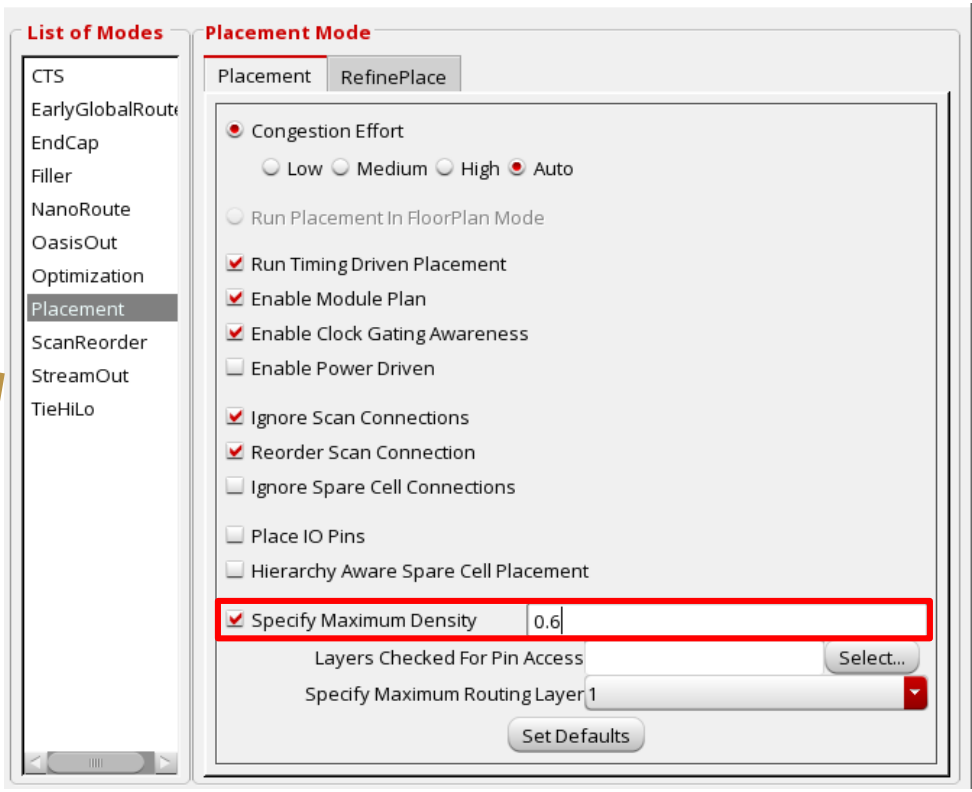
```
Check specified nets
*** Checking Net VCC
*** Checking Net GND

Begin Summary
  Found no problems or warnings.
End Summary
```

Pre-CTS placement

- Place → Place Standard Cells

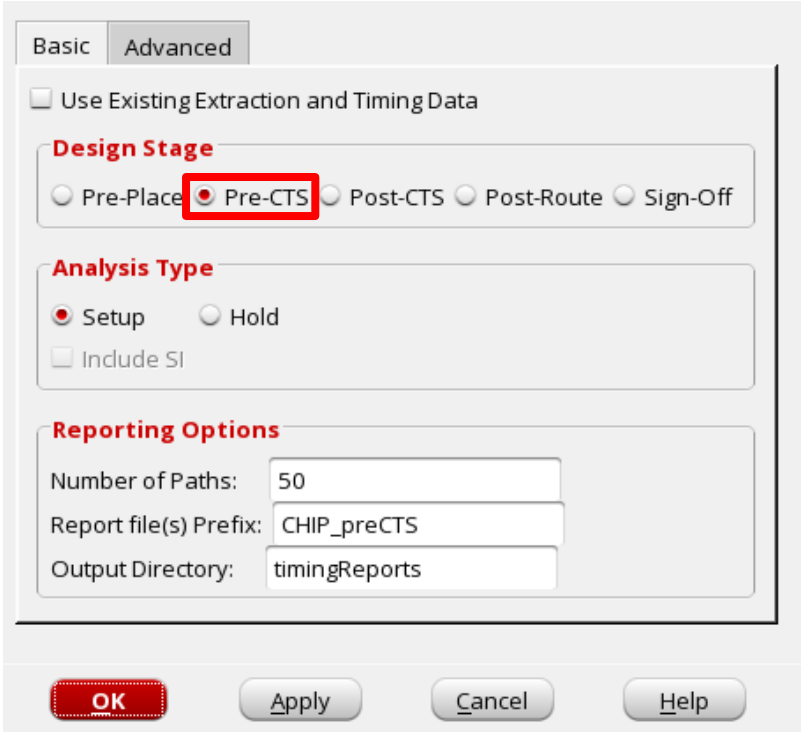






Check Timing

- Timing → Report Timing
- ECO → Optimize Design
  - If WNS is negative or design has violation, try this step

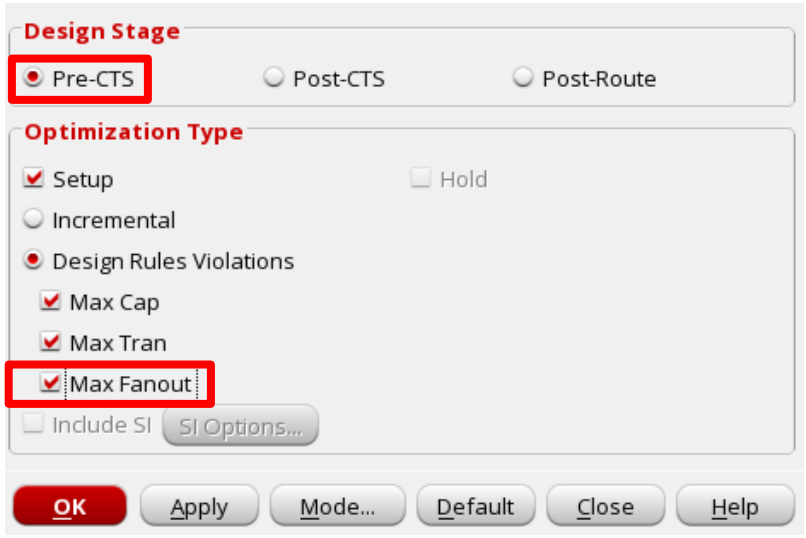


Setup mode	all	reg2reg	default
WNS (ns):	1.270	1.270	6.099
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	70	19	54

DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	1 (1)	-0.745	1 (1)
max_tran	0 (0)	0.000	0 (0)
max_fanout	27 (27)	-121	28 (28)
max_length	0 (0)	0	0 (0)

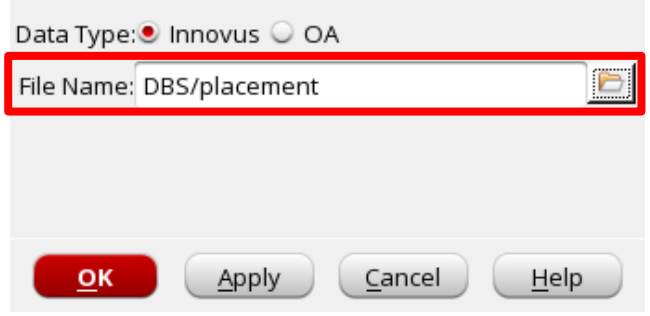
Check Timing (cont.)

- ECO → Optimize Design
  - If WNS is negative or design has violation, try this step




```
------------------------------------------------------------
     optDesign Final Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  1.317  |  1.317  |  5.868  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   70    |   19    |   54    |
+--------------------+---------+---------+---------+

+---------------+-----------------------------+-----------------+
|               |             Real            |      Total      |
|    DRVs       +-----------------+-----------+-----------------|
|               |  Nr nets(terms) | Worst Vio | Nr nets(terms)  |
+---------------+-----------------+-----------+-----------------+
|   max_cap     |      0 (0)      |   0.000   |      0 (0)      |
|   max_tran    |      0 (0)      |   0.000   |      0 (0)      |
|   max_fanout  |      0 (0)      |     0     |      1 (1)      |
|   max_length  |      0 (0)      |     0     |      0 (0)      |
+---------------+-----------------+-----------+-----------------+
```

- Save your design by now.



Clock tree synthesis

- innovus> create_ccopt_clock_tree_spec -file ccopt.spec

```
innovus 2> create_ccopt_clock_tree_spec -file ccopt.spec
Creating clock tree spec for modes (timing configs): func_mode scan_mode
extract_clock_generator_skew_groups=true: create_ccopt_clock_tree_spec will generate skew groups with a name prefix of "_clock_gen" to balance clock generato
r connected flops with the clock generator they drive.
Reset timing graph...
Ignoring AAE DB Resetting ...
Reset timing graph done.
Ignoring AAE DB Resetting ...
Analyzing clock structure...
Analyzing clock structure done.
Reset timing graph...
Ignoring AAE DB Resetting ...
Reset timing graph done.
Wrote: ccopt.spec
```

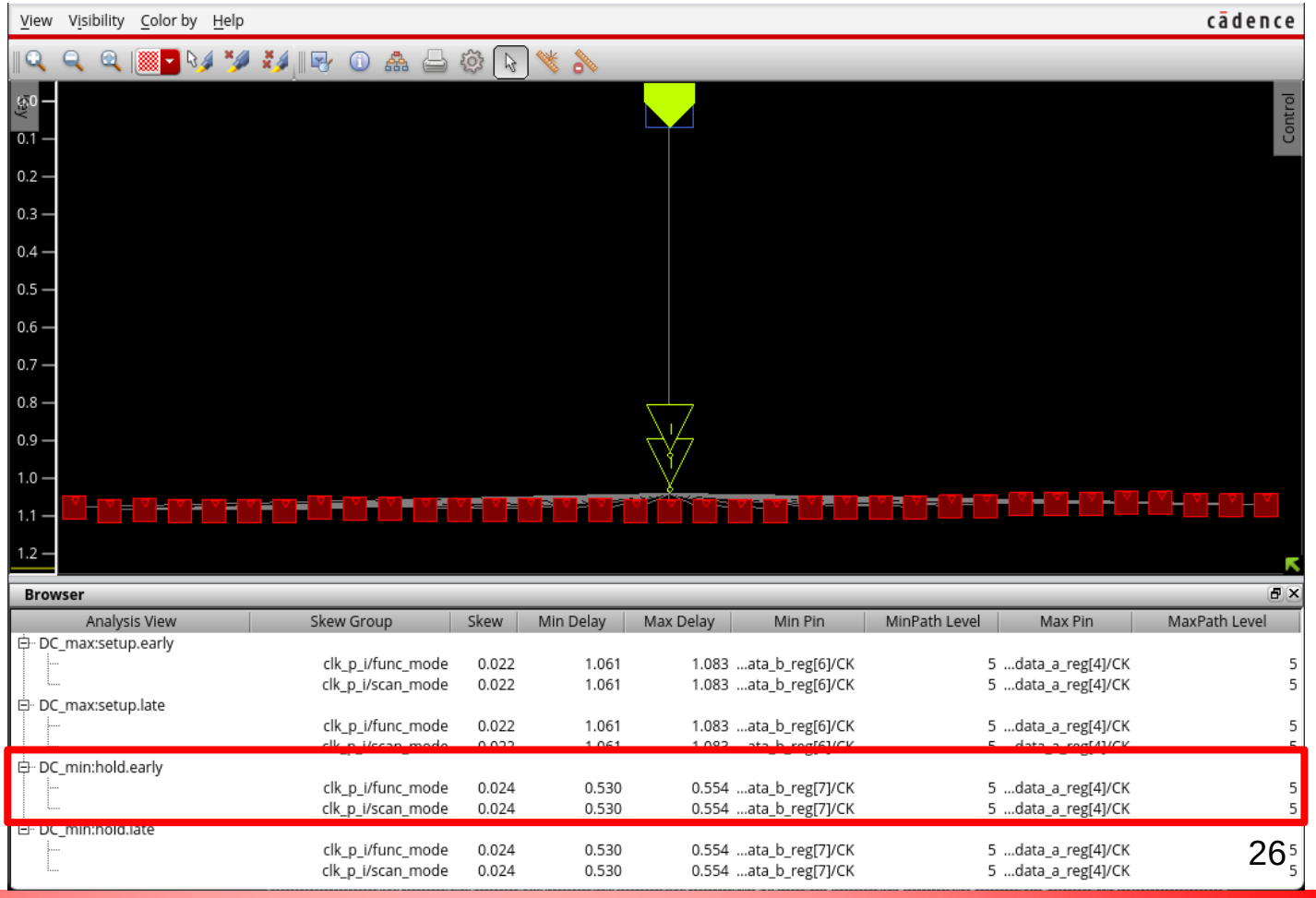
- innovus> source ./ccopt.spec

```
innovus 3> source ./ccopt.spec
Extracting original clock gating for clk_p_i...
  clock_tree clk_p_i contains 35 sinks and 0 clock gates.
  Extraction for clk_p_i complete.
Extracting original clock gating for clk_p_i done.
Checking clock tree convergence...
Checking clock tree convergence done.
```

- innouvs> ccopt_design -cts

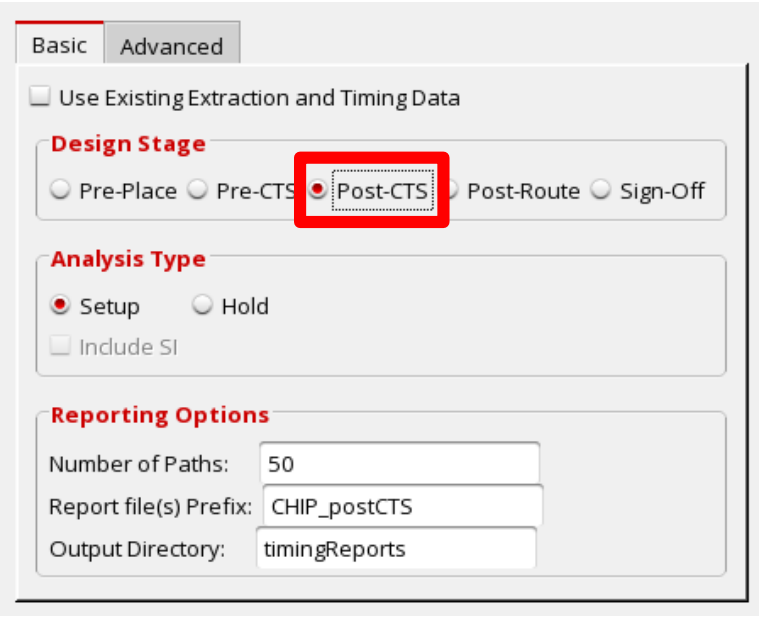
Clock tree synthesis (cont.)

- Clock → CCOpt Clock Tree Debugger
  - Skew
  - Min delay
  - Max delay



Clock tree synthesis (cont.)

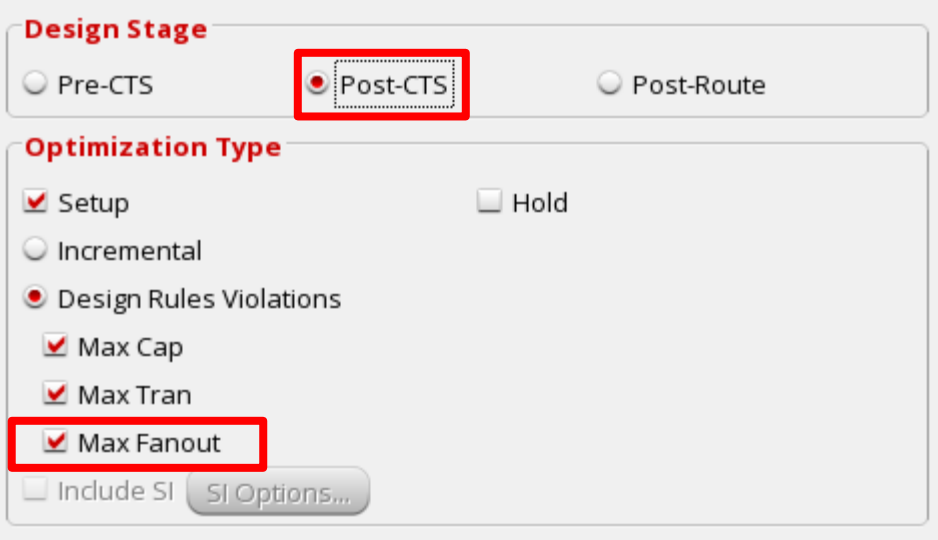
- Do the timing analysis again.
- Timing → Report Timing
  - Design stage is Post-CTS



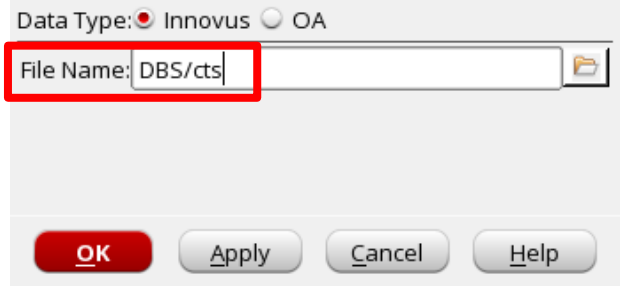

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  1.276  |  1.276  |  5.875  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   70    |   19    |   54    |
+--------------------+---------+---------+---------+

+----------------+--------------------------------+------------------+
|                |              Real              |       Total      |
|    DRVs        +------------------+-------------+------------------|
|                |  Nr nets(terms)  | Worst Vio   |  Nr nets(terms)  |
+----------------+------------------+-------------+------------------+
|   max_cap      |      0 (0)       |   0.000     |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000     |      0 (0)       |
|   max_fanout   |      0 (0)       |     0       |      1 (1)       |
|   max_length   |      0 (0)       |     0       |      0 (0)       |
+----------------+------------------+-------------+------------------+
```

Clock tree synthesis (cont.)

- ECO → Optimize Design
  - If WNS is negative or design has violation, try this step

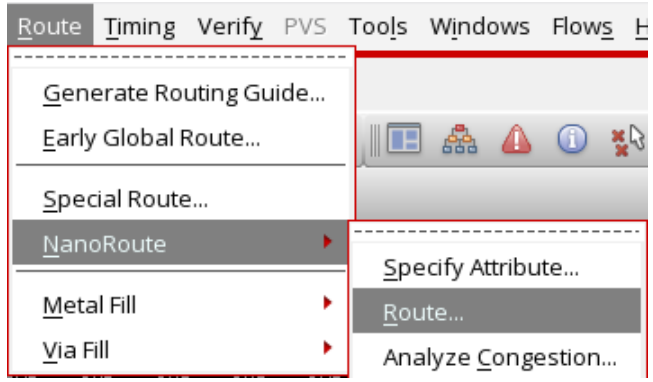


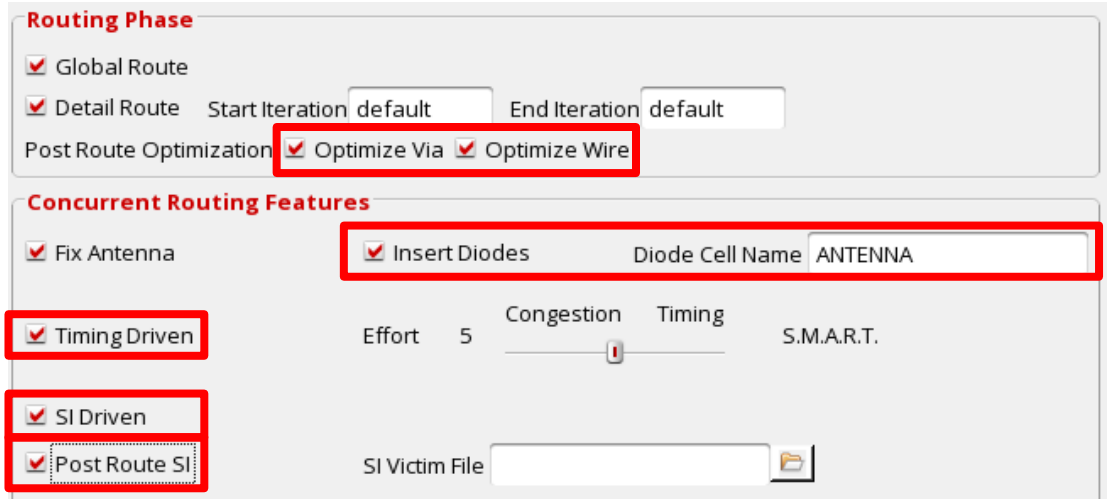
- Save your design by now.



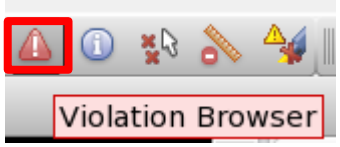
Route

- Route → NanoRoute → Route



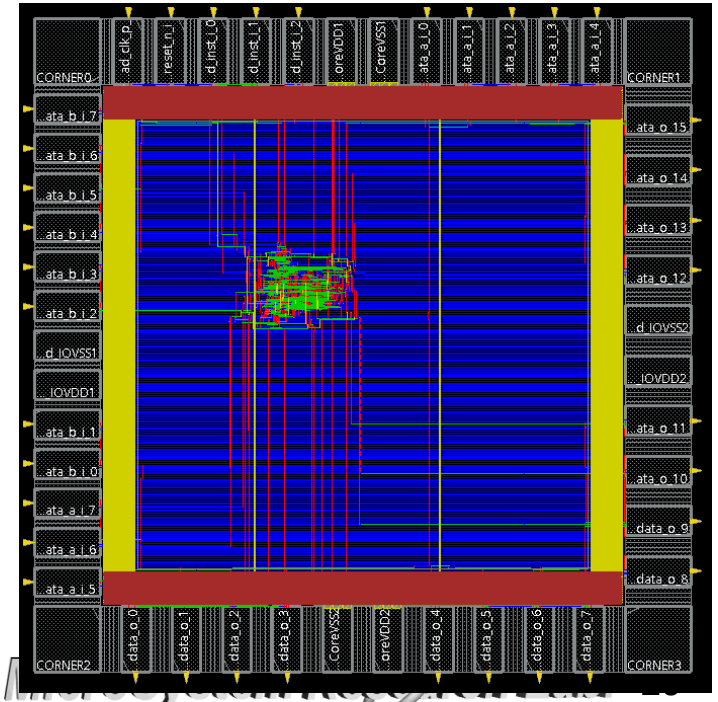


If innovus crashed, then cancel out Timing Driven.



Clear IO filler's overlap violation.

Physical mode



Route (cont.)

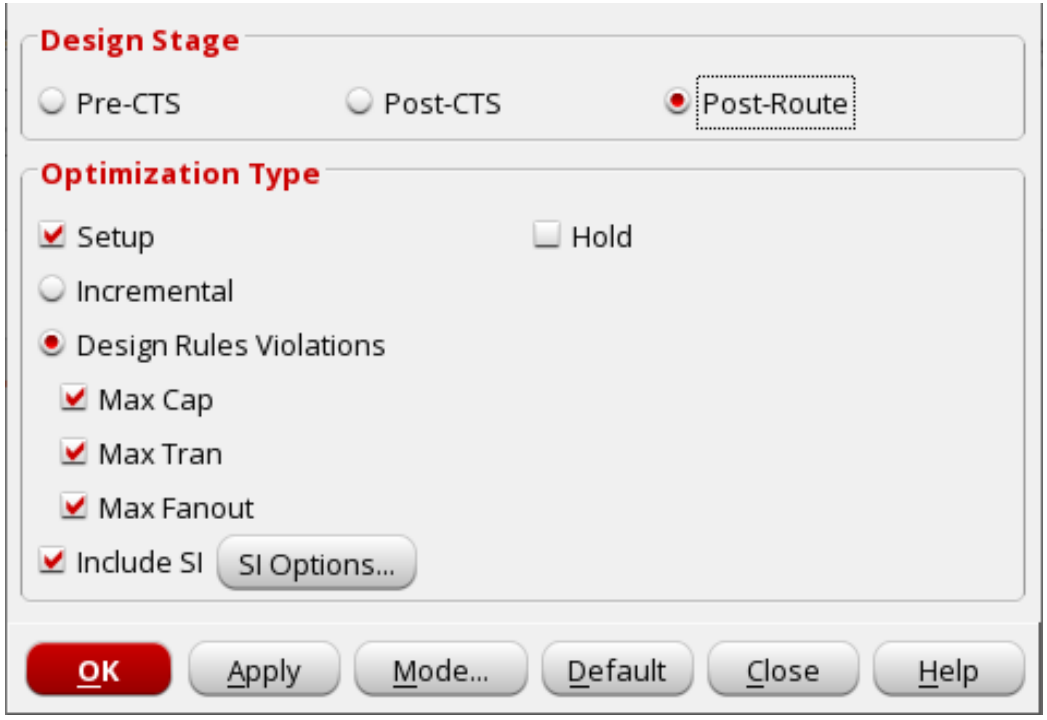
- Since the restriction of Innovus, we need to set Mode before we do the timing analysis.
  - Innovus > setAnalysisMode -analysisType onChipVariation
- Timing → Report Timing (Check setup and hold)

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  1.922  |  1.922  |  6.422  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   70    |   19    |   54    |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      1 (1)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+
```

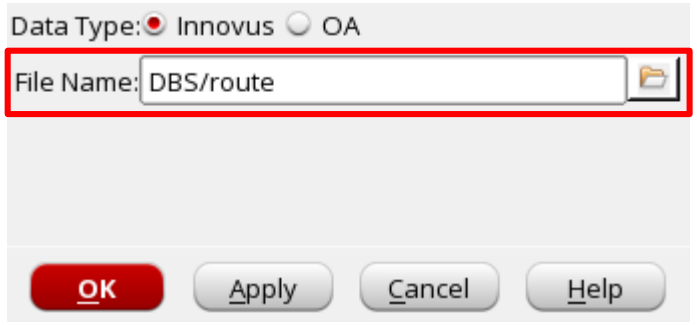
```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 av_func_mode_min av_scan_mode_min

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.225  |  0.225  |  1.701  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   35    |   19    |   16    |
+--------------------+---------+---------+---------+
```

Route (cont.)

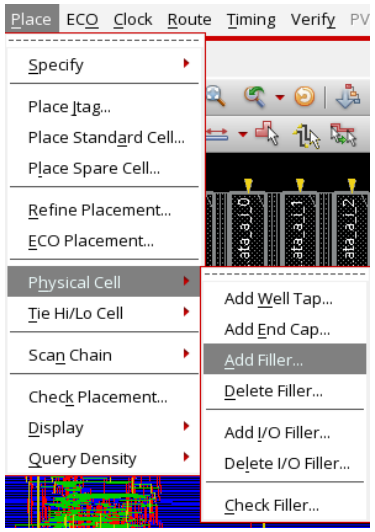
- ECO → Optimize Design
  - If WNS or max_fanout is negative, try this step



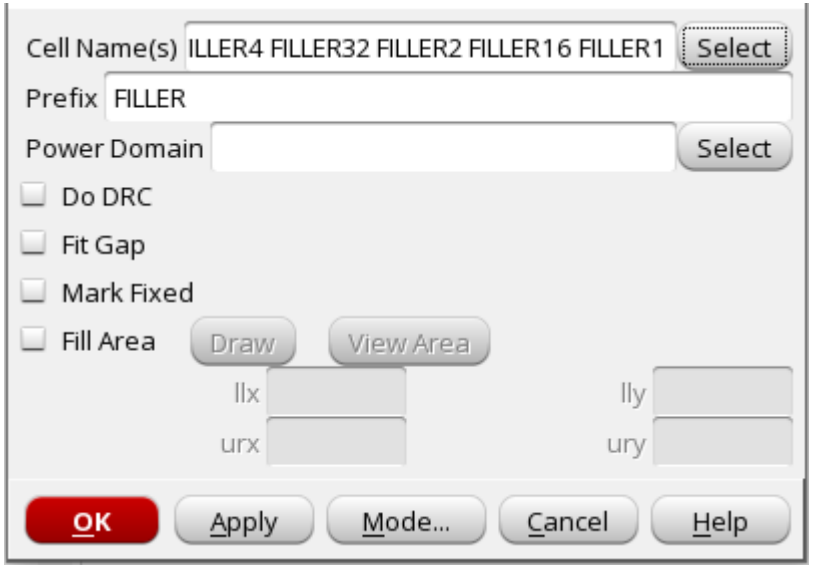
- Save your design by now.

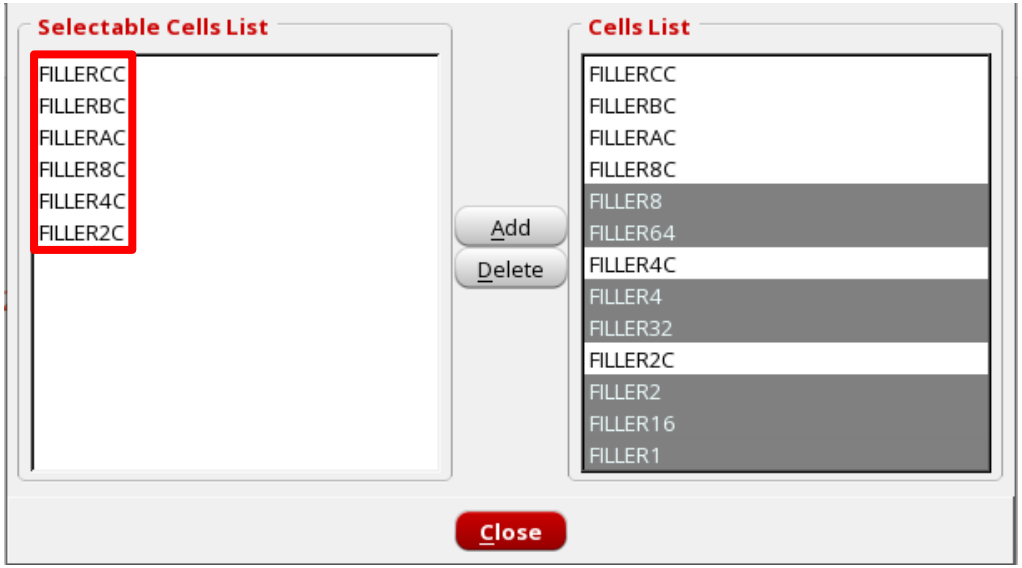


Add Core Filler

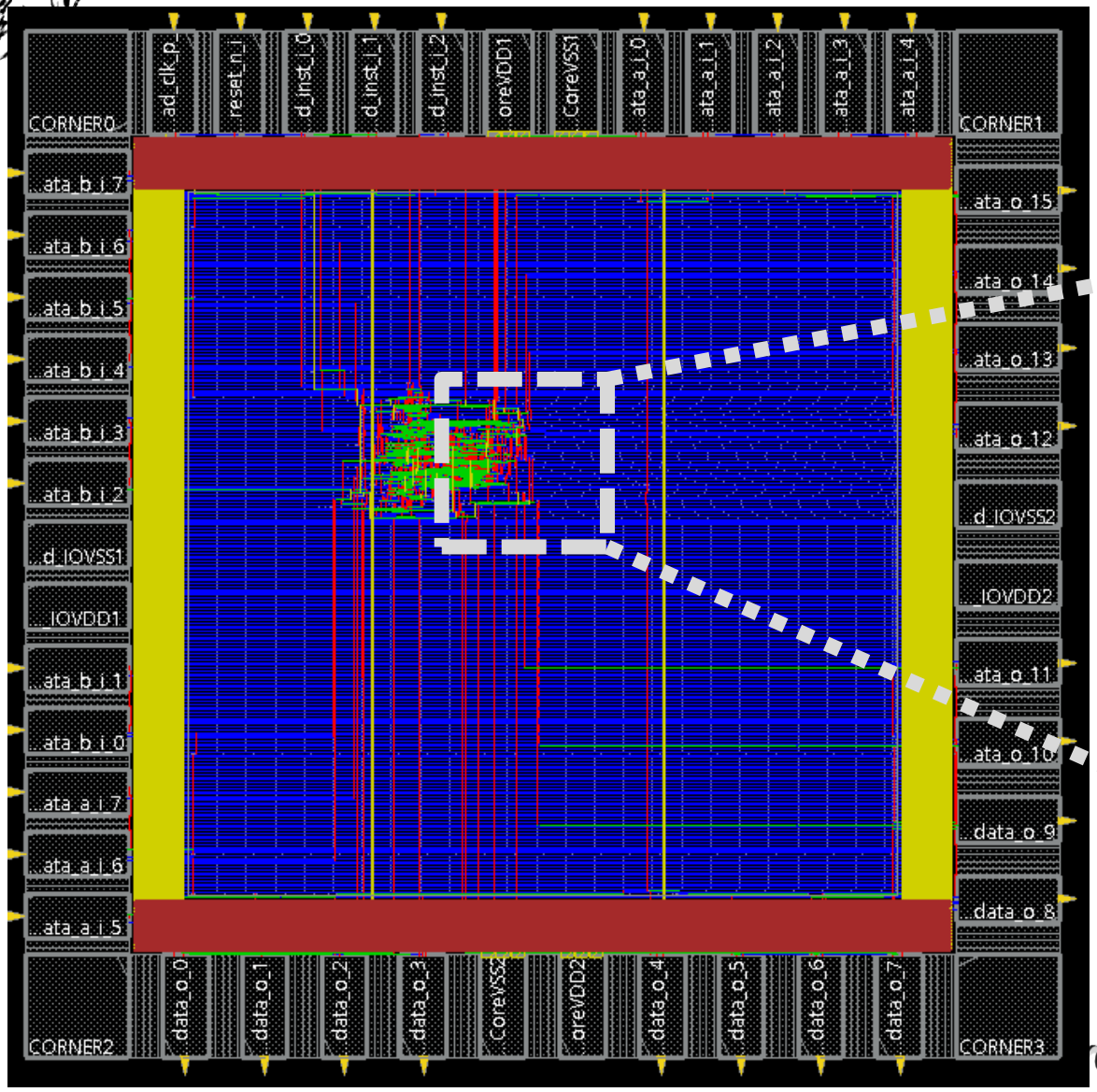


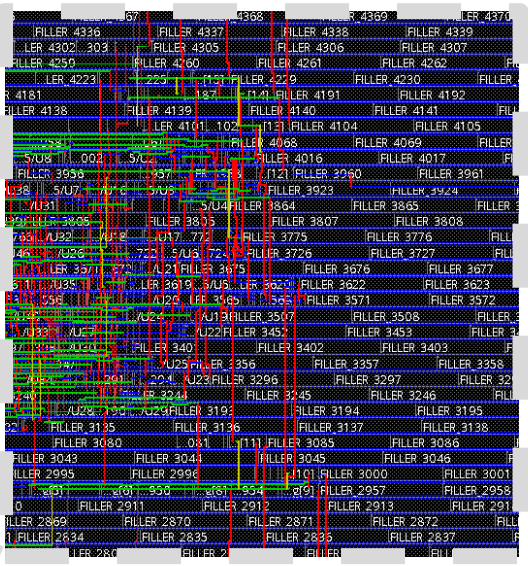
- Place → Physical Cells → Add Filler
- 有C的先載入





Add Core Filler (cont.)



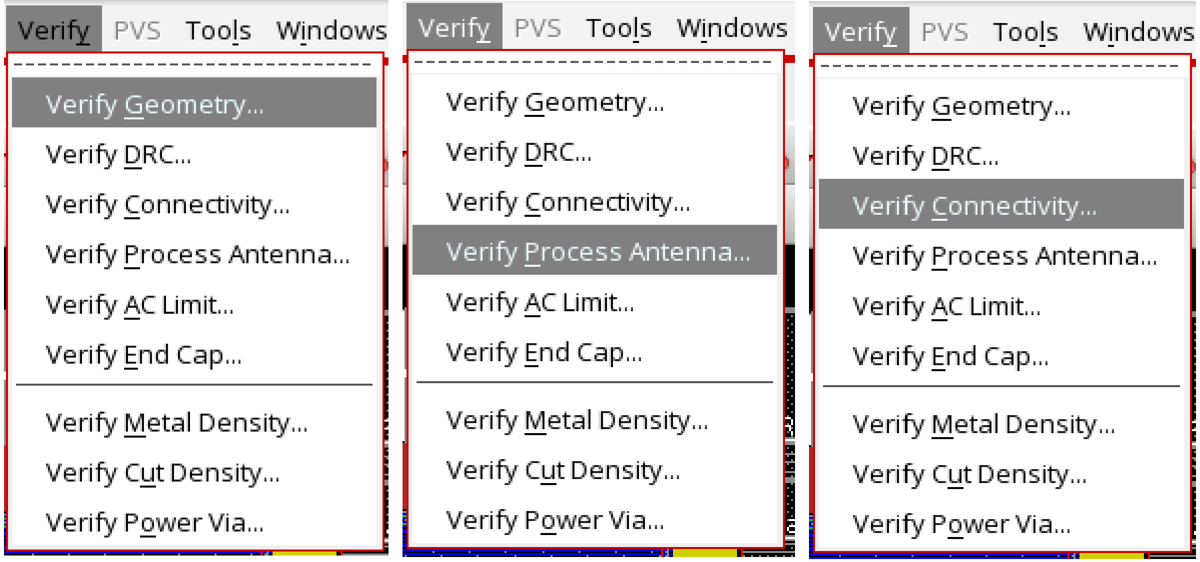


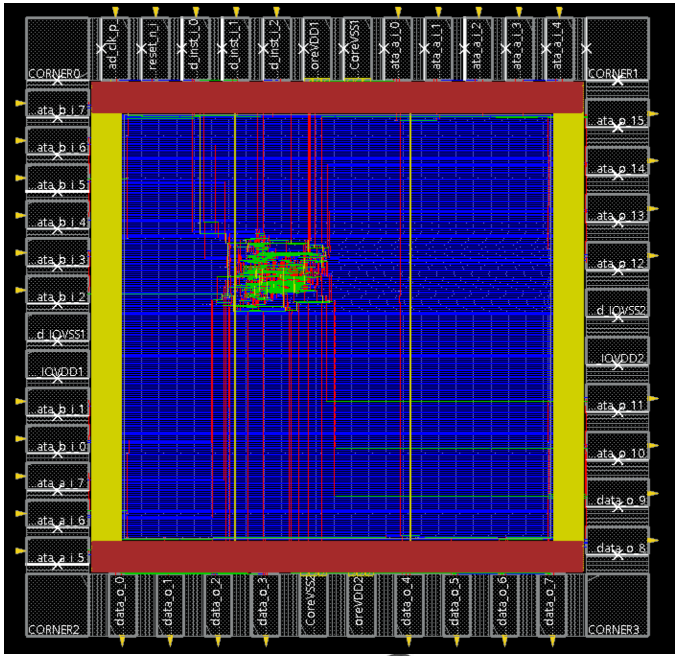
Verify

```
******* START VERIFY ANTENNA ********
Report File: CHIP.antenna.rpt
LEF Macro File: CHIP.antenna.lef
Verification Complete: 0 Violations
******* DONE VERIFY ANTENNA ********
```

```
Check specified nets
*** Checking Net VCC
*** Checking Net GND

Begin Summary
  Found no problems or warnings.
End Summary
```

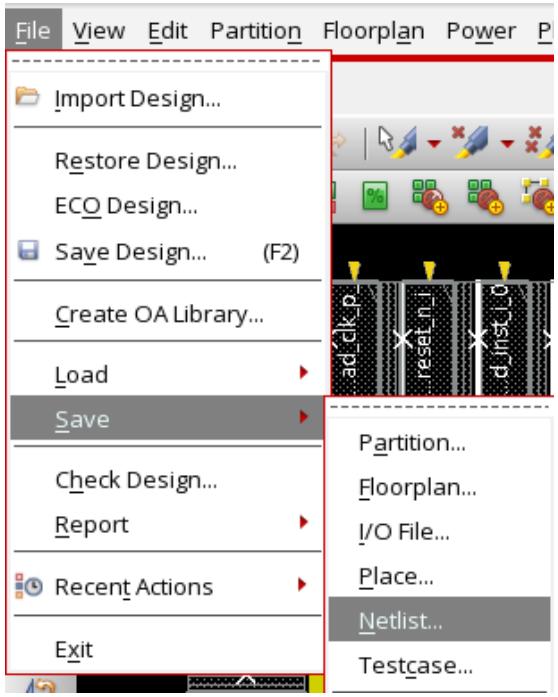
- Verify → Verify Geometry
- Verify → Verify Process Antenna
- Verify → Verify Connectivity



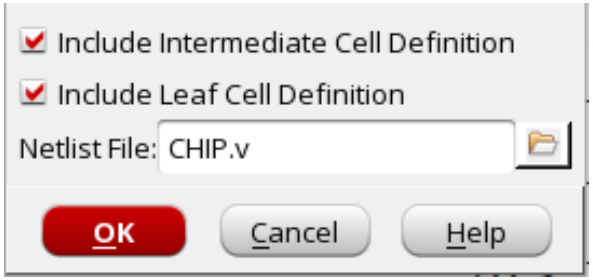


- Save your design by now.
  - DBS/corefiller

Write .v and .sdf



- File → Save →Netlist…, Netlist File填CHIP.v



- innovus > setAnalysisMode -analysisType bcwc
- innovus > write_sdf -max_view av_func_mode_max -min_view av_func_mode_min -edges noedge -splitsetuphold -remashold -splitrecrem -min_period_edges none CHIP.sdf

Posim

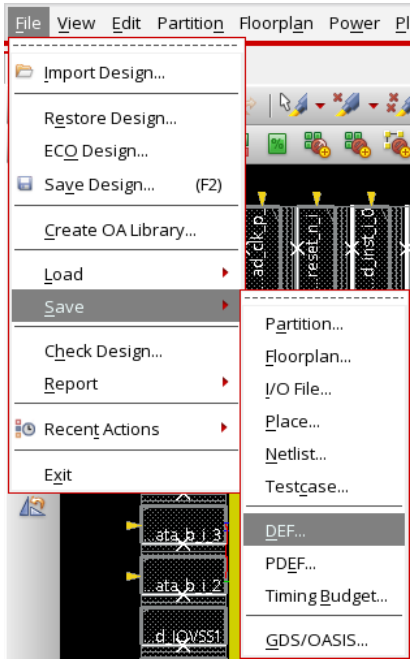
- > vcs HW3_alu_tb.v CHIP.v -v fsa0m_a_generic_core_21.lib.src fsa0m_a_t33_generic_io_21.lib.src –full64 –R -debug_access+all +v2k +define+SDF

Add bonding pad

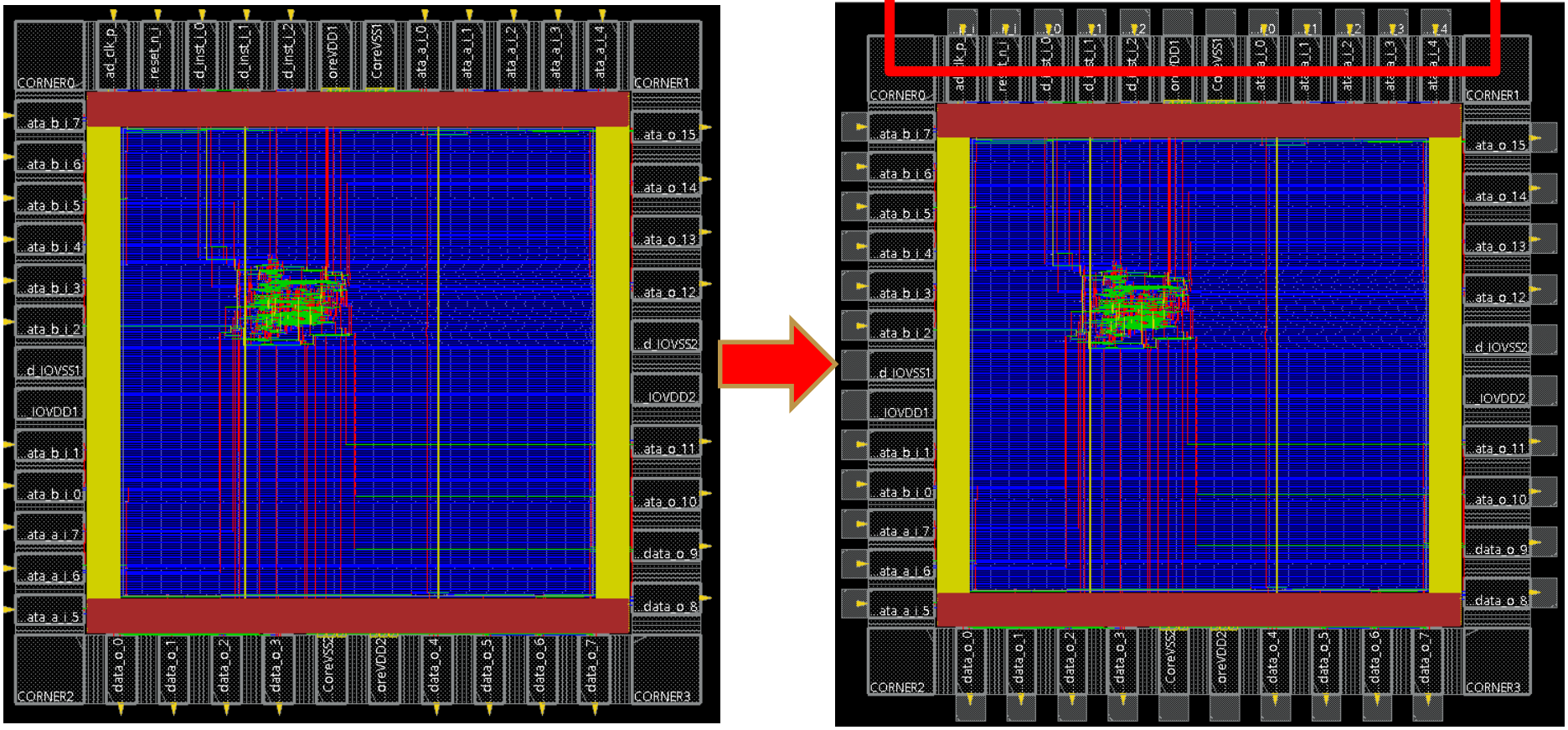
- File → Save → DEF …
  - Select Save Scan, File Name should be CHIP.def
- In Unix terminal
  - > perl addbonding_v3.8D.pl CHIP.def

```
[r11013@cad27 Lab4]$ perl addbonding_v3.8D.pl CHIP.def
Use of comma-less variable list is deprecated at addbonding_v3.8D.pl line 617.
Use of comma-less variable list is deprecated at addbonding_v3.8D.pl line 617.
Use of comma-less variable list is deprecated at addbonding_v3.8D.pl line 617.
Use of comma-less variable list is deprecated at addbonding_v3.8D.pl line 617.
Use of comma-less variable list is deprecated at addbonding_v3.8D.pl line 617.
Use of comma-less variable list is deprecated at addbonding_v3.8D.pl line 617.

==== create SOCE cmd for add bonding pad ====
  -- complete, To add bonding cell, execute commnad below in SOC Encounter terminal

     Encounter> source addbond.cmd

==== create Bonding XY file: CHIP.bondinfo ====
  -- complete
==== create SOCE cmd for add routing blockage on IO Pad ====
  -- complete, to add blockage, execute command below in SOC Encounter terminal:

     Encounter> source addbond.cmd
```

- In innovus terminal
  - Innovus > source addbond.cmd



Add bonding pad (cont.)



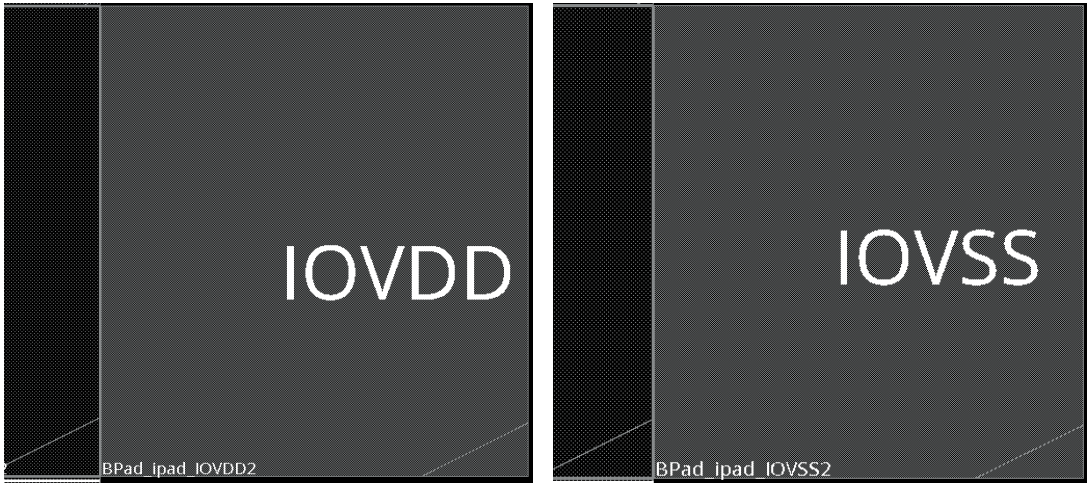
Power label

- 為了在LVS驗證與posim extraction時可以找到IO power的位置，要在export GDS之間在IO power pad外加上power label，預計輸入的位置在右下角的IO power pad及IO ground pad外的bounding pad上
- 注意：label一定要打在pad上面才有效

Power label

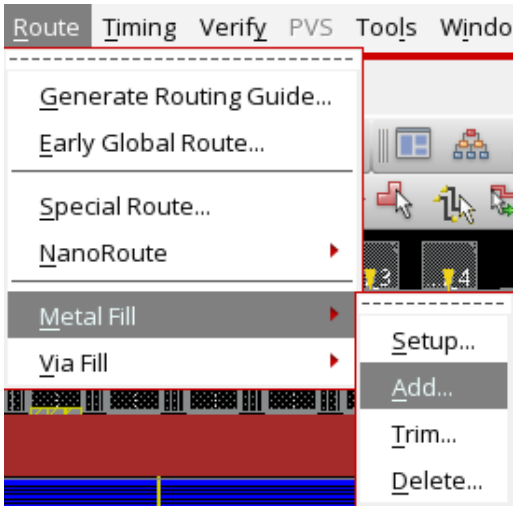
- Type below commands in innovus
  - innovus > add_text -layer metal5 -pt 1435 640 -label IOVDD -height 10
  - innovus > add_text -layer metal5 -pt 1435 750 -label IOVSS -height 10

```
innovus 1> add_text -layer metal5 -pt 1435 640 -label IOVDD -height 10
0x7f283d59e4f0
innovus 2> add_text -layer metal5 -pt 1435 750 -label IOVSS -height 10
0x7f283d59e528
```



- Save your design by now.
  - DBS/finish

Add dummy metal



- Route → Metal Fill → Add

Number of Local CPU(s): 1 Set Multiple CPU...

Iteration Name List:

Model Selection

Shape: Rectangle Square

Connection: Tie High/Low to Net(s): GND VCC

Connection Shape: Tree Mesh

Keep Unconnected Metal Fill(s)

Square Shape

Use Generated Vias Only

Exclude Vias and Via Rules:

Snap to User Grid Stagger On Off Diag

Allow Fill on Cells Ignore Macro Density Table

Incremental Control

Delete Metal Fill before Creating New Metal Fill

FillWire FillWireOPC

Layer Selection

metal1(1) metal2(2) metal3(3) metal4(4) metal5(5) metal6(6)

Timing Aware

Critical Nets from Timing Analysis

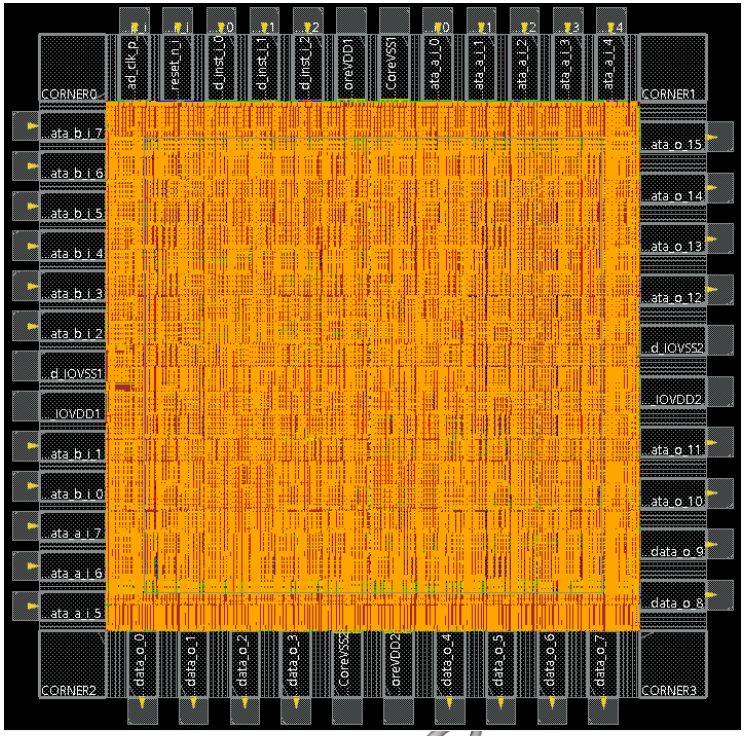
Slack Threshold: 0.2

Area

X1: 0.000 Y1: 0.000

X2: 0.000 Y2: 0.000

OK Apply Defaults Cancel Help



Stream out GDS

- innovus > setStreamOutMode -specifyViaName default -SEvianames false -virtualConnection false -uniquifyCellNamesPrefix false -snapToMGrid false -textSize 1 -version 3
- innovus > streamOut CHIP.gds -mapFile streamOut.map -merge { ./Phantom/fsa0m_a_generic_core_cic.gds ./Phantom/fsa0m_a_t33_generic_io_cic.gds ./Phantom/BONDPAD.gds} -stripes 1 -units 1000 -mode ALL

```
Merging GDS file ./Phantom/fsa0m_a_t33_generic_io_cic.gds ......
        ****** Merge file: ./Phantom/fsa0m_a_t33_generic_io_cic.gds has version number: 5.
        ****** Merge file: ./Phantom/fsa0m_a_t33_generic_io_cic.gds has units: 1000 per micron.
        ****** unit scaling factor = 1 ******
Merging GDS file ./Phantom/BONDPAD.gds ......
        ****** Merge file: ./Phantom/BONDPAD.gds has version number: 5.
        ****** Merge file: ./Phantom/BONDPAD.gds has units: 1000 per micron.
        ****** unit scaling factor = 1 ******
######Streamout is finished!
```