Lab2: Testbench

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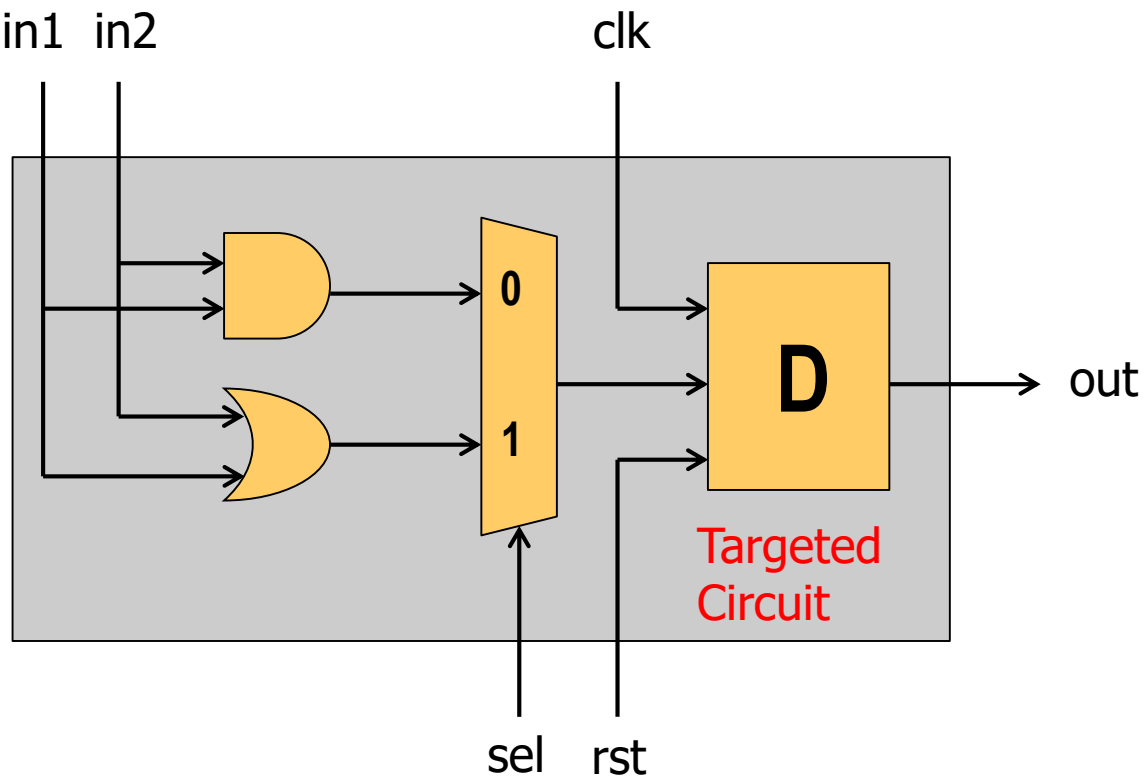
Derived from slides by Bo-Yi Chang

design.v (with 1 error)

```
module IClab(clk,rst,in1,in2,sel,out);
input clk, rst, sel, in1, in2;
output out;
reg out_r;
reg out_w;
assign out=out_r;

always@(*) begin
  if(sel)
    out_w=in1 & in2;
  else
    out_w=in1 ^ in2;
end

always@(posedge clk) begin
  if(~rst)
    out_r<=1'b0;
  else
    out_r<=out_w;
end
endmodule
```



design_tb.v

```
`timescale 1ns/10ps
module tb();
reg clk, rst, in1, in2, sel;
wire out;
initial begin
  $fsdbDumpfile ("iclab.fsdb");
  $fsdbDumpvars (0, "+mda");
  clk=1'b0;
  rst=1'b1;
  in1=1'b0;
  in2=1'b0;
  sel=1'b0;
  #1 rst=1'b0;
  #5 rst=1'b1;
  #4 in1=1'b1; in2=1'b0;
  #10 sel=1'b1;
  #10 sel=1'b0; in1=1'b0;in2=1'b1;
  #10 sel=1'b1;
  #10 sel=1'b0; in1=1'b1;in2=1'b0;
  #10 sel=1'b1;
  #10 sel=1'b0;in1=1'b0;in2=1'b0;
  #10 sel=1'b1;
  #10 $finish;
end

always begin
  #5 clk=~clk;
end

IClab I1(clk,rst,sel,in1,in2,out);
endmodule
```

```
$dumpfile("iclab.vcd");
$dumpvars;
//$fsdbDumpfile("iclab.fsdb");
//$fsdbDumpvars;
```

Compilation

- Put design.v and design_tb.v in the same folder.


```
[r11013@cad27 ~/ICD_lab]$ cd Lab2
[r11013@cad27 Lab2]$ ls
design_tb.v  design.v
[r11013@cad27 Lab2]$
```

Compilation

- vcs design_tb.v design.v –full64 –R –debug_access+all +v2k

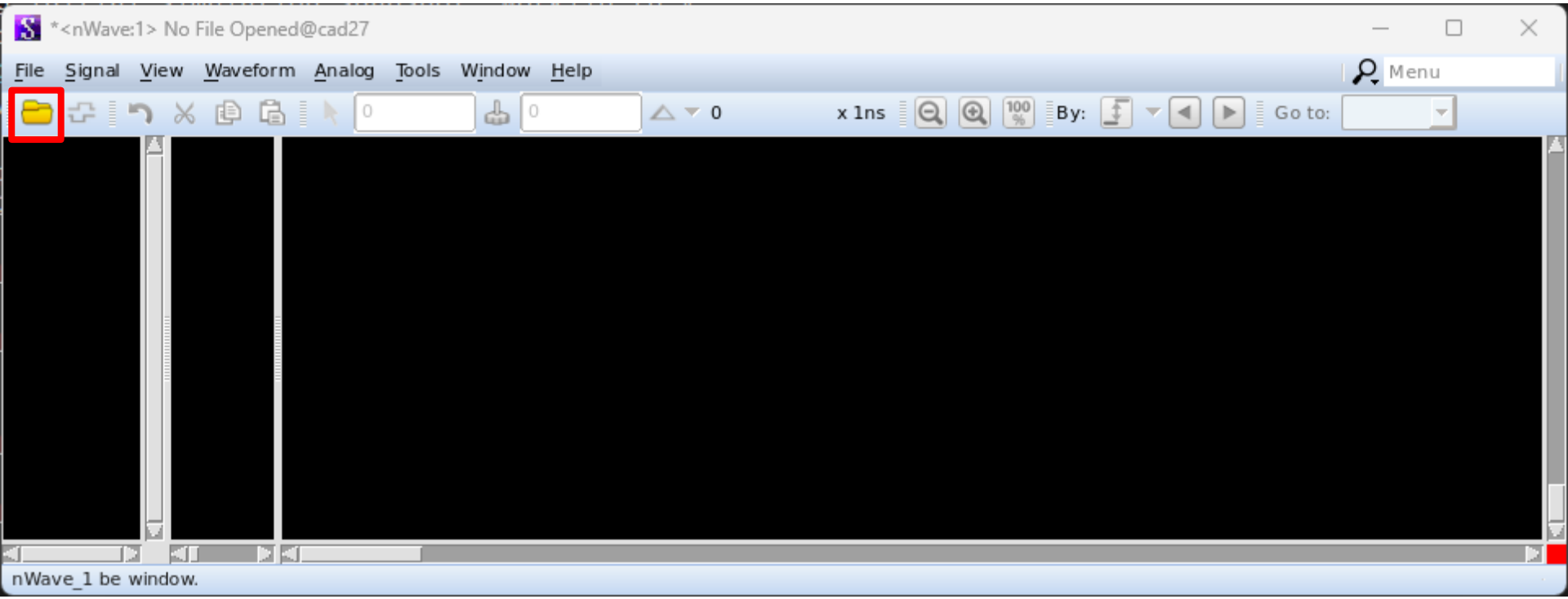
```
 Inclusivity & Diversity - Visit SolvNetPlus to read the "Synopsys Statement on
            Inclusivity and Diversity" (Refer to article 000036315 at
                        https://solvnetplus.synopsys.com)

Parsing design file 'design_tb.v'
Parsing design file 'design.v'
Top Level Modules:
       tb
TimeScale is 1 ns / 1 ps
Starting vcs inline pass...

1 module and 0 UDP read.
recompiling module tb
rm -f _cuarc*.so _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
if [ -x ../simv ]; then chmod a-x ../simv; fi
g++  -o ../simv      -rdynamic  -Wl,-rpath='$ORIGIN'/simv.daidir -Wl,-rpath=./simv.daidir -Wl,-r
/vcs/2022.06/linux64/lib  -Wl,-rpath-link=./  /usr/lib64/libnuma.so.1   objs/amcQw_d.o   _6706_a
  rmar_llvm_0_1.o rmar_llvm_0_0.o          -lvirsim -lerrorinf -lsnpsmalloc -lvfs    -lvcsnew -
/vcs_tls.o   -Wl,-whole-archive  -lvcsucli    -Wl,-no-whole-archive        _vcs_pli_stub_.o   /u
r/cad/synopsys/verdi/cur/share/PLI/VCS/LINUX64/pli.a -ldl  -lc -lm -lpthread -ldl
../simv up to date
CPU time: .509 seconds to compile + .571 seconds to elab + .429 seconds to link
```

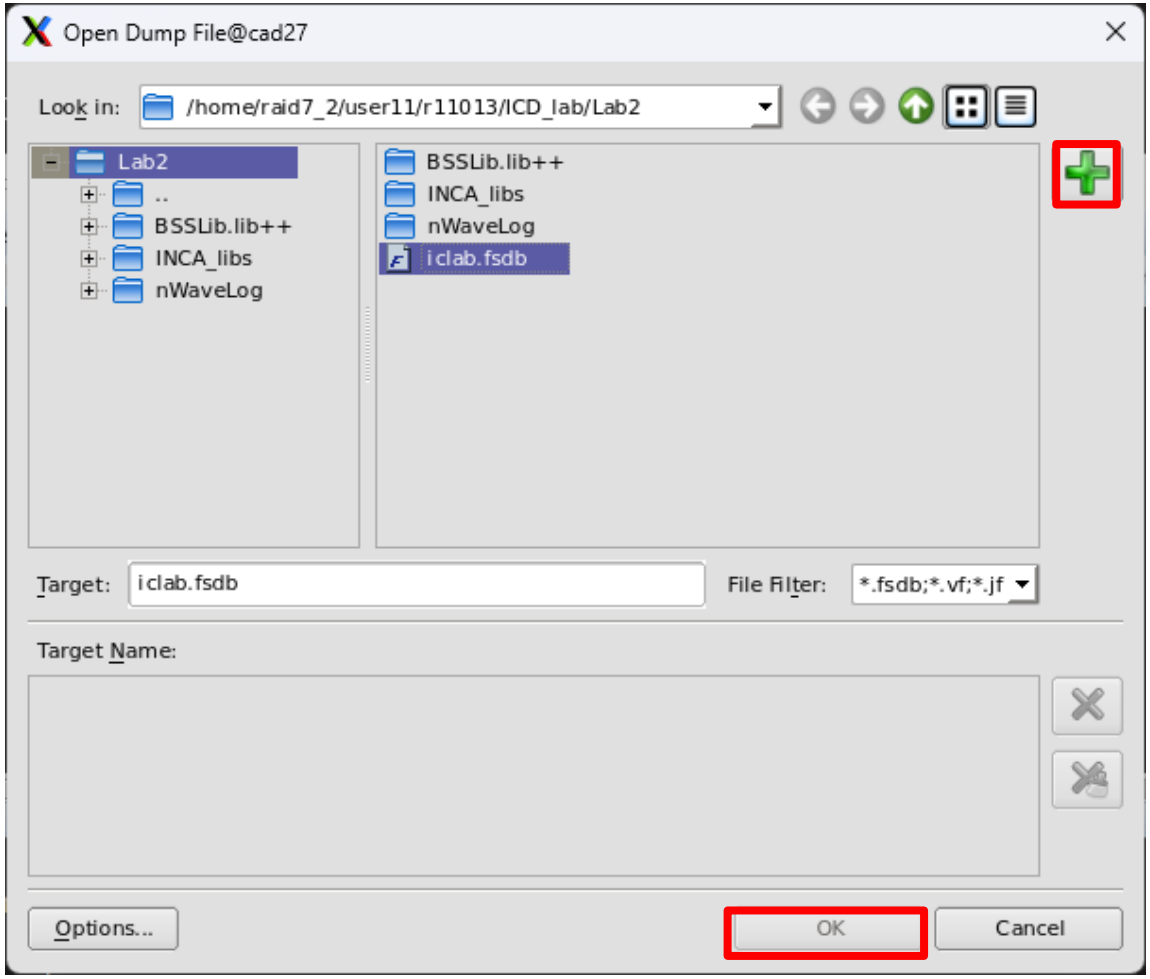
Waveform Verification

- Open nWave. Click the folder icon to open files.



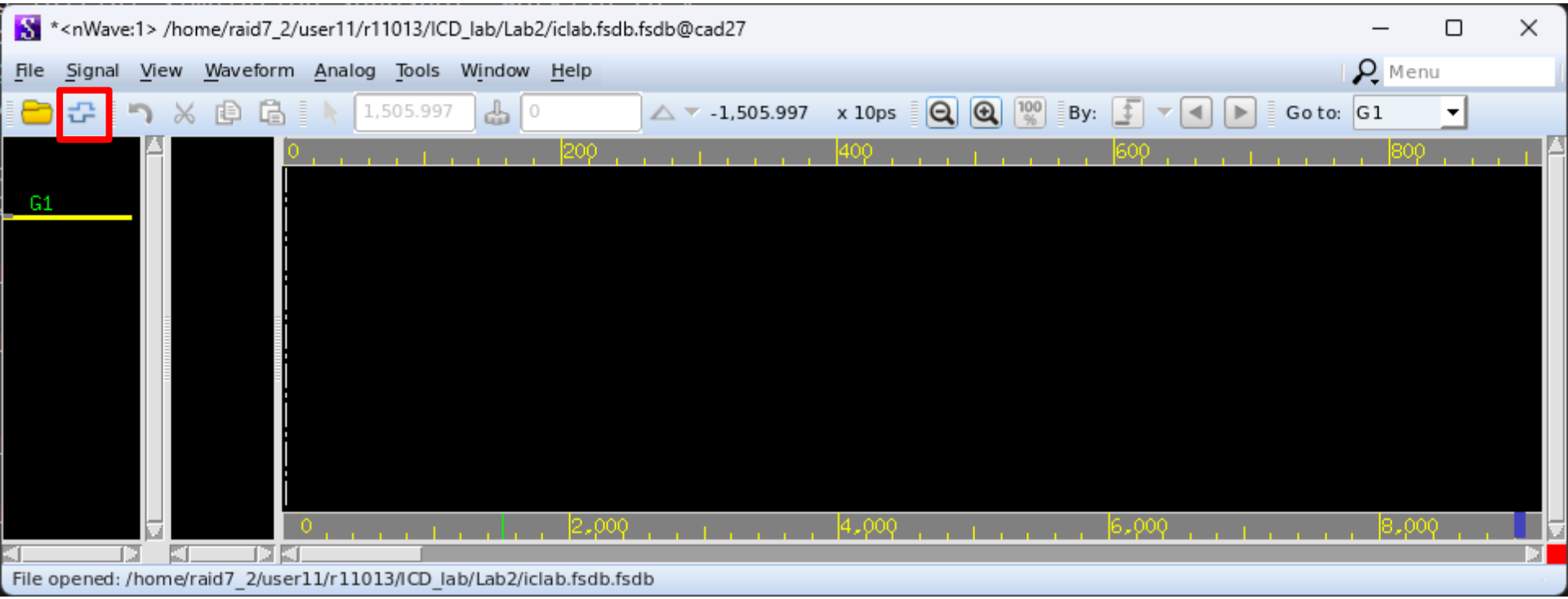
Waveform Verification

- Choose iclab.fsdb. Add, OK.



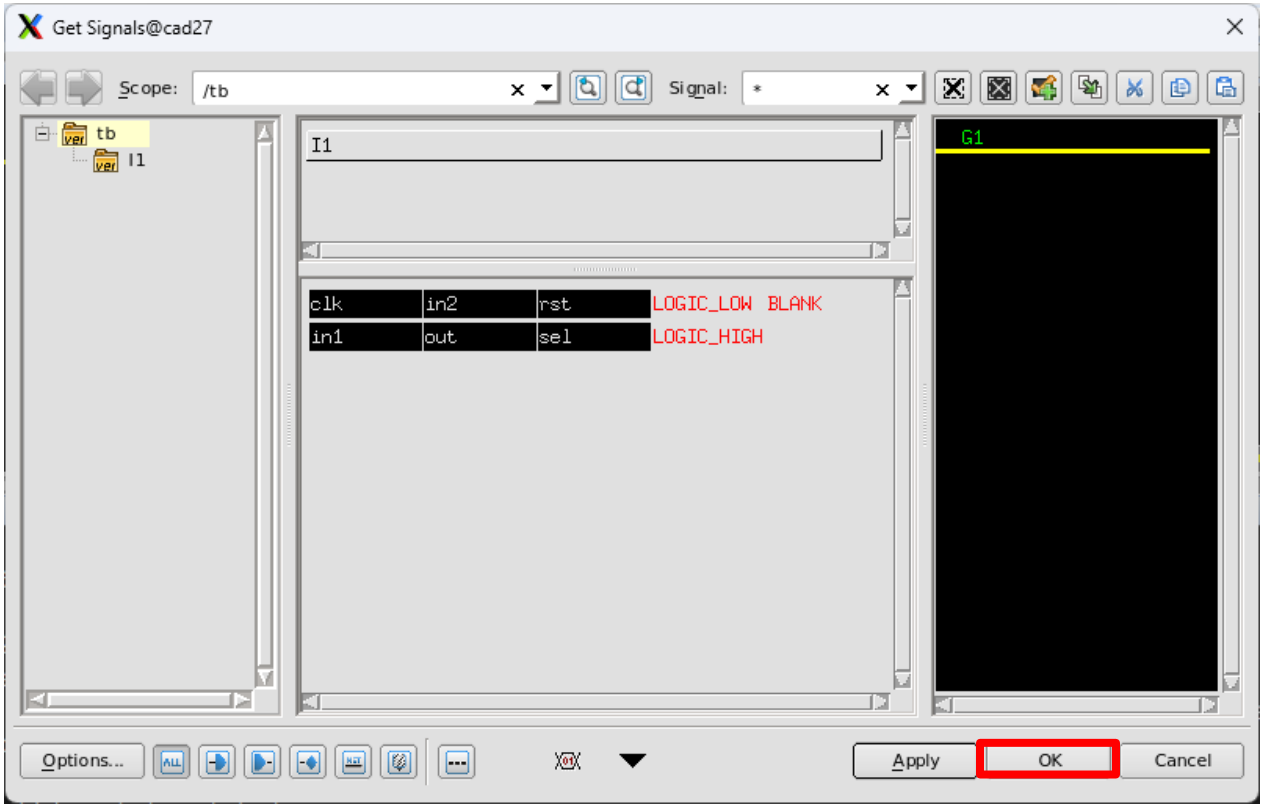
Waveform Verification

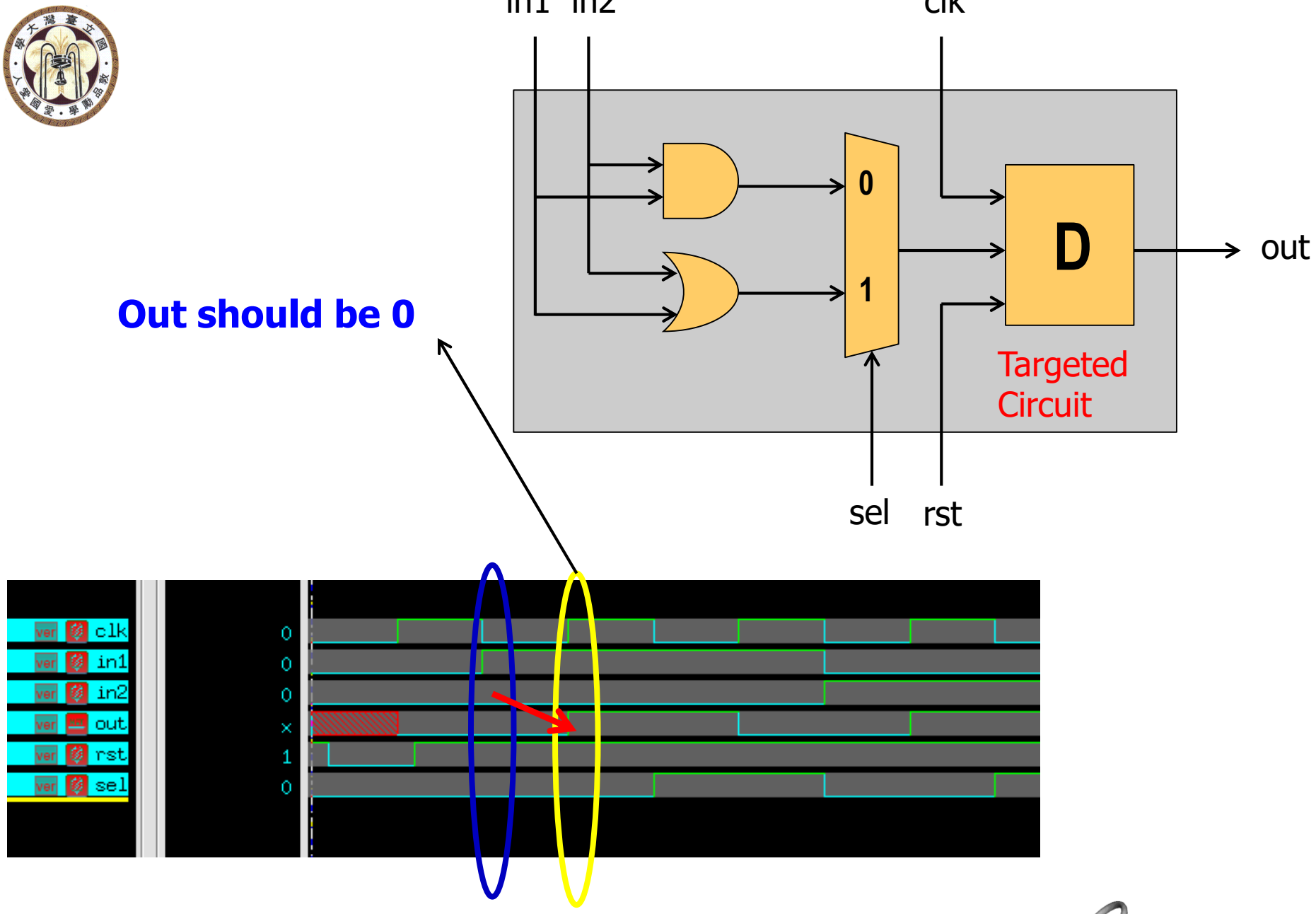
- Display every signal.



Waveform Verification

- Select every signal. Click ok.




in1
in2
clk
0
1
D
out
Targeted
Circuit
sel
rst
Out should be 0
clk
in1
in2
out
rst
sel
0
0
0
x
1
0