Lab3: Synthesis

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Derived from slides by Bo-Yi Chang

Objectives

- In this lab, you will practice synthesizing a design by using design compiler.

Design Files

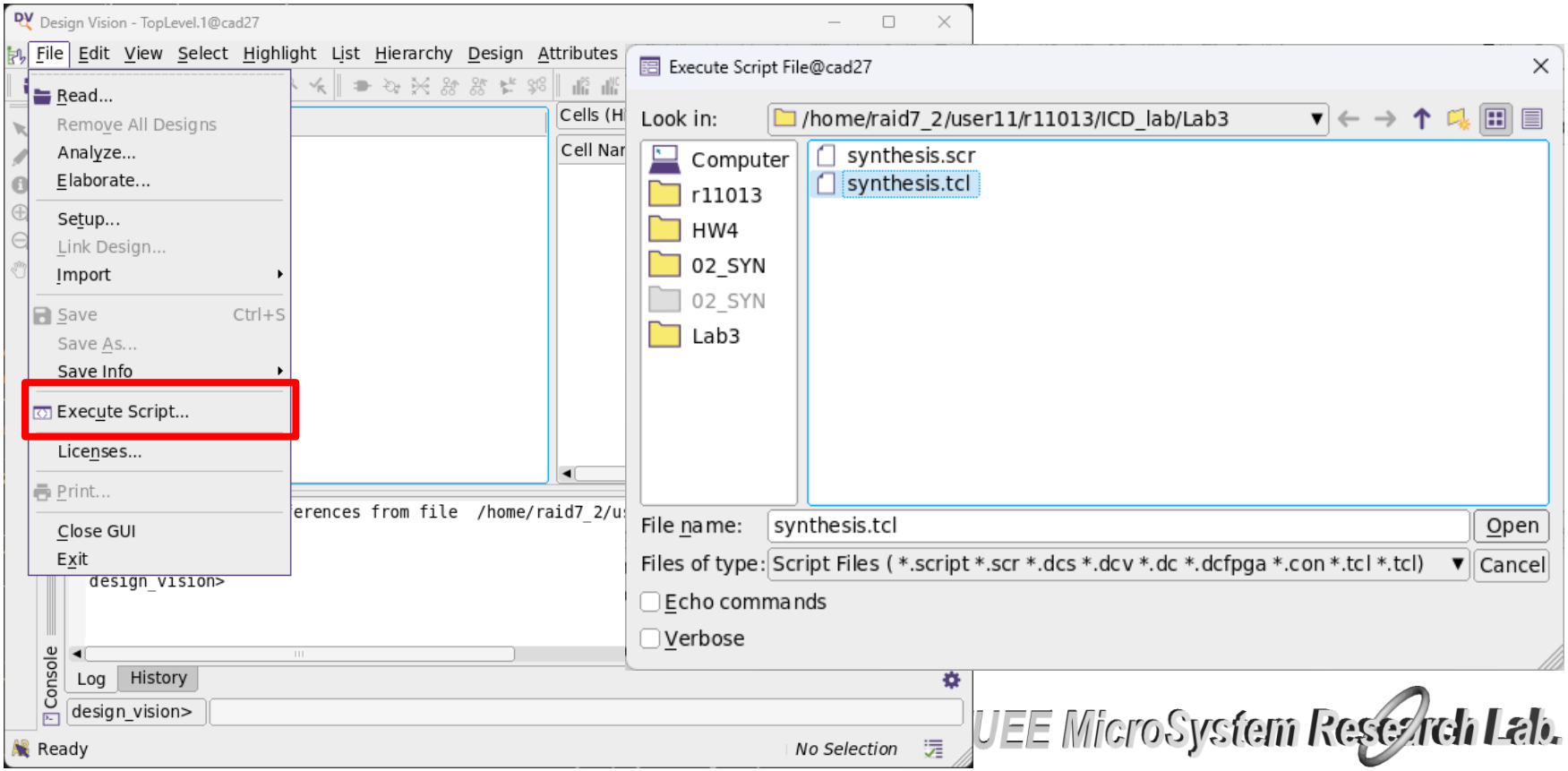
- Download files from NTU Cool and check if you have these files：

1. Some .db files
2. fsa0m_a_generic_core_21.lib
3. Lab3_alu_tb.v
4. Lab1_alu.v
5. synthesis.tcl(and .scr)
6. .synopsys_dc.setup(change _synopsys_dc.setup to .synopsys_dc.setup)

- Put them in the same folder.

Design Compiler

- We provide you a script file so that you do not need to type the commands yourself.



Design Compiler

- We can also use linux command to do synthesis
- dc_shell-t -f synthesis.tcl | tee syn.log

Gate-Level Simulation

- vcs Lab3_alu_tb.v Lab3_alu_syn.v fsa0m_a_generic_core_21.lib.src –full64 –R –debug_access+all +v2k +define+SDF

```
Chronologic VCS simulator copyright 1991-2022
Contains Synopsys proprietary information.
Compiler version T-2022.06_Full64; Runtime version T-2022.06_Full64;  Mar  6 17:23 2024
Warning : License for product VCS-BASE-RUNTIME(947) will expire within 26 days, on: 31-mar-2024.

If you would like to temporarily disable this message, set
 the VCS_LIC_EXPIRE_WARNING environment variable to the number of days
before expiration that you want this message to start (the minimum is 0).

Congratulations!! Your Verilog Code is correct!!

$finish called from file "Lab3_alu_tb.v", line 308.
$finish at simulation time             51854000
           V C S   S i m u l a t i o n   R e p o r t
Time: 51854000 ps
CPU Time:      0.790 seconds;       Data structure size:   0.3Mb
Wed Mar  6 17:24:21 2024
CPU time: 3.317 seconds to compile + .682 seconds to elab + .477 seconds to link + .827 seconds in simulation
```