Building a Memory Array

Term Project of DMHI7005

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Ideal Memory Array with a Placeholder Document

Filp sides of a coin

Physical: Process Module Spec

vs.

Electrical: Device Electric Spec

Memory Cell

- Cell Construction, Interconnect Scheme
- I/O Transfer Characteristics – State, Write, Read

  Cell and Array Parasitics – R/C in cell contact to WL, BL and WL, BL

You will build a memory Array

- Array Construction (Schematic)
- Access Method – Read/Write/Idle, decode/sense, bias and timing
- KPI assessment

States
State Transitions
Transfer Characteristics

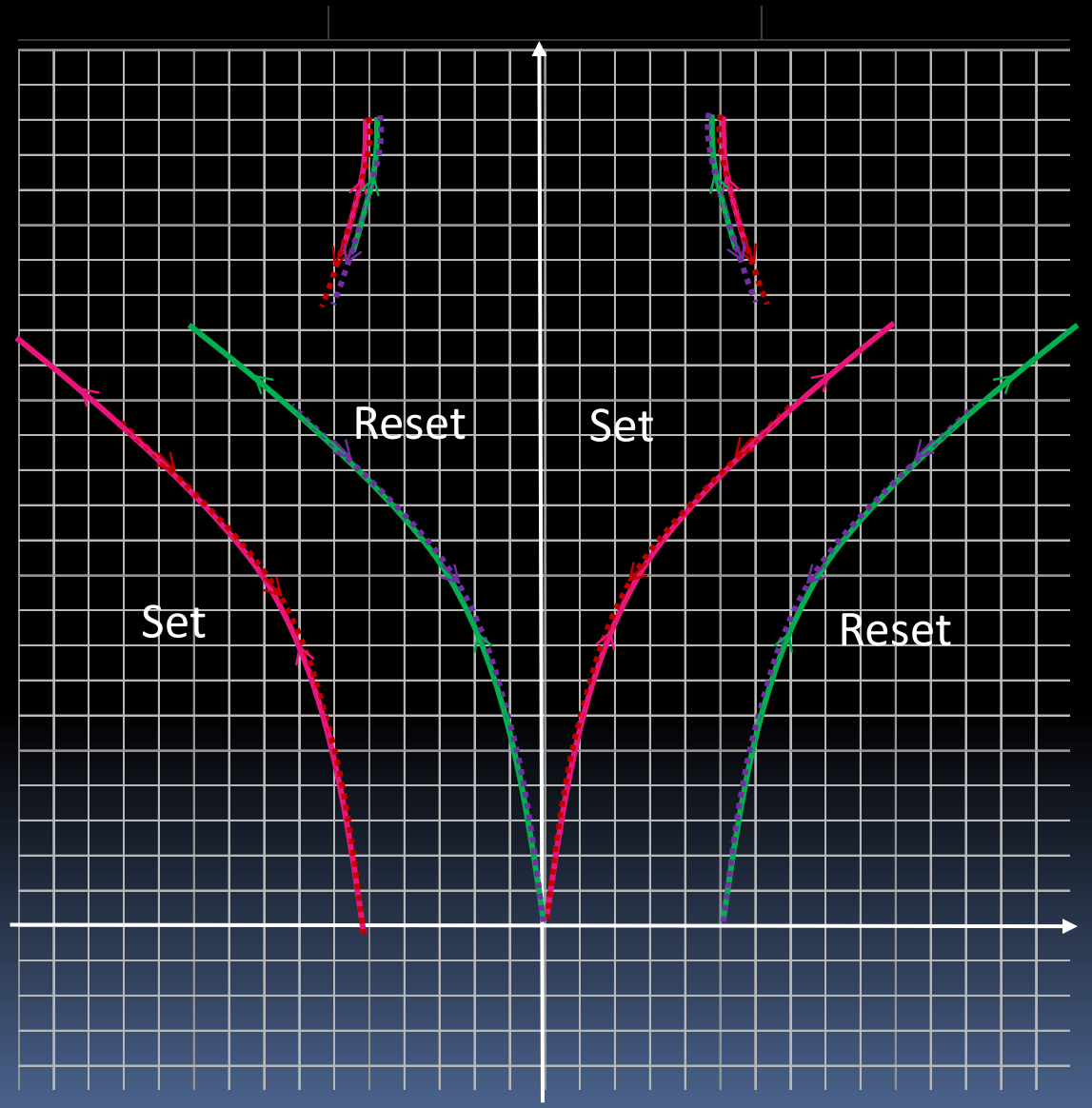
The Hypothetical Memory Cell

Pseudonym called Bipolar Liquid Memory, a.k.a. BLM

Reference:

- **DOI:** 10.1109/IEDM45625.2022.10019415 SKH iedm2022
  Extremely high performance, high density 20nm self-selecting cross-point memory for Compute Express Link
- **DOI:** 10.1109/IEDM50854.2024.10873337 MU, iedm 2025
  VT Window Model of the Single-Chalcogenide Xpoint Memory (SXM)
- **DOI:** 10.1109/IEDM.2009.5424263 INTC, iedm 2009
  A stackable cross point Phase Change Memory

BLM State I-V



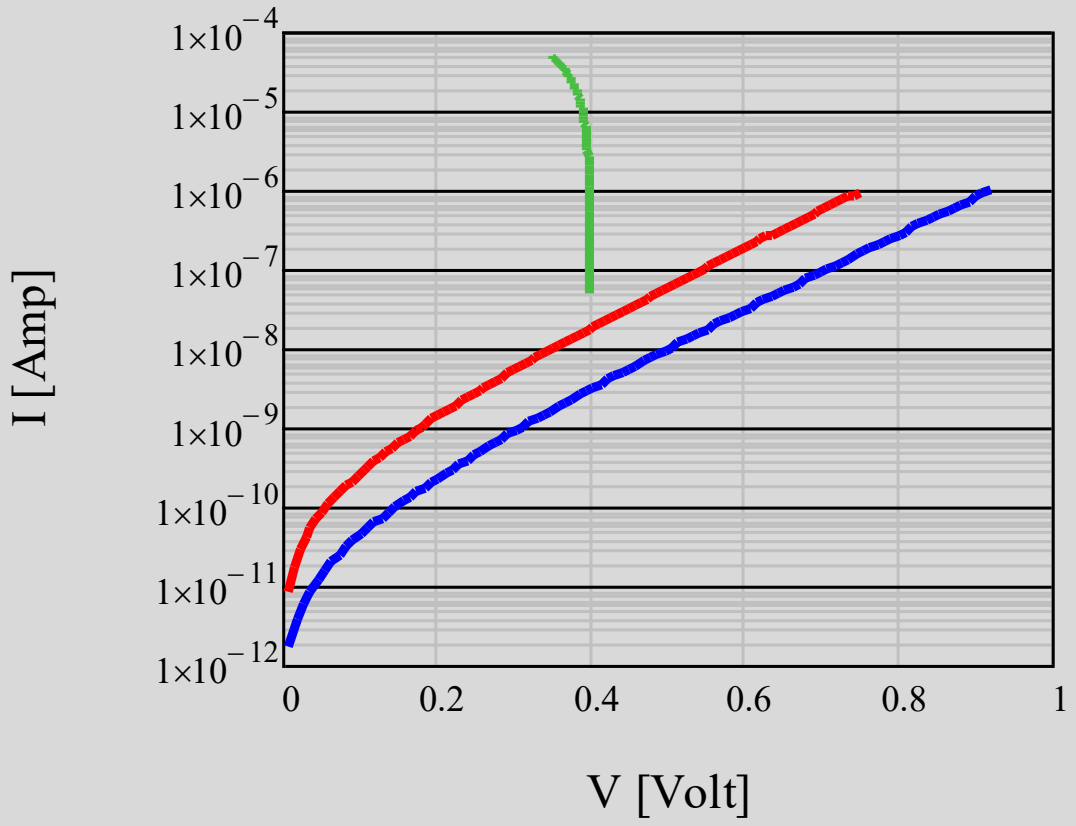
BLM Electric Behavior Model

I-V Characteristics

$$I_{subVt} = \frac{v}{\rho} e^{\frac{v}{ss}}$$

$$ss_{dec} = ss \cdot \ln(10)$$

$$I_{on.lin} = \frac{v - V_h}{R_{on}} + I_h$$



Set State

$V_{Tset} = 750 \cdot mV$ $I_{Tset} = 0.949 \cdot \mu A$

$\rho_{set} = 1 \cdot G\Omega$ $ss_{dec} = 241.771 \cdot \frac{mV}{dec}$

Reset State

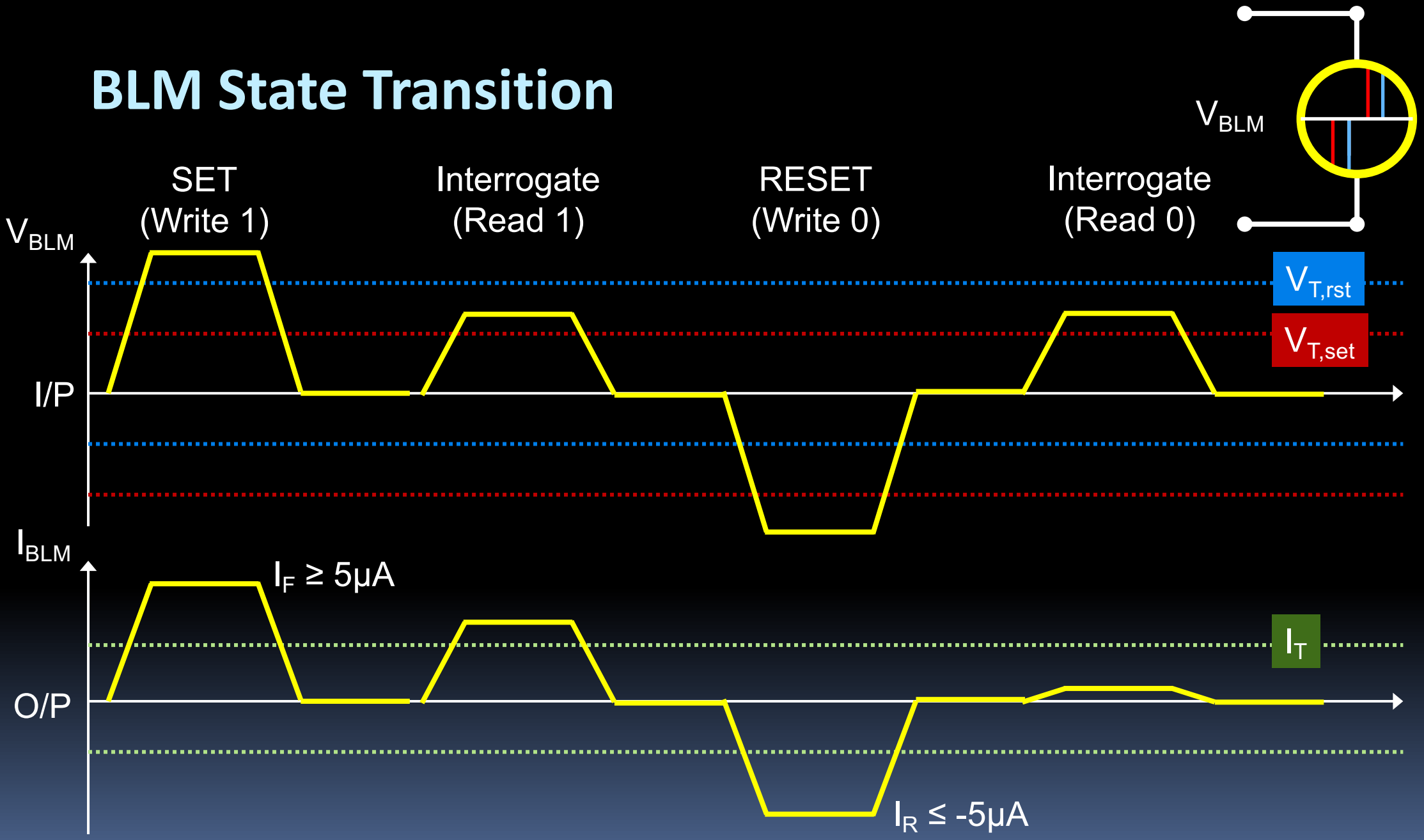
$V_{Trst} = 920 \cdot mV$ $I_{Trst} = 0.979 \cdot \mu A$

$\rho_{rst} = 6 \cdot G\Omega$ $ss_{dec} = 241.771 \cdot \frac{mV}{dec}$

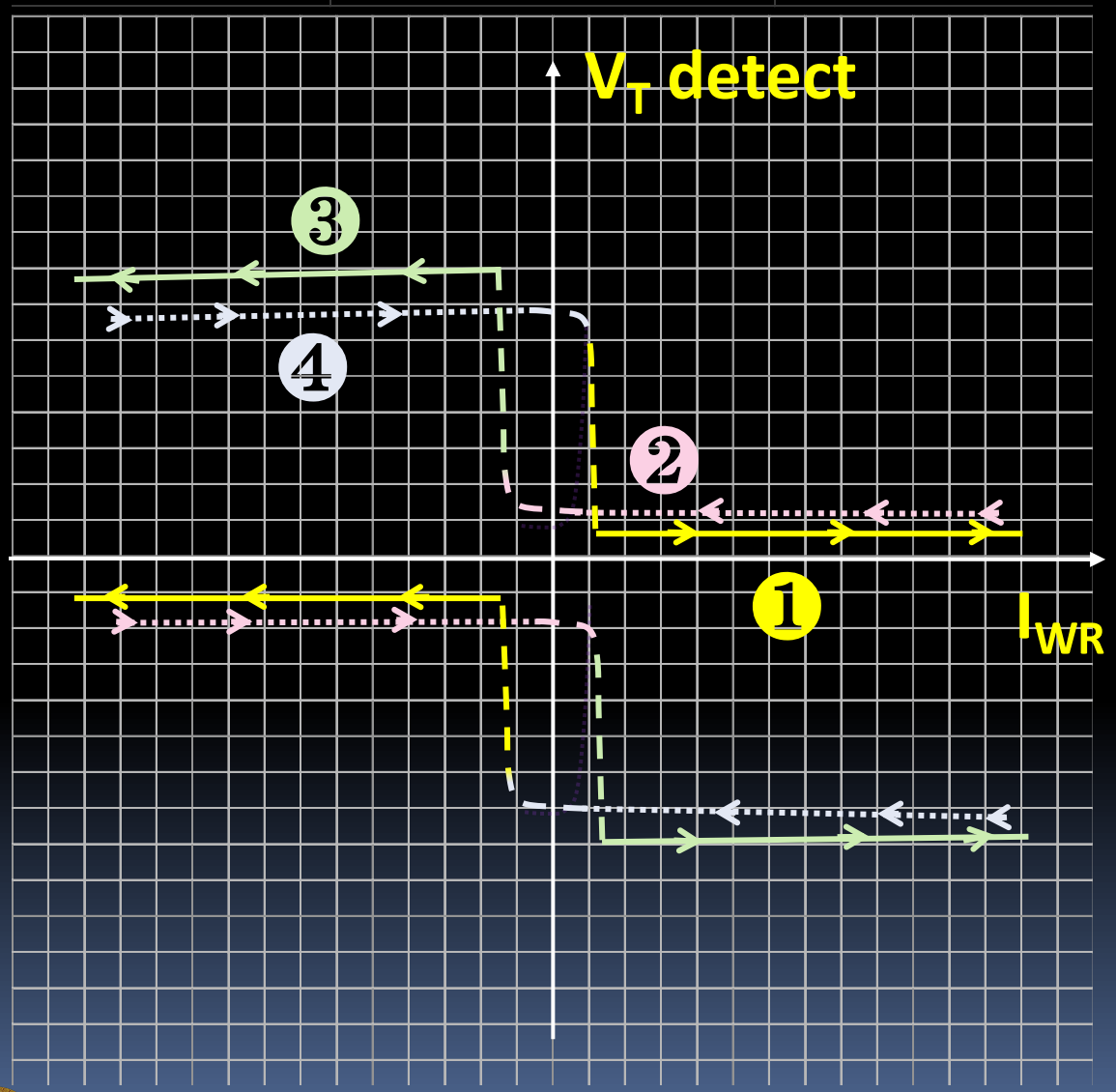
On State

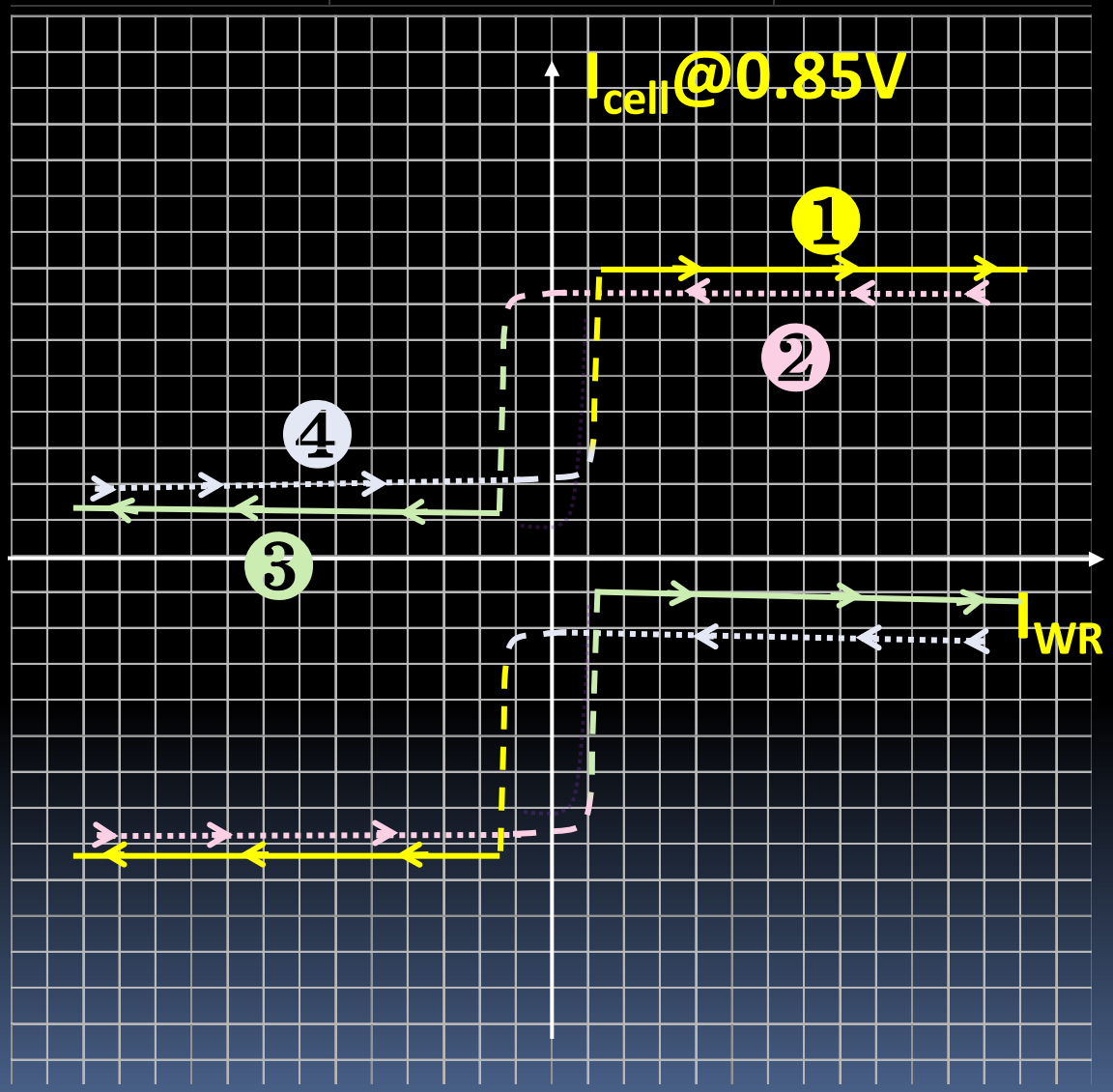
$V_h = 400 \cdot mV$ $I_h = 50 \cdot nA$ $R_{on} = -1 \cdot K\Omega$

BLM State Transition

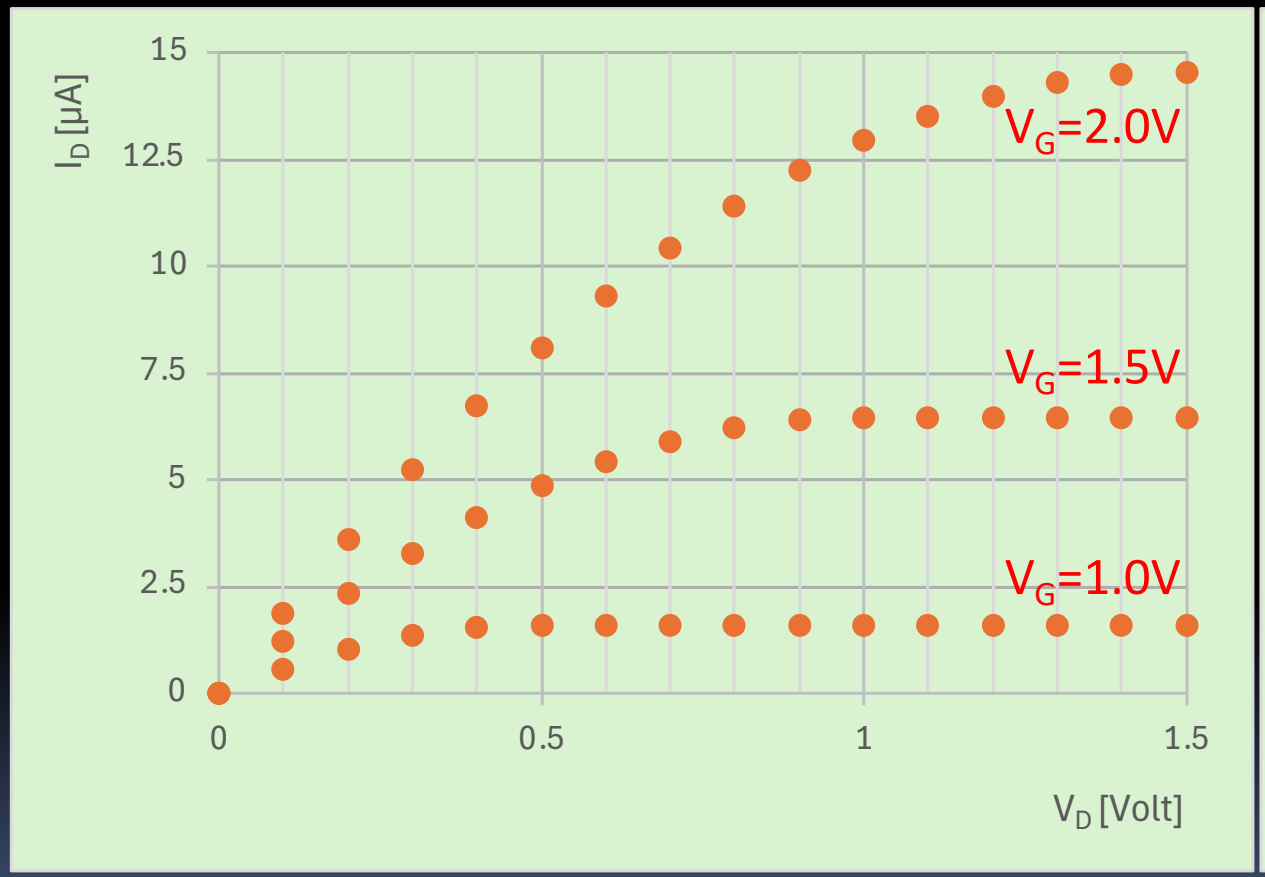


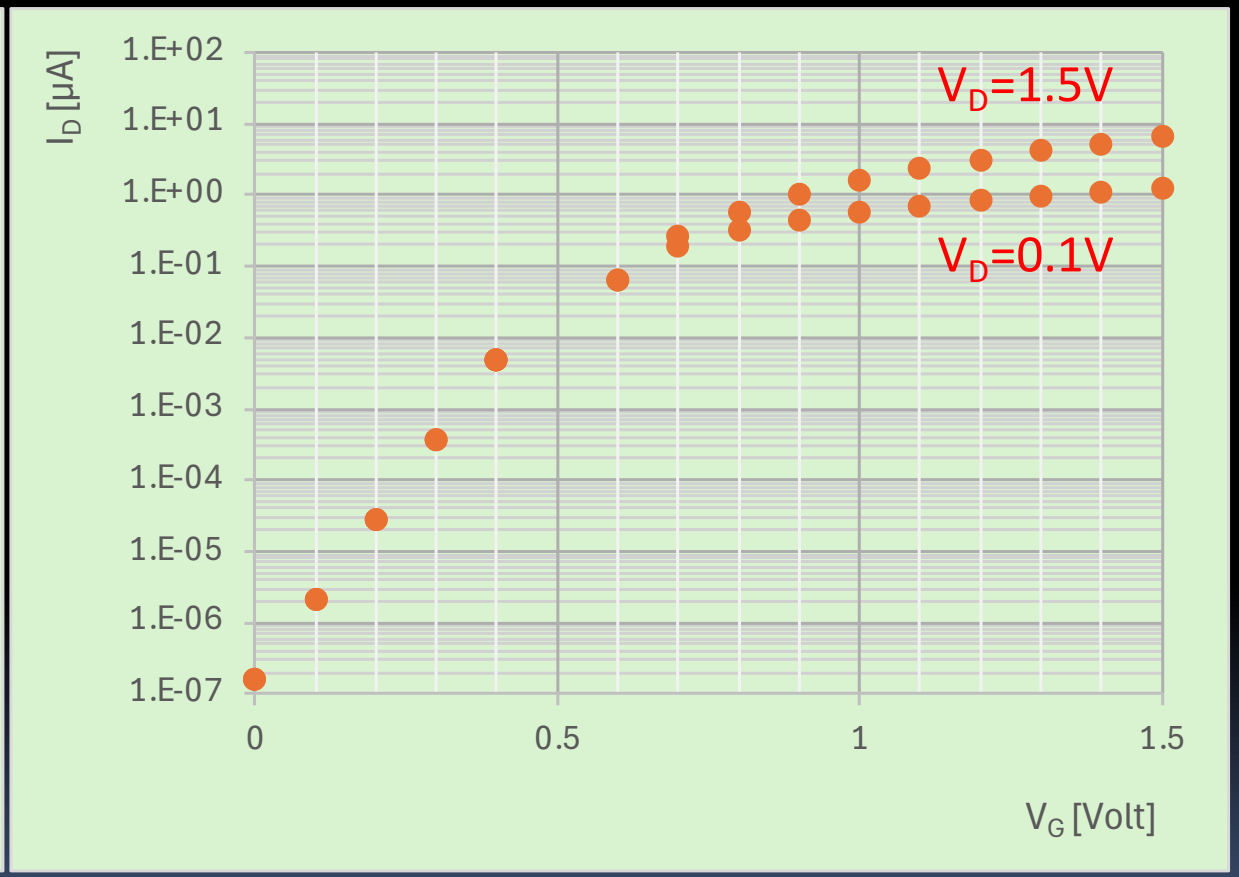
BLM Transfer Characteristics



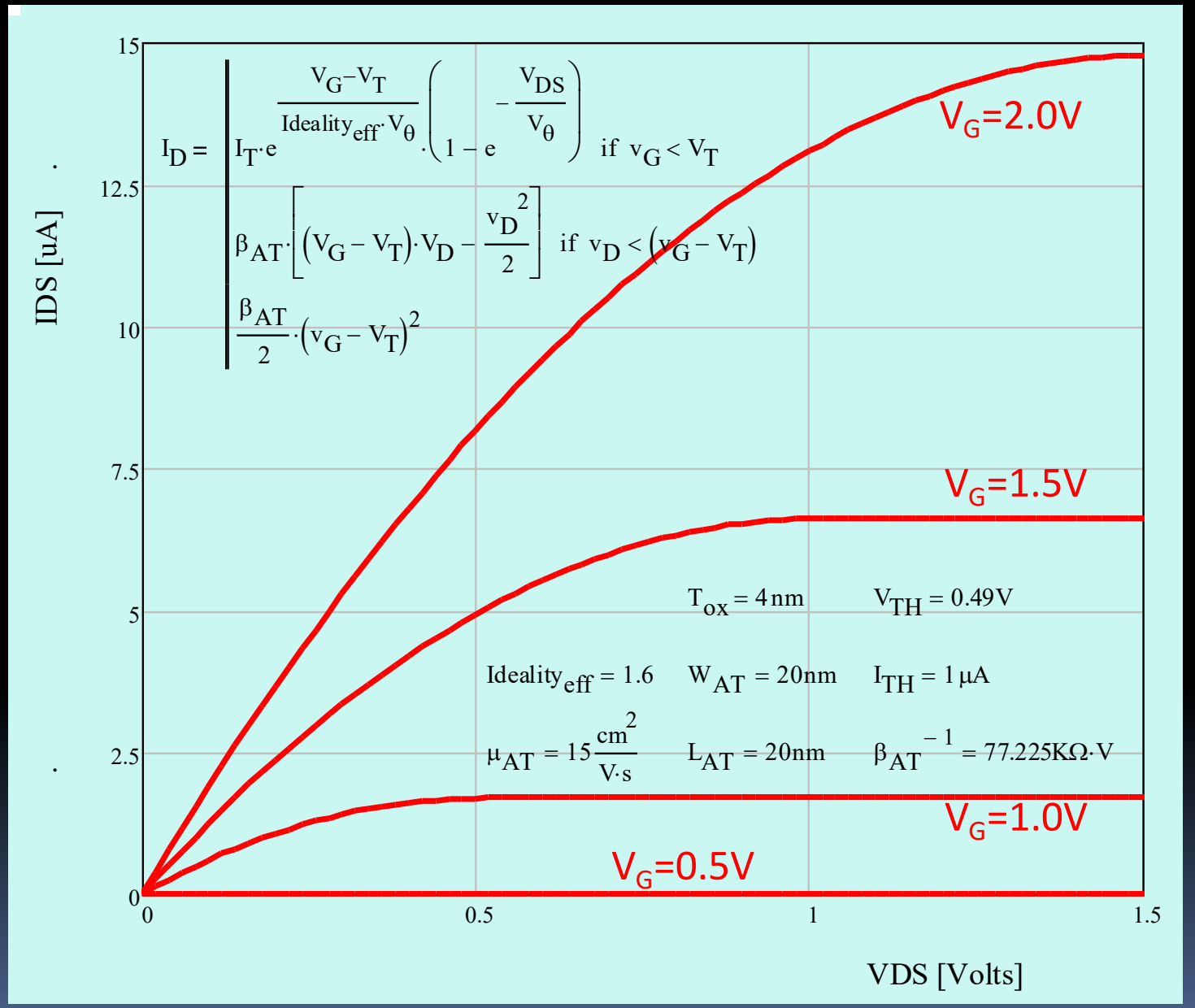


Access Transistor (for optional 1T1R cell)





Access Transistor Behavior Model



Array Parasitics

wordline resistance	**Ω/cell**	10
bitline resistance	**Ω/cell**	10
wordline capacitance	**aF/cell**	30
bitline capacitance	**aF/cell**	30

Supporting Materials

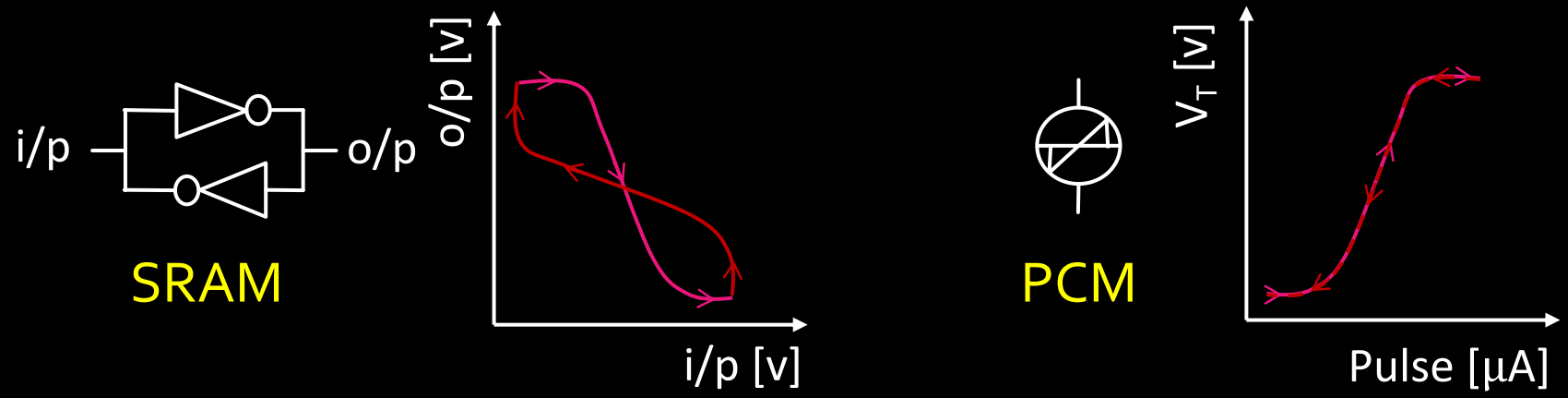
Physics development methodology

Starting with abductive filtering, then moving into inductive refinement.

- It’s a phenomenological ‘duck test’—applying abductive reasoning to prioritize plausible switching mechanisms in new device assessments, while systematically ruling out less likely alternatives.
- Once the scope is narrowed, inductive reasoning will be applied to extract underlying physics from specific observations. Key assumptions will be explicitly identified and subjected to validation.

“Hysteresis” of Transfer characteristics

- Output traces subject to input and prior history in a cyclic loop



- Transfer characteristics:
  - Input (WRITE) metrology actuates the switching mechanism
  - Output (READ) metrology manifests the switched physics
- Benchmark with the similar transfer characteristics to construct hypothesis

BLM References – Keywords SSM, SOM, SXM

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   Polarity-dependent threshold voltage shift in ovonic threshold switches: Challenges and opportunities
2. **DOI:** 10.1109/IEDM45625.2022.10019415 SKH IEDM 2022
   Extremely high performance, high density 20nm self-selecting cross-point memory for Compute Express Link
3. **DOI:** 10.23919/VLSITechnologyandCir57934.2023.10185210 SKH VLSI 2023
   The chalcogenide-based memory technology continues: beyond 20nm 4-deck 256Gb cross-point memor
4. **DOI:** 10.1109/IEDM45741.2023.10413748 SKH IEDM 2023
   Enhanced Endurance Characteristics in High Performance 16nm Selector Only Memory (SOM)
5. **DOI:** 10.1109/IEDM45741.2023.10413815 POSTECH IEDM 2023
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    Enhancing Selector-Only Memory Reliability Through Multi-Step Write Pulse
11. **DOI:** 10.1109/IEDM50854.2024.10873326 Samsung IEDM 2024
    Ab-Initio Screening of Amorphous Chalcogenides for Selector-Only Memory (SOM) through Electrical Properties and Device Reliability
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    Achieving 3-bit Operation in Selector-only-memory by Controlling Variability with Microwave Annealing and Bipolar Pulse Scheme
13. **DOI:** 10.1109/IEDM50854.2024.10873555 IMEC iedm 2024
    Selector Only Memory: Exploring Atomic Mechanisms from First-Principles
14. **DOI:** 10.1109/LED.2024.3497957 POSTECH EDL 2025
    Improved Memory Performance Through Integration of Ferroelectric and Ovonic Threshold Switching Layer
15. **DOI:** 10.1109/LED.2025.3549369 POSTECH EDL 2025
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16. **DOI:** 10.1109/IMW61990.2025.11026942 Macronix IMW 2025
    Enhancing 3D XPT/SOM Reliability: Strategies for Mitigating Spike Current and Improving Read Endurance
17. **DOI:** 10.23919/VLSITechnologyandCir65189.2025.11074870 SKH, VLSI 2025
    Achieving Outstanding Endurance (>10^7) in Large-Array Two-Deck 16 nm SOM Through Process, Structure, and Design Strategies for Emerging SCM Applications
18. **DOI:** 10.23919/VLSITechnologyandCir65189.2025.11075063 Samsung VLSI 2025
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19. **DOI:** 10.23919/VLSITechnologyandCir65189.2025.11075112 Postech VLSI 2025
    Multi-Stack InTe Selector-Only Memory (SOM) Achieving Ultra-Low Power Operation (10 μA) **and Excellent Endurance (**~1010 **cycles)**
20. **DOI:** 10.23919/VLSITechnologyandCir65189.2025.11074807 Samsung VLSI 2025
    Differences in Operational Mechanisms of As- and Sb-Based Selector Only Memory for Emerging 3DXP Architecture
21. **DOI:** 10.1109/JEDS.2025.3557732 Postech, JEDS 2025
    Optimizing Pulse Conditions for Enhanced Memory Performance of Se-Based Selector-Only Memory
22. DOI: 10.48550/arXiv.2508.12118 Micron, Arxiv 2025
    Microscopic model of the operation of the Single-chalcogenide X-point Memory
23. **DOI:** 10.1109/IEDM50854.2024.10873337 Micron, IEDM 2025
    VT Window Model of the Single-Chalcogenide Xpoint Memory (SXM

Access Transistor Behavior Model in Python

```
import numpy as np
import csv

# Device parameters
tox = 4e-9             # gate oxide thickness [m]
eps0 = 8.854e-12       # permittivity of free space [F/m]
eps_ox = 3.9 * eps0    # SiO2 permittivity [F/m]
Cox = eps_ox / tox     # oxide capacitance per area [F/m^2]
mu = 0.0015            # electron mobility [m^2/V·s]
W = 20e-9              # channel width [m]
L = 20e-9              # channel length [m]
Vth = 0.49             # threshold voltage [V]
n_factor = 1.6         # subthreshold slope factor
Vt_thermal = 0.026     # thermal voltage [V]
I0 = 1e-6              # prefactor for subthreshold [A]

# Precompute K = μ·Cox·(W/L)
K = mu * Cox * (W / L)
# Bias vectors
Vds_vals = np.arange(0, 2.01, 0.1)
Vgs_vals = np.arange(0, 2.01, 0.1)

with open('nmos_id_table.csv', 'w', newline='') as f:
    writer = csv.writer(f)
    writer.writerow(['Vds (V)', 'Vgs (V)', 'Id (μA)'])
    for Vgs in Vgs_vals:
        for Vds in Vds_vals:
            # enforce zero current at Vds = 0
            if Vds == 0.0:
                Id = 0.0
            # subthreshold region
            elif Vgs < Vth:
                Id = I0 * np.exp((Vgs - Vth) / (n_factor * Vt_thermal)) * (1 - np.exp(-Vds / Vt_thermal))
            else:
                # linear/triode if Vds < Vgs - Vth
                if Vds < (Vgs - Vth):
                    Id = K * ((Vgs - Vth) * Vds - 0.5 * Vds**2)
                # saturation otherwise
                else:
                    Id = 0.5 * K * (Vgs - Vth)**2
            # convert to microamps
            writer.writerow([f'{Vds:.1f}', f'{Vgs:.1f}', f'{Id*1e6:.6f}'])
print("Generated nmos_id_table.csv with 21×21 bias points.")
```