CSA Project Phase I

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1. Draw the schematic for a single stage processor and fill in your code in the to run the simulator.

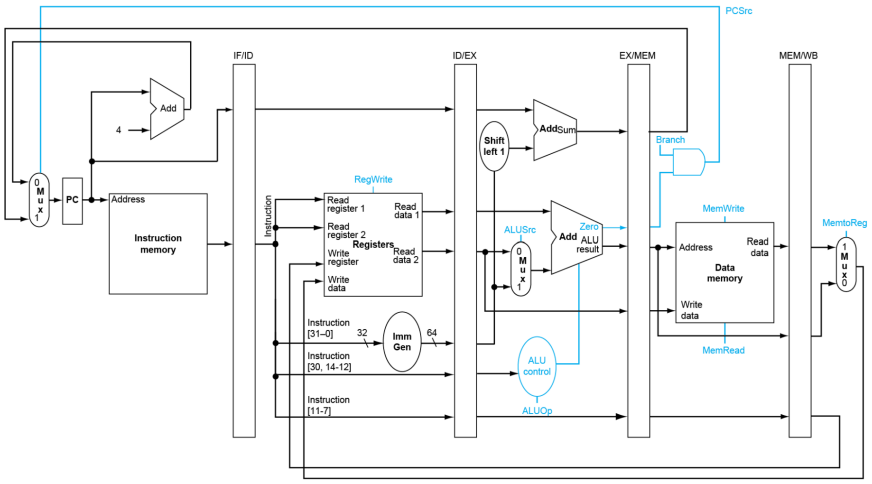

Figure 1: Single stage processor schematic (Source: Lecture 4 slide 84)

This is the whole schematic of the single stage processor. I implemented instruction fetch, instruction decode, instruction execution, load and store, write back in a cycle, which can be shown by Figure 1

2. Measure and report average CPI, Total execution cycles, and Instructions per cycle for both these cores by adding performance monitors to your code.

testcase0:

```
Single Stage Core Performance Metrics-----------------------------
Number of cycles: 6
Total Number of Instructions: 5
Cycles per instruction: 1.2
Instructions per cycle: 0.833333
```

testcase1:

```
Single Stage Core Performance Metrics-----------------------------
Number of cycles: 40
Total Number of Instructions: 39
Cycles per instruction: 1.02564
Instructions per cycle: 0.975001
```

testcase2:

```
Single Stage Core Performance Metrics-----------------------------
Number of cycles: 28
Total Number of Instructions: 11
Cycles per instruction: 2.54545
Instructions per cycle: 0.392858
```