Aseem Maheshwari

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Summary

- 20+ years of experience in ASIC/FPGA design and verification with 5+ years in leading ASIC pre & post-silicon teams
- Hands-on expertise in building scalable, reusable, self-checking DV TBs using SystemVerilog/UVM methodology; building emulation & formal testbenches; post-silicon validation
- Proven success in fostering productive working relationships, managing multiple, simultaneous tasks while leading and directing high performance engineering teams to complete projects within time and budget constraints
- Strong technical and management skills. Excellent written and verbal communication skills

Experience

Meta Platforms Oct 2022 – Present
Silicon Engineering Manager *Sunnyvale, CA*

- Leading a team developing IPs for AR/VR optimized silicon relying heavily on Audio, Machine Learning and Low Power technologies
- Responsibilities include architecture, micro-architecture, RTL design, synthesis/PnR and static timing analysis, functional/gate-level verification, FPGA implementation and prototyping, and lab debug
- Managing IP requirements and tradeoffs among features, performance, cost, and schedule in close collaboration with systems and software leads
- Spearheading initiatives to improve quality, velocity, and satisfaction

Palo Alto Networks Jun 2013 – Oct 2022
Sr. Principal Engineer, ASIC Engineering *Santa Clara, CA*

- Managed a team of 15+ engineers verifying complex ASICs for firewall products. Responsible for staffing (internally as well as leveraging external partners), planning, schedules and employee assessments
- Leading effort for defining/verifying fourth generation Flow Engine ASIC. Led effort to successfully verify/tape-out/bring up silicon for multiple generations of flow engine chips
- Championed design verification methodology improvements/enhancements to improve design and verification quality and development time
  * Drove emulator selection, deployment and use models
  * Deployed automated mechanisms to validate PCAPs against architectural and simulation models
  * Status reporting and dashboards
- Verifying QoS features (scheduling, shaping) using a Python-SystemC-Veloce emulation flow
- Verified multiple blocks in the ingress and egress pipelines including the access control lists and the forwarding engines
- Verified ISA of a custom microcontroller by developing a reference model using SystemC, a random instruction generator using Python, formal property verification using VC-Formal

Seagate (formerly SandForce, LSI, Avago) Jul 2011 – Jun 2013
Principal Verification Design Engineer *Milpitas, CA*

- Verified the 4x Gen2 dual-port PCIe interface for the next-generation flash storage processor. Architected and developed infrastructure and tests for AHCI and NVM Express (NVMe) host interfaces in a PCIe environment using UVM. Also verified hardware-based virtualization (SR-IOV), power management, error handling and recovery features, including interrupt servicing

- Wrote embedded firmware tests in C to verify DMA (over PCIe) programming model and functionality. Also wrote tests duplicating emulation fail scenarios to facilitate debug

Marvell (formerly Cavium) Mar 2008 – Jul 2011

Principal Engineer *Marlborough, MA*

- Designed and implemented the add-work engine for the schedule/synchronize/order unit in the Octeon 2 CN68xx product line. The logic handled ordering of new work into 8 input work queues of arbitrarily large size (with overflow into DRAM), with a performance of 100M add-work's/sec
- Owned full chip integration, modeling the PLLs and pad frame on CN63xx, In addition, added in hardware-assist logic to all of CN63xx's MAC-PHY interfaces to support the IEEE 1588 protocol
- Designed and implemented a high-performance DDR3 Memory Controller for the Octeon 2 CN63xx/CN68xx product lines. Developed several advanced queuing, arbitration, page-management, and scheduling features to maximize bandwidth, minimize latency, and optimize power management of the controller. Worked with custom designers to implement the associated PHY in a 65nm process, targeted at up to DDR3-1600. Ran synthesis and timing analysis to meet timing performance, power and yield constraints. Also ran gate level simulations with back-annotated SDF and LEC formal verification to verify quality
- Verified the NAND Flash Controller for the Octeon Plus CN52xx product line

Texas Instruments Oct 2003 – Mar 2008

Design Verification Lead *Dallas, TX*

- Led a team of 4 engineers verifying a multi-core, multi-threaded VLIW DSP. Responsible for verification planning, defining test generation flows, infrastructure development and execution
- Championed effort to align methodology and tools for processor verification across TI
- Led project to improve product delivery for the Guinness Book of World Record winning 1GHz DSP. Reduced test times by 2s per test insertion for an overall savings of 3.09 months of tester time per million parts
- Verified the low power and memory test/characterization features of a single chip W-CDMA baseband device for the base station market. The market for this chip is estimated to be US$ 600 million
- Verified a 750 MHz fixed point ISA DSP (part of the TMS320 family of DSPs). This CPU core (along with the corresponding mega-module) is being leveraged in multiple chips across TI. The market for this core is estimated to be over US$ 1 billion over the next ten years

Intrinsix Mar 2001 – Oct 2003

Design Engineer *Westborough, MA*

- Worked on multiple product teams with responsibilities including micro-architecture, RTL design, synthesis and static timing analysis, functional/gate-level verification, FPGA implementation and prototyping, and lab debug
- Successful projects included verification of a personal authentication SoC (for use in Bloomberg terminals), design and implementation of a Digital Test Controller FPGA (for MEMS test systems), verification and synthesis of a high-performance configurable RISC core and design and implementation of major portions of a telephony/switch ASIC

Immersive Technologies Jun 2000 – Jan 2001

Design Engineer *Malden, MA*

- Developed and implemented a 'beam traversal' algorithm in C++ for finding geometry in the path of a beam, to replace the traditional ray tracing algorithms used for rendering in computer graphics. Resulted in a 3-5x speed-up in the image generation time
- Designed and implemented a fully pipelined hash-table in hardware to replace one in software. The design took in five 16-bit integers, computed the hash, interacted with SRAM and output the hashed-value

Education

Carnegie Mellon University Aug 1998 – May 2000
Master of Science, Electrical & Computer Engineering *Pittsburgh, PA*

Indian Institute of Technology (IIT), Madras Aug 1994 – May 1998
Bachelor of Technology, Electrical Engineering *Chennai, India*

Skills

Languages/Methodology Verilog, SystemVerilog, UVM, VHDL, Verisity e, Verilog PLI/DPI, C, C++, Perl, Python, Make, Shell scripting, SVA, TestBuilder

Protocols/Standards/Interfaces PCIe, AHCI, NVM Express, ONFI, DDR3, Ethernet, Interlaken