SoC/ASIC Verification Consultant · aseemm@gmail.com

Aseem Maheshwari | Resume

- Profile: 20+ years of ASIC/FPGA verification experience
- Languages: UVM, SystemVerilog, Verilog, C/C++/SystemC, Python
- Methodology: Constrained-random/Coverage-driven Simulation, Emulation, Formal, Architecture/Performance Modeling, SVA
- Protocols: PCIe, AHCI, NVM Express, Interlaken, DDR3, Ethernet (L2, L3, L4)
- Domains: Networking, Processors (CPU, DSP), Storage (SSDs, DDR3)

Experience

ASIC Verification Engineer

- Verified multiple blocks in the ingress and egress pipelines including the access control list and the forwarding engine using a constrained-random UVM environment
- Verified ISA of a custom microcontroller by developing a reference model using SystemC, a random instruction generator using Python, formal property verification using VC-Formal
- Verified QoS features (scheduling, shaping) using a Python-SystemC-Veloce emulation flow

ASIC Verification Engineer

- Verified a 4x Gen2 PCIe interface for a storage processor. Developed infrastrucure and tests for AHCI and NVMe host interfaces using UVM. Verified SR-IOV, power management, error handling and recovery features, including interrupt servicing
- Wrote embedded firmware tests in C to verify DMA (over PCIe) programming model and functionaity

SoC Verification Engineer

- Designed/Implemented a high-performance DDR3 memory controller with advanced queuing, arbitration, page-management and scheduling features
- Verified NAND Flash Controller using a C based TB

SoC Verification Engineer

- Verified a multi-core multi-threaded VLIW DSP and a fixed-point ISA DSP

Education

Carnegie Mellon University (Pittsburgh, PA)

- Master of Science, Electrical and Computer Engineering

Indian Institute of Technology, Madras (Chennai, India)

- Bachelor of Technology, Electrical Engineering