ASEEM MAHESHWARI

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Technical Skills

Languages: Python, C/C++, HTML/CSS, JavaScript, SQL, Verilog, SystemVerilog
Libraries/Frameworks: React, Node.js, Gatsby, Flask, Tensorflow, Dash, SystemC, UVM
Big Data & ML: Python (numpy, pandas, matplotlib, seaborn)
Misc: Docker, Git, Jenkins

Projects

Gym Reservation Bot | *Python, Selenium, Google Cloud Console*   **January 2021**
- Utilized python to implement unsupervised machine learning techniques for time series anamoly detection on 3TB of unstructured data, which reduced total process time by 20 percent.
- Wrangld 10TB of trading data stored in Hadoop DFS using Scala to remodel and visualize.

Ticket Price Calculator App | *Java, Android Studio*   **November 2020**
- Created an Android application using Java and Android Studio to calculate ticket prices for trips to museums in NYC.
- Processed user inputted information in the back-end of the app to return a subtotal price based on the tickets selected.
- Utilized the layout editor to create a UI for the application in order to allow different scenes to interact with each other.

Transaction Management GUI | *Java, Eclipse, JavaFX*   **October 2020**
- Designed a sample banking transaction system using Java to simulate the common functions of using a bank account.
- Used JavaFX to create a GUI that supports actions such as creating an account, deposit, withdraw, list all acounts, etc.
- Implemented object-oriented programming practices such as inheritance to create different account types and databases.

Experience

Palo Alto Networks   **June 2012 – Present**
Sr. Principal Engineer, ASIC Engineering   *Santa Clara, CA*
- Hardware verification of complex ASICs used in firewalls (ACL, Forwarding, Packet-edit Engines, QoS features, Microcontroller ISA, Ethernet, Interlaken)
- Managed a team of 15+ engineers as well as worked as an individual contributor
- Championed methodology improvements for quality (formal, emulation) and schedule improvements
- **Technologies used:** UVM, SystemVerilog, Python, SystemC

Seagate (formerly SandForce)   **July 2011 – June 2013**
Principal Engineer   *Milpitas, CA*
- Hardware verification of flash storage processors (PCIe, AHCI, NVMe, DMA Engines)
- **Technologies used:** UVM, SystemVerilog, C, Synopsys VCS

Marvell (formerly Cavium)   **March 2008 – July 2011**
Principal Engineer   *Marlborough, MA*
- Hardware design of network processors (DDR3 controller, Add-work engines, Full chip integration, IEEE 1588)
- Hardware verification of network processors (NAND flash controller/ONFI)
- Championed methodology improvements for quality (assertions)
- **Technologies used:** TestBuilder (C++ library), Verilog, Cadence NCSim, SVA

Texas Instruments   **October 2003 – March 2008**
Design Verification Lead   *Dallas, TX*
- Hardware verification of VLIW DSPs & SoCs (DSP ISA, Low-power & DFT features)
- Led project to improve product delivery for the Guinness Book of World Record winning 1GHz DSP. Reduced test times by 2s per test insertion for an overall savings of 3.09 months of tester time per million parts
- **Technologies used:** Specman e, C, C++, Perl, Synopsys VCS

Intrinsix   **March 2001 – October 2003**
Design Engineer   *Westborough, MA*
- Design and Verification Consultant for ASIC and FPGA development
- Hardware verification for ARM-based Authentication SoCs, Digital Test Controller FPGA for MEMS test systems, RISC cores

- Hardware design for telephony/switch ASIC
- **Technologies used:** Specman e, OVM, C, VMM/Vera/NTB

Immersive Technologies
June 2000 – January 2001

Design Engineer
Malden, MA

- Computer Graphics start-up with proprietary hardware/software technology accelerating computer image generation to minutes instead of hours
- Developed and implemented a 'beam traversal' algorithm in C++ for finding geometry in the path of a beam, to replace the traditional ray tracing algorithms used for rendering in computer graphics. Resulted in a 3-5x speed-up in the image generation time
- **Technologies used:** C++

Education

Carnegie Mellon University
Aug. 1998 – May 2000

Master of Science in Electrical & Computer Engineering
Pittsburgh, PA

Indian Institute of Technology (IIT), Madras
Aug. 1994 – May 1998

Bachelor of Technology in Electrical Engineering
Chennai, India