Aseem Maheshwari

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Technical Skills

Languages: Python, C/C++, HTML/CSS, JavaScript, SQL, Verilog, SystemVerilog
Libraries/Frameworks: Scikit-Learn, Numpy, Pandas, BeautifulSoup, Matplotlib, Seaborn, React, Node.js, Gatsby, Flask, Tensorflow, Dash, SystemC, UVM
Big Data & ML: Data Visualization, Data Analytics, Statistics, Data Science Pipeline (cleansing, wrangling, visualization, modeling, interpretation)
Misc: Docker, Git, Jenkins

Projects

Data Analytics & Visualization | *Python, Numpy, Pandas, Matplotlib, Seaborn*

- Utilized python to do exploratory data analysis of bank stock prices, and see how they progressed through the financial crises to early 2016.
- Analyzed 911 call data from Kaggle

ML Models | *Python, Scikit-Learn, Numpy, Pandas, Matplotlib, Seaborn*

- Created a linear regression model to predict where a company should focus its effors for better customer yearly spend.
- Created a logistic regression model to predict ad click-throughs.
- Using data from Lending Club, created a Decision Tree model and Random Forest model to predict customers with a high probability of paying back loans.

Experience

Palo Alto Networks **June 2012 – Present**
Sr. Principal Engineer, ASIC Engineering *Santa Clara, CA*

- Hardware verification of complex ASICs used in firewalls (ACL, Forwarding, Packet-edit Engines, QoS features, Microcontroller ISA, Ethernet, Interlaken)
- Managed a team of 15+ engineers as well as worked as an individual contributor
- Championed methodology improvements for quality (formal, emulation) and schedule improvements
- **Technologies used:** UVM, SystemVerilog, Python, SystemC

Seagate (formerly SandForce, LSI, Avago) **July 2011 – June 2013**
Principal Engineer *Milpitas, CA*

- Hardware verification of flash storage processors (PCIe, AHCI, NVMe, DMA Engines)
- **Technologies used:** UVM, SystemVerilog, C

Marvell (formerly Cavium) **March 2008 – July 2011**
Principal Engineer *Marlborough, MA*

- Hardware design of network processors (DDR3 controller, Add-work engines, Full chip integration, IEEE 1588)
- Hardware verification of network processors (NAND flash controller/ONFI)
- Championed methodology improvements for quality (assertions)
- **Technologies used:** TestBuilder (C++ library), Verilog, SVA

Texas Instruments **October 2003 – March 2008**
Design Verification Lead *Dallas, TX*

- Hardware verification of VLIW DSPs & SoCs (DSP ISA, Low-power & DFT features)
- Led project to improve product delivery for the Guinness Book of World Record winning 1GHz DSP. Reduced test times by 2s per test insertion for an overall savings of 3.09 months of tester time per million parts
- **Technologies used:** Specman e, C, C++, Perl

Intrinsix **March 2001 – October 2003**
Design Engineer *Westborough, MA*

- Design and Verification Consultant for ASIC and FPGA development
- Hardware verification for ARM-based Authentication SoCs, Digital Test Controller FPGA for MEMS test systems, RISC cores
- Hardware design for telephony/switch ASIC
- **Technologies used:** Specman e, OVM, C, VMM/Vera/NTB

Immersive Technologies **June 2000 – January 2001**

Design Engineer *Malden, MA*

- Computer Graphics start-up with proprietary hardware/software technology accelerating computer image generation to minutes instead of hours
- Developed and implemented a 'beam traversal' algorithm in C++ for finding geometry in the path of a beam, to replace the traditional ray tracing algorithms used for rendering in computer graphics. Resulted in a 3-5x speed-up in the image generation time
- **Technologies used:** C++

Education

Carnegie Mellon University **Aug. 1998 – May 2000**

Master of Science in Electrical & Computer Engineering *Pittsburgh, PA*

Indian Institute of Technology (IIT), Madras **Aug. 1994 – May 1998**

Bachelor of Technology in Electrical Engineering *Chennai, India*