**Q \ What are the essential in memory write and read operations ? how can perform write and read operations ?**

**Sol** \ Two registers are essential in memory write and read operations, the Memory Data Register (**MDR**) and Memory Address Register (**MAR**).

**a write operation**

**1**. The word to be stored into the memory location is first loaded by the CPU into MDR.

**2**. The address of the location into which the word is to be stored is loaded by the CPU into a MAR.

**3**. A write signal is issued تصدر by the **CPU**

**read operation**

**1**. The address of the location from which the word is to be read is loaded into the MAR.

**2**. The required word will be loaded by the memory into the MDR ready for use by the CPU.

**3**. A read signal is issued by the **CPU**.

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## Q \ What are the main registers in fetching an instruction for execution ?

Two main registers are involved in fetching an instruction for execution: the program counter **(PC)** and the instruction register **(IR).** The PC is the register that contains the address of the next instruction to be fetched. The fetched instruction is loaded in the IR for execution. After a successful instruction fetch, the PC is updated to point to the next instruction to be executed.

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## Q \ What is a bus ? what are the bus types in computer system ?

**A bus** : is a group of parallel wires that transfer data from one part of the computer to another **(data, I/O, control, and address)**

Microprocessors are regarded as one of the most important devices in our everyday machines called computers

المايكرو بروسيسر :يشير إلى واحد من أهم الأجهزه الموجوده في الكمبيوتر .

Microprocessor is an electronic circuit that functions as the central processing unit (CPU) of a computer, providing computational control. Microprocessors are also used in other advanced electronic systems, such as computer printers, automobiles, and jet airliners

المايكرو بروسير : هو دائرة الكترونيه وظيفتها كـ وحدة المعالجه المركزيه تسيطر على الحسابات . تستخدم في انظمة الكترونيه متقدمه مثل طابعات الكمبيوتر , المركبات,طائرات خطوطً وأيضا النقل الجوي

Typical microprocessors incorporate arithmetic and logic . رياضي ومنطقيً انواع المايكرو بروسيسر نموذجيا

Microprocessors are classified by the semiconductor technology of their design (TTL (transistor-transistor logic); CMOS (complementary-metaloxide semiconductor), or ECL (emitter-coupled logic)

المايكرو بروسيسر يصنف الى :

TTL: transistor-transistor logic

CMOS :complement-metal-oxide semiconductor

ECL :emitter-coupled logic

(ENIAC): Electronic Numerical Integrator and Computer.

TTL technology is most commonly used, while CMOS is favored for portable computers.

TTL هو الشائع الاستخدام بينما

Cmos هو المفضل في الكمبيوتر المحمول

CMOS is favored for portable computers and other battery-powered devices?

Because of its low power consumption.

Cmos هو المفضل في الكمبيوتر المحمول الحاوي للبطاريه ؟ :

ج /بسبب قلة استهلاكه للطاقه .

ECL is used where the need for its greater speed offsets the fact that it consumes the most power

ECL يستخدم عند الحاجه الى سرعة ازاحه كبيره وفي الحقيقه ذلك يستهلك معظم الطاقه:

 The register set can divide to :  General–purpose set registers : which use for any purpose Special–purpose set registers: has specific function within CPU such as program counter (PC), instruction registers (IR), segment register, stack pointer.

الرجيستر يقسم الى نوعين

1 – . مجاميع الرجيستر ذات الغرض العام: تستخدم لاي غرض

مجاميع الرجيستر ذات الغرض الخاص : وظيفتها داخل وحدة المعالجه المركزيه مثل عداد البرنامج, 2 – مسجل الايعازات , مسجل الجزء, مؤشر الستاك

 ALU performs the arithmetic, logic and shift operations  CU is responsible for fetch the instruction to be executed from main memory and decoding and executing it. : مسؤوله عن الحسابات والعمليات المنطقيهALU

CU مسؤول عن جلب الايعازات لتنفيذها من الذا : كره الرئيسيه وفك الشفره وتنفيذها

Registers are essentially extremelyضروري جداfast memory locations within the CPU that are used to create and store the results of CPU operations and other calculations

Address registers may be dedicated مكرس to a particular معين addressing mode or may be used as address general purpose. Address registers must be long enough to hold the largest address

عنوان الرجيستر ربما يكون يشير الى عنوان او ربما يستخدم لغرض عام , عنوان الرجيستر يجب ان يكون طويل وكافي لتحمل أكبر عنوان

Memory Access Registers:

Two registers are essential in memory write and read operations, the Memory Data Register (MDR) and Memory Address Register (MAR). The MDR and MAR are used exclusively by the CPU and are not directly accessible to programmers

مسجل مدخل الذاكره في الذاكره هي عمليات القراء والكتابه , مسجل بياناتً : مسجلات اثنين اساسيا غي قابل للدخولً من خلال المعالج وليس مباشرةً الذاكره ومسجل عنوان الذاكره وتيستخدم كلاهما حصرا للبرامج .

In order to perform a write operation into a specified memory location, the MDR and MAR are used as follows:

1. The word to be stored into the memory location is first loaded by the CPU into MDR. 2. The address of the location into which the word is to be stored is loaded by the CPU into MAR. 3. A write signal is issued تصدر by the CPU.

عملية القراءه

1 – . في مسجل بيانات الذاكرهً الكلمه تخزن في موقع الذاكره تكون الاول تحميلا

2 – عنوان الموقع حيث الكلمه تخزن وتحمل بواسطه المعالج الى مسجل عنوان الذاكره

3 – اشارة الكتابه تصدر بواسطة المعالج

Similarly, to perform a memory read operation, the MDR and MAR are used as follows:

1. The address of the location from which the word is to be read is loaded into the MAR. 2. A read signal is issued by the CPU. 3-The required word will be loaded by the memory into the MDR ready for use by the CPU

عمليات القراءة

1 – ه ل الى مسجل عنوان الذاكر َمَحُ قرأ وتُ عنوان موقع حيث الكلمه ت

2 – اشارة الكتابه تصدر بواسطة المعالج

3 – ل بواسطة الذاكره الى مسجل بيانات الذاكره للقراءة بواسطة المعالجَ حمُ الكلمة المطلوبه سوف ت

Instruction Fetching Registers:

Two main registers are involved in fetching an instruction for execution: the

program counter (PC) and the instruction register (IR). The PC is the register that

contains the address of the next instruction to be fetched

Q / what are the register essential in memory write and read operations?

How can perform write and read operation ? Sol / the Memory Data Register (MDR) and Memory Address Register (MAR) are used

exclusively by the CPU and are not directly accessible to programmers.

Q / what are mmx register and where used? which different from xmm register ? Sol / MMX technology was added onto the Pentium processor by Intel to improve the

performance of advanced multimedia and communications applications. The eight 64-bit MMX

registers support special instructions called SIMD

XMM rigisterThe x86 architecture also contains eight 128-bit registers called XMM

registers. They are used by streaming SIMD extensions to the instruction set.

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Q / how can X86 processor access to the memory in real address mode ?

Sol \ In real-address mode, an x86 processor can access 1,048,576 bytes of memory (1 MByte) using 20-bit addresses in the range 0 to FFFFF hexadecimal.

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Q / what is the control level ? what are ways of control units can be designed?

Sol / Control Level, is where a control unit makes sure that instructions are decoded and

executed properly and that data is moved where and when it should be.

Control units can be designed in one of two ways: They can be hardwired or they can be

microprogrammed.

Q / what are the main register in fetching an instruction for execution ?

Sol / instruction register (IR) and program counter (PC).

Q / why interrupt can be masked ? what is the action taken when maskable interrupt

activated ?

Sol / . If the interrupts are disabled using clear interrupt Flag instruction, the microprocessor

will not get interrupted even if INTR is activated. That is, INTR can be masked. INTR is a non

vectored interrupt, which means, the 8086 does not know where to branch to service the

interrupt

The action taken is as follows:

1. Complete the current instruction. 2. Activates INTA output, and receives type Number, say N 3. Flag register value, CS value of the return address & IP value of the return address are pushed on to the stack. 4. IP value is loaded from contents of word location N x 4. 5. CS is loaded from contents of the next word location. 6. 2 Interrupt Flag and trap Flag are reset to 0. ———————————————————————————————————

Q / what are the following sentence cash memory in its various forms , plays a

particularly important role in processor performance ?

sol / Cache can improve a processor’s efficiency by offering it access to the data it

needs more quickly than regular memory would. Not only are cache memory chips (typically Static Random Access Memory, or SRAM) faster than regular memory chips, but they also have a faster connection to the processor.

---

Q / what is programmable interrupt controller chip ? drown how a typical pc

uses device to provide interrupt inputs ?

sol / The 8259A programmable interrupt controller chip accepts interrupts from up to eight

different devices.

A typical PC uses two of these devices to provide 15 interrupt inputs (seven on the master PIC

with the eight input coming from the slave PIC to process its eight inputs)7. The sections

following this one will describe the devices connected to each of those inputs.

Q / What are the difference between web browser and microprocessor caches ?

Sol / Processors aren't the only computer-related component to use a cache. Many software programs, such as Web browsers, also use a cache While a processor's cache and a browser's cache are not the same thing, they are conceptually similar. For both components, a cache speeds up access to recently used information. Web browsers, for example, set up memory and/or disk caches

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Q / فراغات

1- any instruction issued by the processor must carry at least two types of information

instruction queu and IP.

2- the primary sources of interrupts connect to an intel 8259A

3- in direct mode the operand of instruction represent address of memory location .

4- relative mode is the same as indexed addressing except program counter (PC).

5- interrupt instruction with type number is a two byte instruction , the first provides the

OP-code and second byte interrupt type number.

6- Any instruction issued by the processor must carry at least two types of

information op-code field and address field.

7- The 80x86 provides a 256 entry interrupt vector table beginning at address 0:0 in

memory

8- The control unit decodes the instruction’s function to determine

9- In response to the second INTA the microprocessor receives the 8 bit, say N, from a programmable Interrupt controller.

التعاريف Latency : is defined as the time interval between the request for information and access to

the first bit of that information.

Store output operand : if the output operand in memory the control unit uses a write

operation to store data.

Back side bus : a microprocessor bus that connects the cpu to level 2 cash, typically aback

side bus runs at faster clock speed than to front side bus that connects cpu to main memory.

GDT : in the flag segmentation model at least two segments are required one for code and

one for data each segment is defined by by a segment descriptor , a 64 bit called glopal

dedcriptor table (GDT).

Break point interrupt : when a break point inserted the system executes the instructions

up to the break point and then goes to break point procedure.

One and half –address instruction : take the form operation dd1, add2, one refers to a register and other refers to memory and vice versa. Direct mode address : the operand of instruction represent address of the memory

location that holds the operand.

Fetch operands : If the instruction uses an input operand located in memory, the control

unit uses a read operation to retrieve the operand and copy it into internal registers.

Paging : is important solution to vexing problem software and hardware designer.

Op-code field : any instruction issued by the processor must carry at least two type of

information.

Local descriptor table ( LDT) : in the multi- segment model , each task or program is given

its own table of segment descriptors , called a local descriptor table (LDT).