USART

USART - Universal synchronous asynchronous receiver transmitter:

- STM32F407xx cihazında 4 USART, 2 UART bulunmaktadır.
- USART ile seri veri iletimi yapılır: 1 zaman diliminde 1 bit iletilmesi
- STM32F4 cihazlarında senkron veya asenkron iletim yapılabilir.
- Senkrondan kasıt USART ile birlilte clock sinyalinin de gönderilmesidir.
- Full duplex veri iletimi yapabilir: Aynı anda veri gönderip alabilme.
- 8 veya 16 bit aşırı örnekleme

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- Kesirli Baud Rate üretici ile farklı hızlar ayarlanabilir.
- USART1 ve USART6 10.5 Mbit/s hızında diğerleri 5.25 MBit/s hızında iletişim arayüzüne sahiptir.
- Veri uzunluğu8 veya 9 bit olarak, Stop biti 1 veya 2 bit olarak ayarlanabilir.
- Kızılötesi, akıllı kart desteği vardır.
- Tek bir iletişim kanalı ile half duplex olarak çalışabilir.
- DMA ile alınan veya gönderilecek veri için SRAM kullanılabilir.
- Parite biti göddderebilir ve kontrol edebilir. Hata olması durumunda interrupt üretebilir.

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Herhangi 2 yönlü (bidirectional) iletişim en az 2 pin kullanır:
1. RX: Receive Pin: Alıcı
Veriden gürültünün ayrıştırılması için oversampling kullanılır.
2. TX: Transmitter Pin: Verici
Bu pin aktifleştirildiğinde ve herhangi bir iletim olmadığında yüksek seviyede bulunur.

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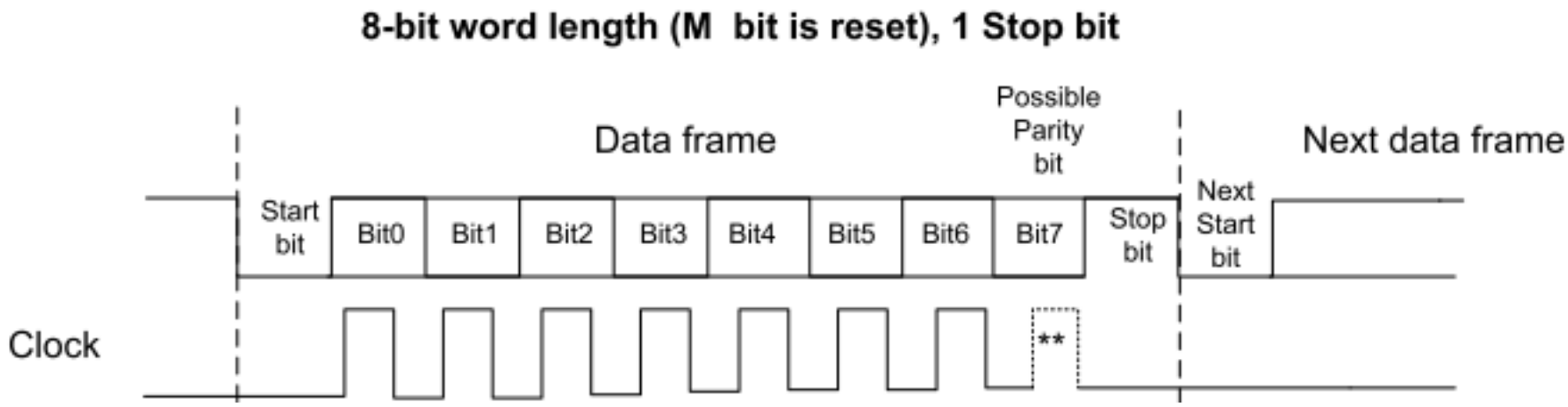
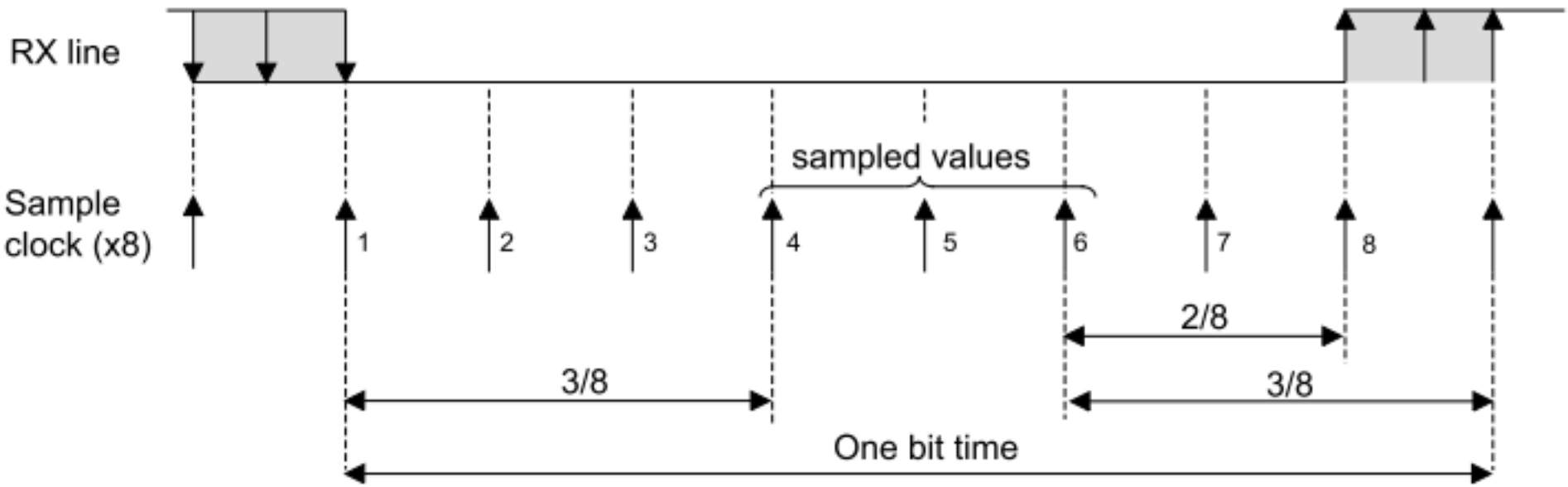


USART veri iletimi şu şekilde olur:

1. Bekleme durumu
2. Başlama biti
3. Düşük değerlikli önce bitler önce olmak üzere 8 veya 9 bit veri,
4. Stop biti

Data sampling when oversampling by 8



Oversampling 8 olarak seçilirse (OVER8=1) daha yüksek hızda veri iletilebilir (maksimum fPCLK/8).
Oversampling 8 olarak seçilirse (OVER8=0) maksimum hız fPCLK/16 ile sınırlandırılır.

Baud rate generation

$$\text{Tx/Rx baud} = \frac{f_{CK}}{8 \times (2 - \text{OVER8}) \times \text{USARTDIV}}$$

USARTDIV is an unsigned fixed point number that is coded on the USART_BRR register.

- When OVER8=0, the fractional part is coded on 4 bits and programmed by the DIV_fraction[3:0] bits in the USART_BRR register
- When OVER8=1, the fractional part is coded on 3 bits and programmed by the DIV_fraction[2:0] bits in the USART_BRR register, and bit DIV_fraction[3] must be kept cleared.

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Baud rate hesap örnekleri (OVER8=0):
Örnek 1:
BRR yazmacında 0x1BC var ise tam kısım 0x1B=27
Kesirli kısım: 0xC: $12 \times 16^{-1} = 0.75$
USARTDIV=27.75
Örnek 2:
USARTDIV=25.62 ise Tam kısım: 25=0x19
Kesirli kısım: $0.62 \times 16 = 9.92 \approx 10$ =0xA
BRR yazmacı: 0x19A dolayısıyla USARTDIV=25.625
Örnek 3:
USARTDIV=50.99 ise Tam kısım: 50=0x32
Kesirli kısım: $0.99 \times 16 = 15.84 \approx 16$ =0x10 taşan sayı tam kısma eklenir
BRR yazmacı: 0x330 dolayısıyla USARTDIV=51.00

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Baud rate hesap örnekleri (OVER8=1):
Örnek 1:
BRR yazmacında 0x1B6 var ise tam kısım 0x1B=27
Kesirli kısım: 0x6: $6 \times 8^{-1} = 0.75$
USARTDIV=27.75
Örnek 2:
USARTDIV=25.62 ise Tam kısım: 25=0x19
Kesirli kısım: $0.62 \times 8 = 4.96 \approx 5$ =0x5
BRR yazmacı: 0x195 dolayısıyla USARTDIV=25.625
Örnek 3:
USARTDIV=50.99 ise Tam kısım: 50=0x32
Kesirli kısım: $0.99 \times 8 = 7.92 \approx 8$ =0x10 taşan sayı tam kısma eklenir
BRR yazmacı: 0x330 dolayısıyla USARTDIV=51.00

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Baud rate hesabı 9600 için (OVER8=0):

$$9600 = \frac{16000000}{8 \times (2-0) \times (USARTDIV)}$$

USART 104.1666

Tam kısım 104=0x68

Kesirli kısım: 0.1666 x 16=2.67 yaklasık 3 alınır.

bu durumda BRR:0x683=104.1875 olur.

Hata %0.02

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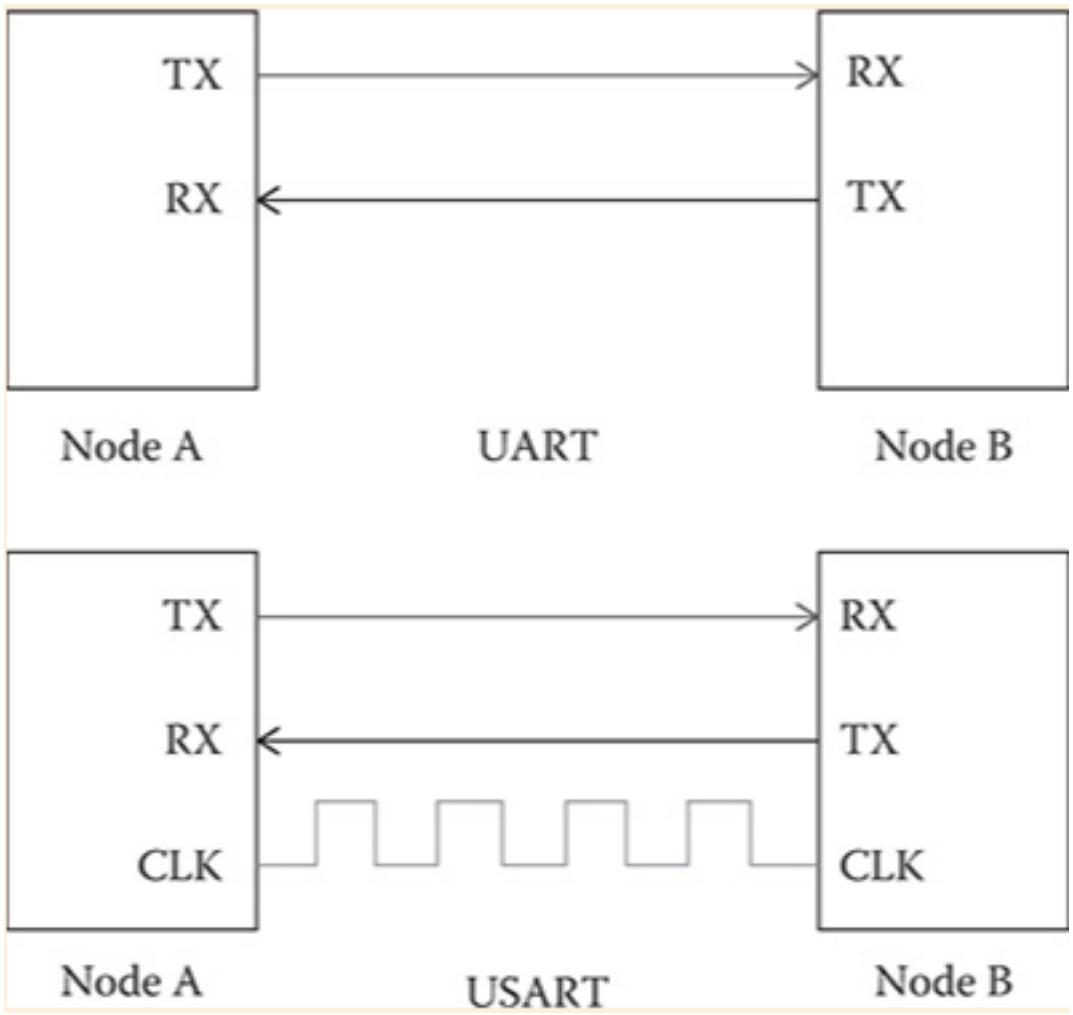
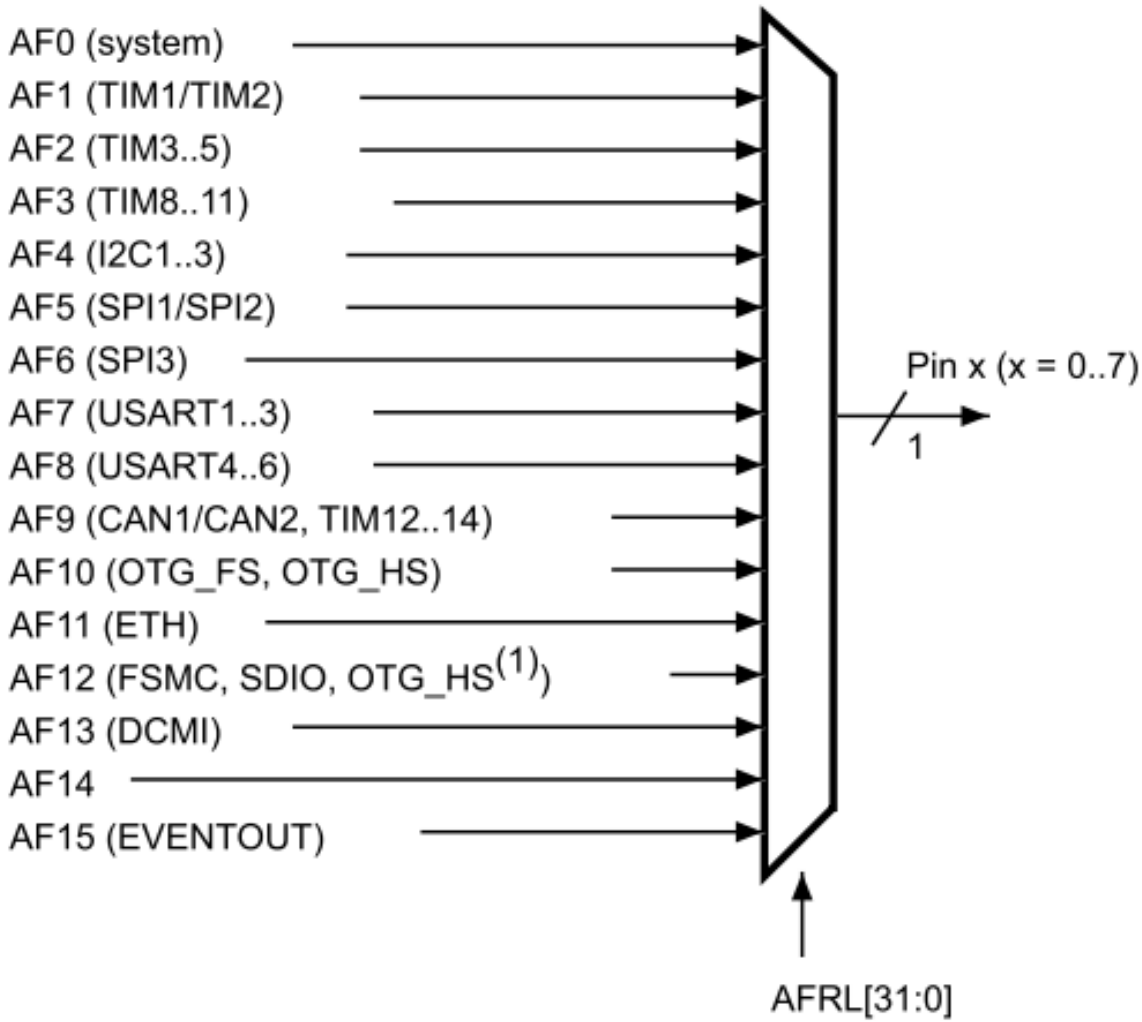

TX
RX
RX
TX
Node A
UART
Node B
TX
RX
CLK
RX
TX
CLK
Node A
USART
Node B

USART

STM32F407xx Datasheet (dm00037051.pdf)

Port		AF7
		USART1/2/3/ I2S3ext
	PA0	USART2_CTS
	PA1	USART2_RTS
	PA2	USART2_TX
	PA3	USART2_RX
	PA4	USART2_CK

RM0090 GPIOx_AFRL



Status register (USART_SR)

Address offset: 0x00

Reset value: 0x0000 00C0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						CTS	LBD	TXE	TC	RXNE	IDLE	ORE	NF	FE	PE
						rc_w0	rc_w0	r	rc_w0	rc_w0	r	r	r	r	r

Bit 7 **TXE**: Transmit data register empty

This bit is set by hardware when the content of the TDR register has been transferred into the shift register. An interrupt is generated if the TXEIE bit =1 in the USART_CR1 register. It is cleared by a write to the USART_DR register.

0: Data is not transferred to the shift register

1: Data is transferred to the shift register)

Note: This bit is used during single buffer transmission.

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Bit 6 **TC**: Transmission complete

This bit is set by hardware if the transmission of a frame containing data is complete and if TXE is set. An interrupt is generated if TCIE=1 in the USART_CR1 register. It is cleared by a software sequence (a read from the USART_SR register followed by a write to the USART_DR register). The TC bit can also be cleared by writing a '0' to it. This clearing sequence is recommended only for multibuffer communication.

0: Transmission is not complete

1: Transmission is complete

Bit 5 **RXNE**: Read data register not empty

This bit is set by hardware when the content of the RDR shift register has been transferred to the USART_DR register. An interrupt is generated if RXNEIE=1 in the USART_CR1 register. It is cleared by a read to the USART_DR register. The RXNE flag can also be cleared by writing a zero to it. This clearing sequence is recommended only for multibuffer communication.

0: Data is not received

1: Received data is ready to be read.

Data register (USART_DR)

Address offset: 0x04

Reset value: 0xXXXX XXXX

Bits 31:9 Reserved, must be kept at reset value

Bits 8:0 **DR[8:0]**: Data value

Contains the Received or Transmitted data character, depending on whether it is read from or written to.

The Data register performs a double function (read and write) since it is composed of two registers, one for transmission (TDR) and one for reception (RDR)

The TDR register provides the parallel interface between the internal bus and the output shift register (see Figure 1).

The RDR register provides the parallel interface between the input shift register and the internal bus.

When transmitting with the parity enabled (PCE bit set to 1 in the USART_CR1 register), the value written in the MSB (bit 7 or bit 8 depending on the data length) has no effect because it is replaced by the parity.

When receiving with the parity enabled, the value read in the MSB bit is the received parity bit.

Baud rate register (USART_BRR)

The baud counters stop counting if the TE or RE bits are disabled respectively.

Address offset: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIV_Mantissa[11:0]												DIV_Fraction[3:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:16 Reserved, must be kept at reset value

Bits 15:4 **DIV_Mantissa[11:0]**: mantissa of USARTDIV

These 12 bits define the mantissa of the USART Divider (USARTDIV)

Bits 3:0 **DIV_Fraction[3:0]**: fraction of USARTDIV

These 4 bits define the fraction of the USART Divider (USARTDIV). When OVER8=1, the DIV_Fraction3 bit is not considered and must be kept cleared.

Control register 1 (USART_CR1)

Address offset: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OVER8	Reserved	UE	M	WAKE	PCE	PS	PEIE	TXEIE	TCIE	RXNEIE	IDLEIE	TE	RE	RWU	SBK
rw	Res.	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit 15 **OVER8**: Oversampling mode

0: oversampling by 16

1: oversampling by 8

Bit 13 **UE**: USART enable

When this bit is cleared, the USART prescalers and outputs are stopped and the end of the current byte transfer in order to reduce power consumption. This bit is set and cleared by software.

0: USART prescaler and outputs disabled

1: USART enabled

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Bit 12 **M**: Word length

This bit determines the word length. It is set or cleared by software.

0: 1 Start bit, 8 Data bits, n Stop bit

1: 1 Start bit, 9 Data bits, n Stop bit

Note: The M bit must not be modified during a data transfer (both transmission and reception)

Bit 3 **TE**: Transmitter enable

This bit enables the transmitter. It is set and cleared by software.

0: Transmitter is disabled

1: Transmitter is enabled

Bit 2 **RE**: Receiver enable

This bit enables the receiver. It is set and cleared by software.

0: Receiver is disabled

1: Receiver is enabled and begins searching for a start bit

Control register 2 (USART_CR2)

Address offset: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	LINEN	STOP[1:0]		CLKEN	CPOL	CPHA	LBCL	Res.	LBDIE	LBDL	Res.	ADD[3:0]			
	rw	rw	rw	rw	rw	rw	rw		rw	rw	rw	rw	rw	rw	rw

Bits 13:12 **STOP**: STOP bits

These bits are used for programming the stop bits.

00: 1 Stop bit

01: 0.5 Stop bit

10: 2 Stop bits

11: 1.5 Stop bit

Note: The 0.5 Stop bit and 1.5 Stop bit are not available for UART4 & UART5.