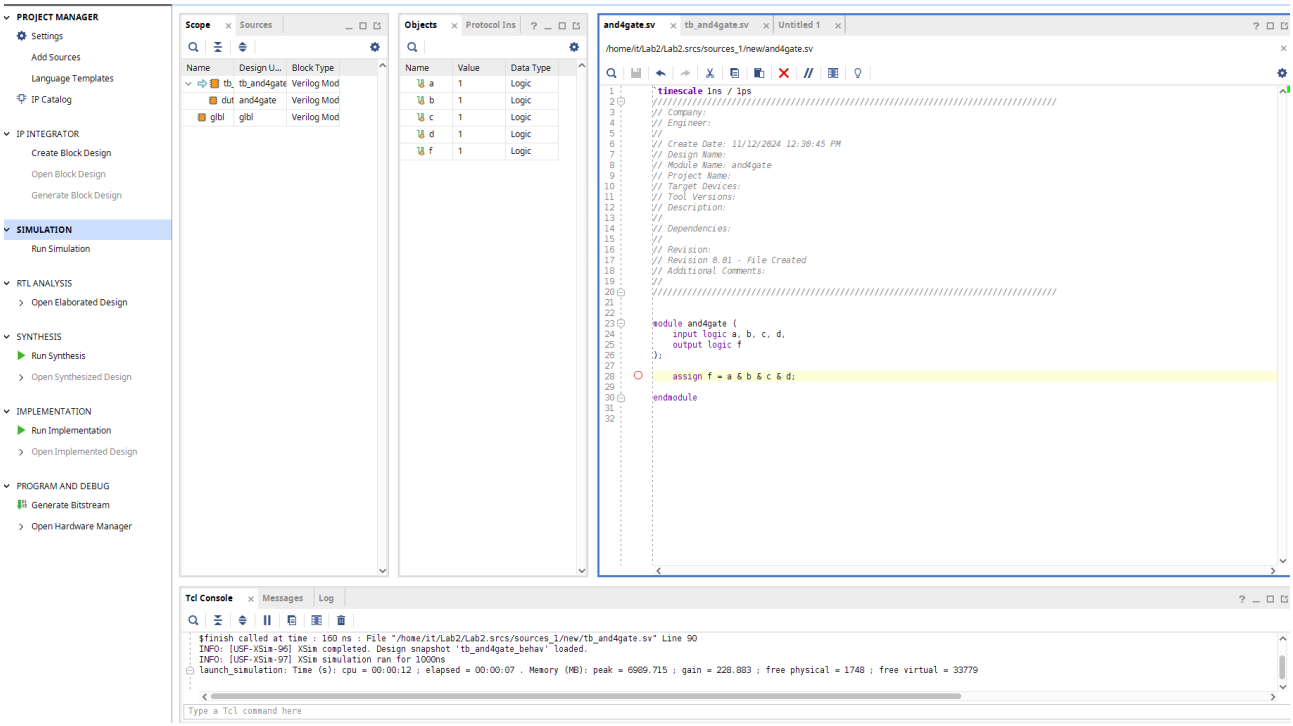
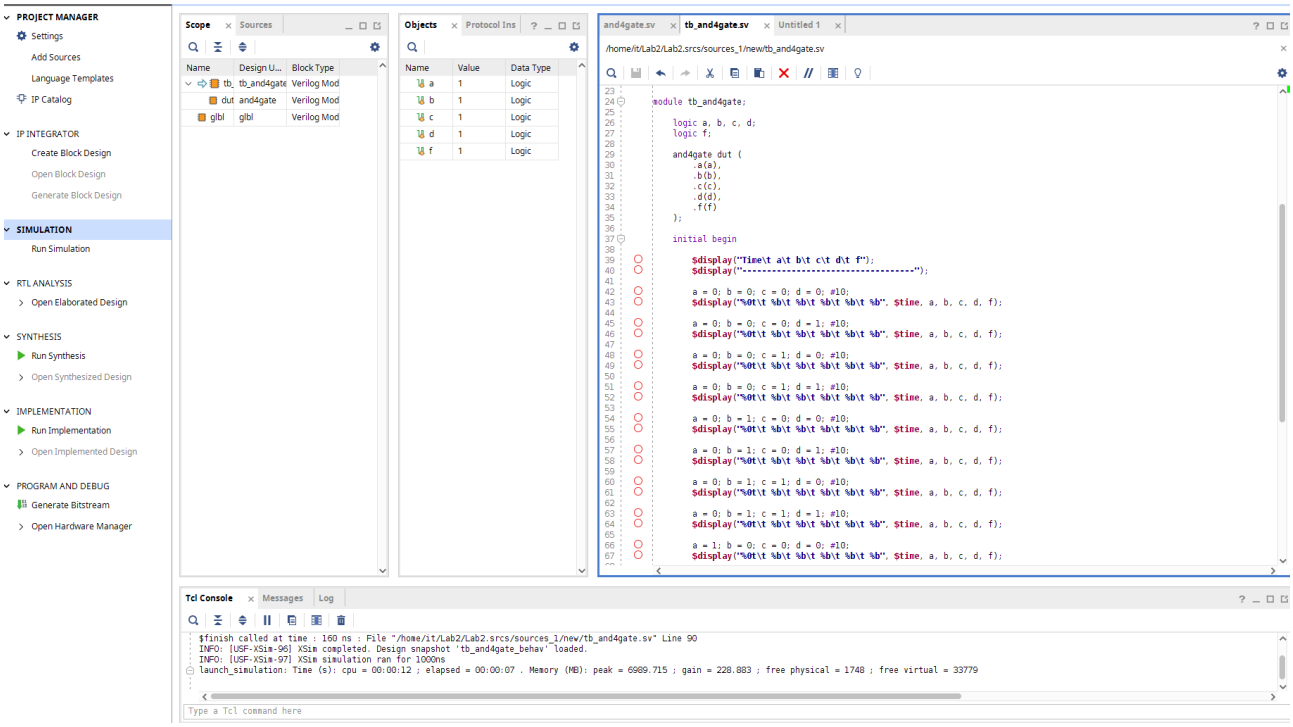
Module ID: CX-203
Post-Lab2 Write-Up
Tue, Nov 12, 2024

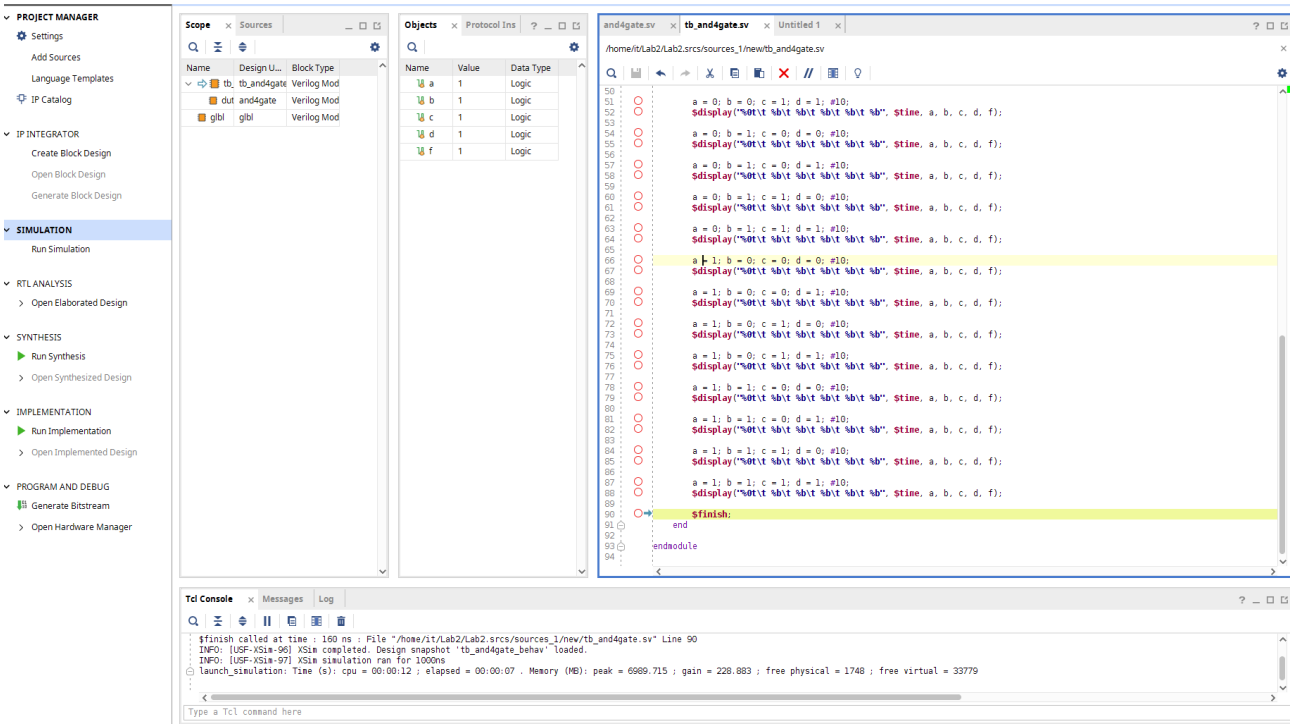
Lab 2: Combinational Circuit Design using Gate-Level Modeling and Synthesis on FPGA

GitHub URL: https://github.com/asewaket/cx-203-lab2

Task1




PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Scope
Sources
Objects
Protocol Ins
and4gate.sv
tb_and4gate.sv
Untitled 1
/home/it/Lab2/Lab2.srcs/sources_1/new/tb_and4gate.sv
Tcl Console
Messages
Log
Type a Tcl command here


PROJECT MANAGER
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Run Simulation
RTL ANALYSIS
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and4gate.sv
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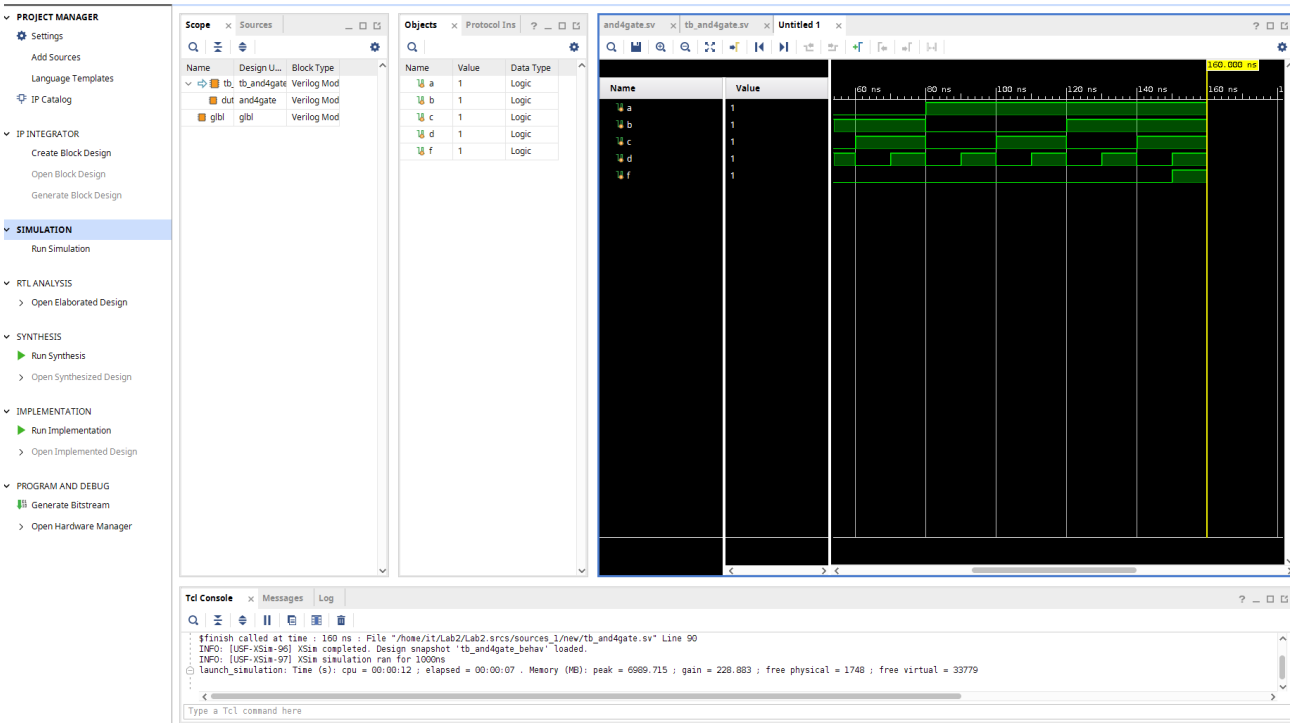
Untitled 1
/home/it/Lab2/Lab2.srcs/sources_1/new/tb_and4gate.sv
Tcl Console
Messages
Log
Type a Tcl command here


PROJECT MANAGER
Settings
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Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
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Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
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Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
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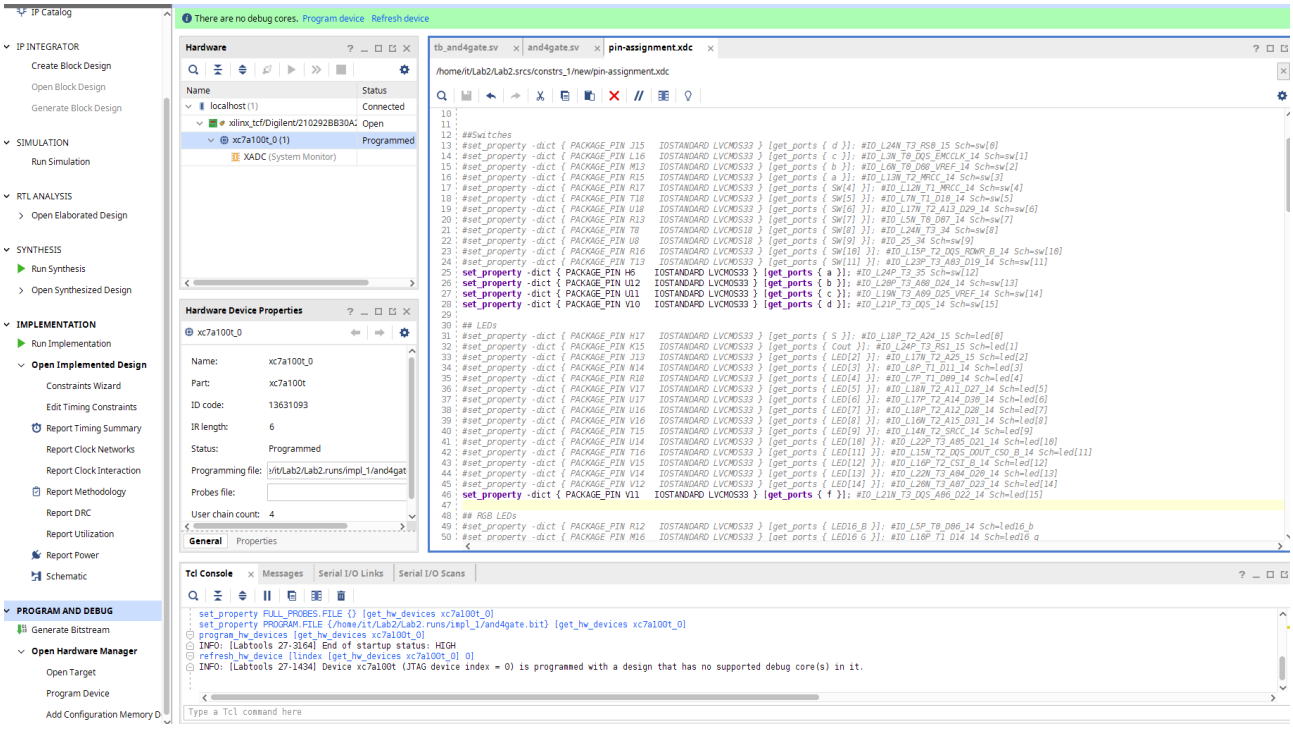
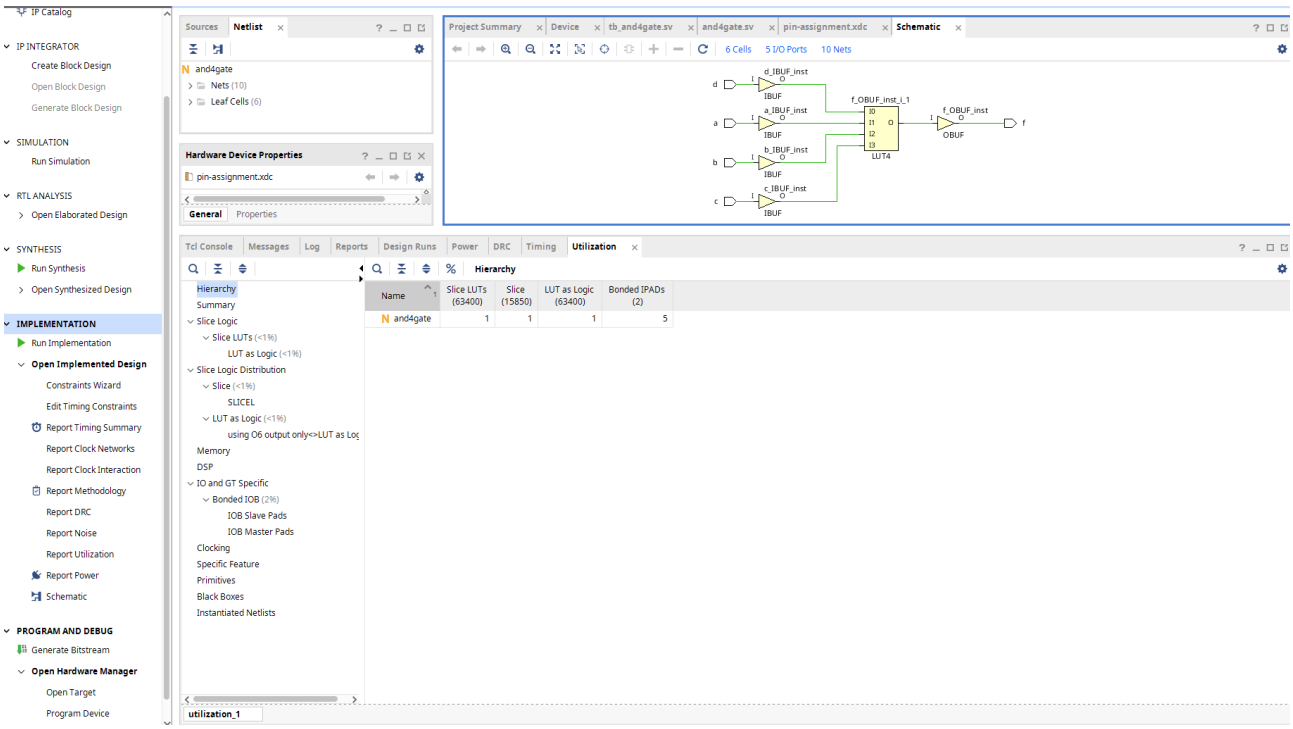
Scope
Sources
Objects
Protocol Ins
and4gate.sv
tb_and4gate.sv
Untitled 1
Tcl Console
Messages
Log
$finish called at time : 160 ns : File "/home/it/Lab2/Lab2.srcs/sources_1/new/tb_and4gate.sv" Line 90
INFO: [USF-XSim-96] XSim completed. Design snapshot 'tb_and4gate_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:12 ; elapsed = 00:00:07 . Memory (MB): peak = 6989.715 ; gain = 228.883 ; free physical = 1748 ; free virtual = 33779
Type a Tcl command here


IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Utilization
Report Power
Schematic
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Open Target
Program Device
Add Configuration Memory D
There are no debug cores. Program device Refresh device
Hardware
localhost (1)
xilinx_tcf/Digilent/210292BB30A2
xc7a100t_0 (1)
XADC (System Monitor)
Hardware Device Properties
Name: xc7a100t_0
Part: xc7a100t
ID code: 13631093
IR length: 6
Status: Programmed
Programming file: i/it/Lab2/Lab2.runs/impl_1/and4gat
Probes file:
User chain count: 4
General
Properties
tb_and4gate.sv
and4gate.sv
pin-assignment.xdc
/home/it/Lab2/Lab2.srcs/constrs_1/new/pin-assignment.xdc
Tcl Console
Messages
Serial I/O Links
Serial I/O Scans
set_property FULL_PROBES.FILE {} [get_hw_devices xc7a100t_0]
set_property PROGRAM.FILE {/home/it/Lab2/Lab2.runs/impl_1/and4gate.bit} [get_hw_devices xc7a100t_0]
program_hw_devices [get_hw_devices xc7a100t_0]
INFO: [Labtools 27-3164] End of startup status: HIGH
refresh_hw_device [lindex [get_hw_devices xc7a100t_0] 0]
INFO: [Labtools 27-1434] Device xc7a100t (JTAG device index = 0) is programmed with a design that has no supported debug core(s) in it.
Type a Tcl command here


IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
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Constraints Wizard
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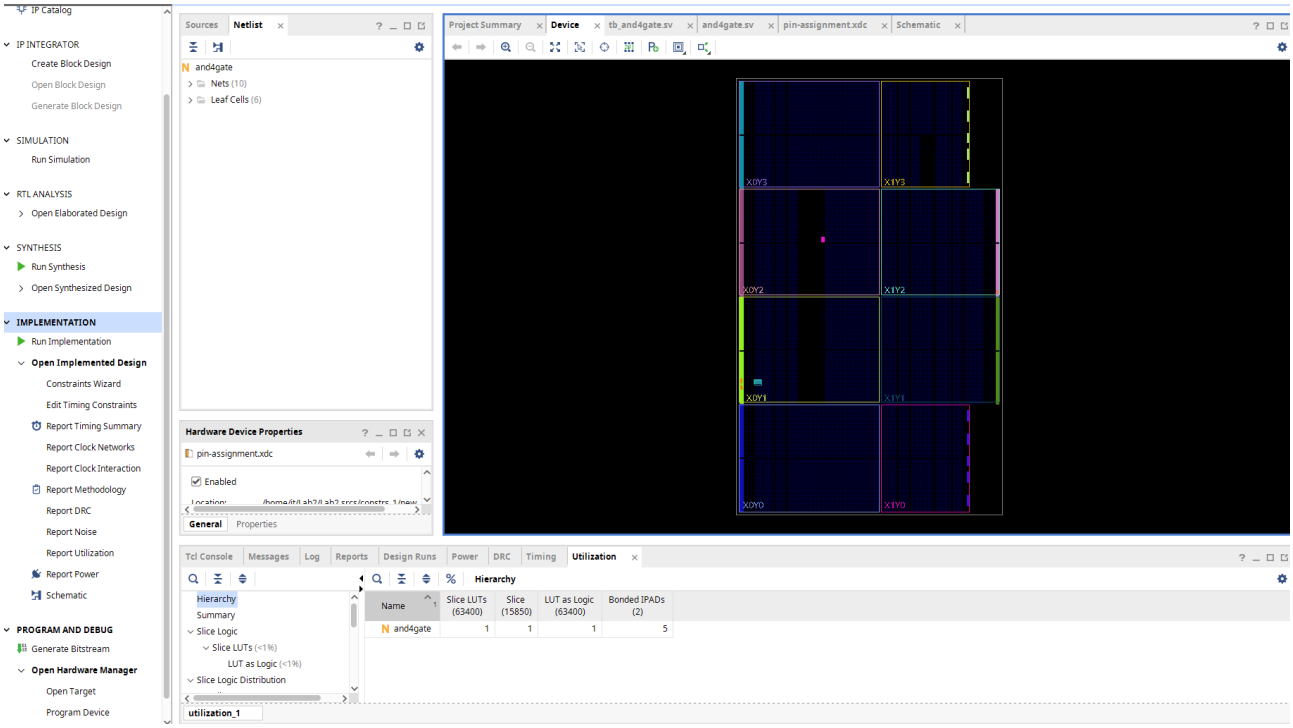
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Open Target
Program Device
Sources
Netlist
and4gate
Nets (10)
Leaf Cells (6)
Hardware Device Properties
pin-assignment.xdc
General
Properties
Project Summary
Device
tb_and4gate.sv
and4gate.sv
pin-assignment.xdc
Schematic
6 Cells
5 I/O Ports
10 Nets
d_IBUF_inst
a_IBUF_inst
b_IBUF_inst
c_IBUF_inst
IBUF
f_OBUF_inst_i_1
LUT4
f_OBUF_inst
OBUF
Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Timing
Utilization
Hierarchy
Summary
Slice Logic
Slice LUTs (<1%)
LUT as Logic (<1%)
Slice Logic Distribution
Slice (<1%)
SLICEL
LUT as Logic (<1%)
using O6 output only<>LUT as Log
Memory
DSP
IO and GT Specific
Bonded IOB (2%)
IOB Slave Pads
IOB Master Pads
Clocking
Specific Feature
Primitives
Black Boxes
Instantiated Netlists
Name
Slice LUTs (63400)
Slice (15850)
LUT as Logic (63400)
Bonded IPADs (2)
and4gate
1
1
1
5
utilization_1


IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
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Constraints Wizard
Edit Timing Constraints
Report Timing Summary
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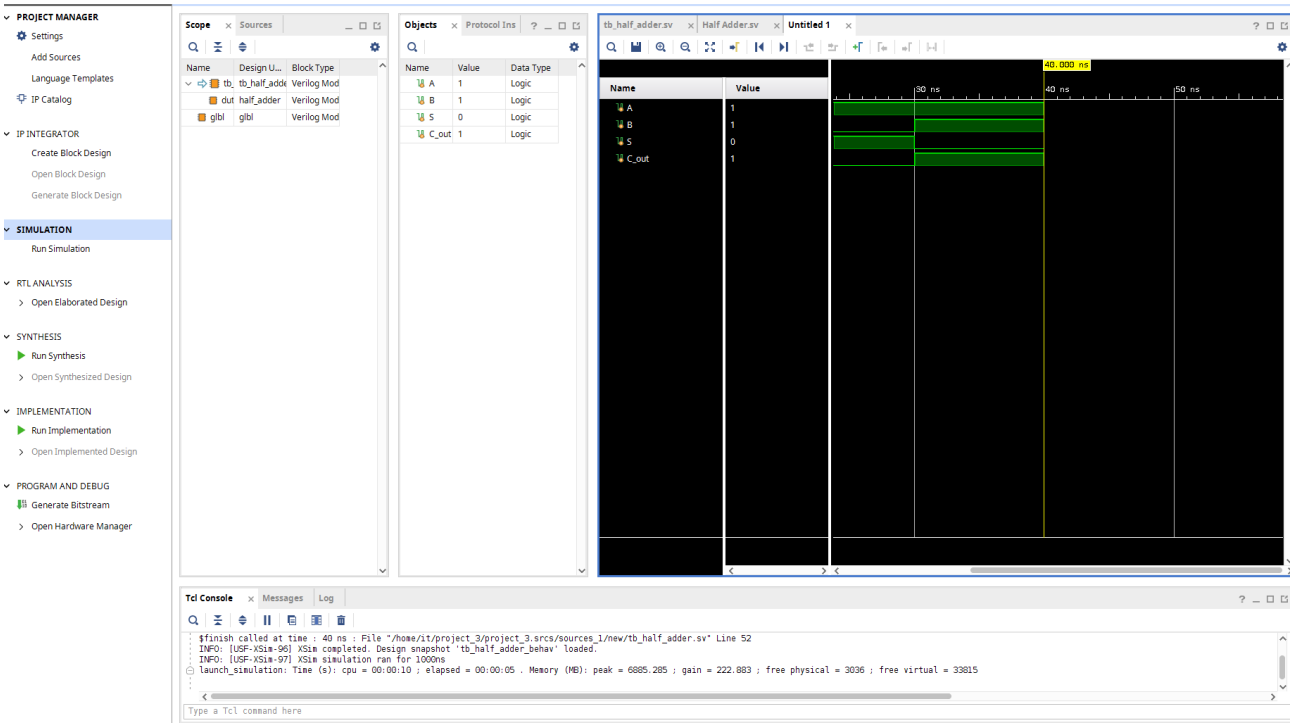
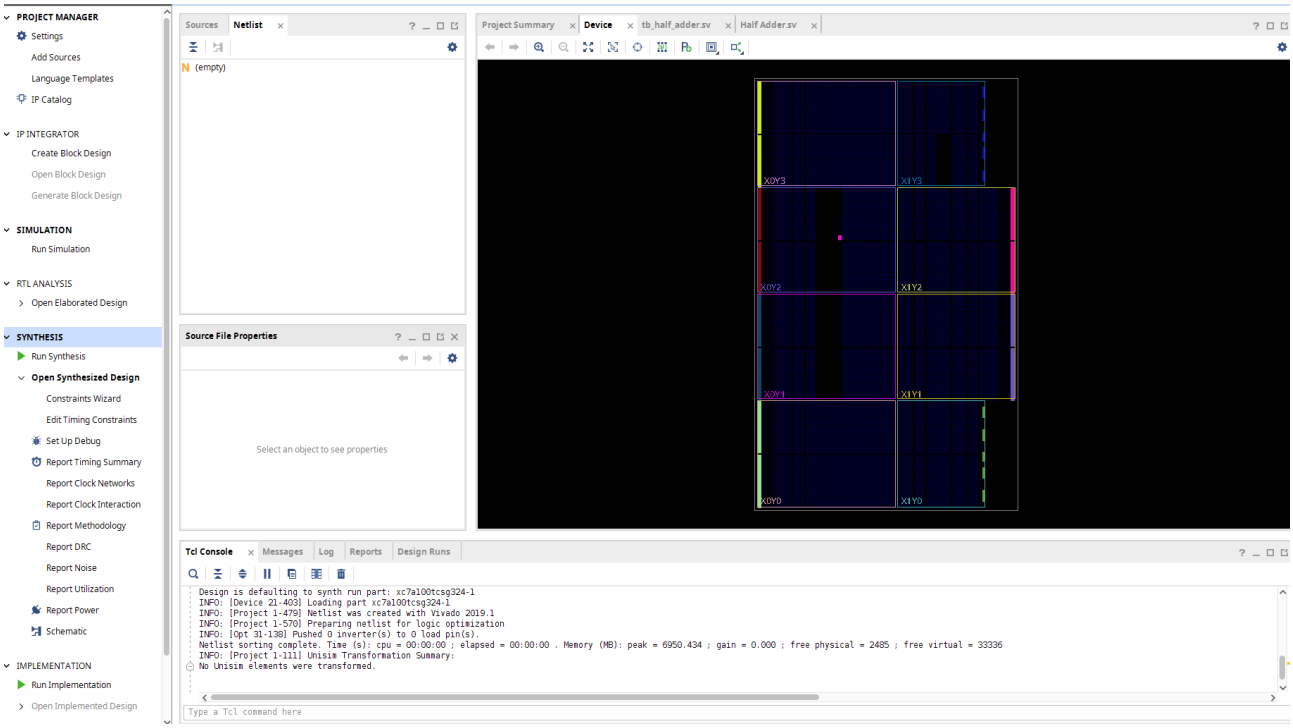
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Open Target
Program Device
Sources
Netlist
and4gate
Nets (10)
Leaf Cells (6)
Hardware Device Properties
pin-assignment.xdc
Enabled
General
Properties
Project Summary
Device
tb_and4gate.sv
and4gate.sv
pin-assignment.xdc
Schematic
X0Y3
X1Y3
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Timing
Utilization
Hierarchy
Summary
Slice Logic
Slice LUTs (<1%)
LUT as Logic (<1%)
Slice Logic Distribution
Name
Slice LUTs (63400)
Slice (15850)
LUT as Logic (63400)
Bonded IPADs (2)
and4gate
1
1
1
5
utilization_1

Task2


PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Scope
Sources
Objects
Protocol Ins
tb_half_adder.sv
Half Adder.sv
Untitled 1
Name
Value
A
B
S
C_out
40.000 ns
30 ns
40 ns
50 ns
Tcl Console
Messages
Log
$finish called at time : 40 ns : File "/home/it/project_3/project_3.srcs/sources_1/new/tb_half_adder.sv" Line 52
INFO: [USF-XSim-96] XSim completed. Design snapshot 'tb_half_adder_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:10 ; elapsed = 00:00:05 . Memory (MB): peak = 6885.285 ; gain = 222.883 ; free physical = 3036 ; free virtual = 33815
Type a Tcl command here


PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
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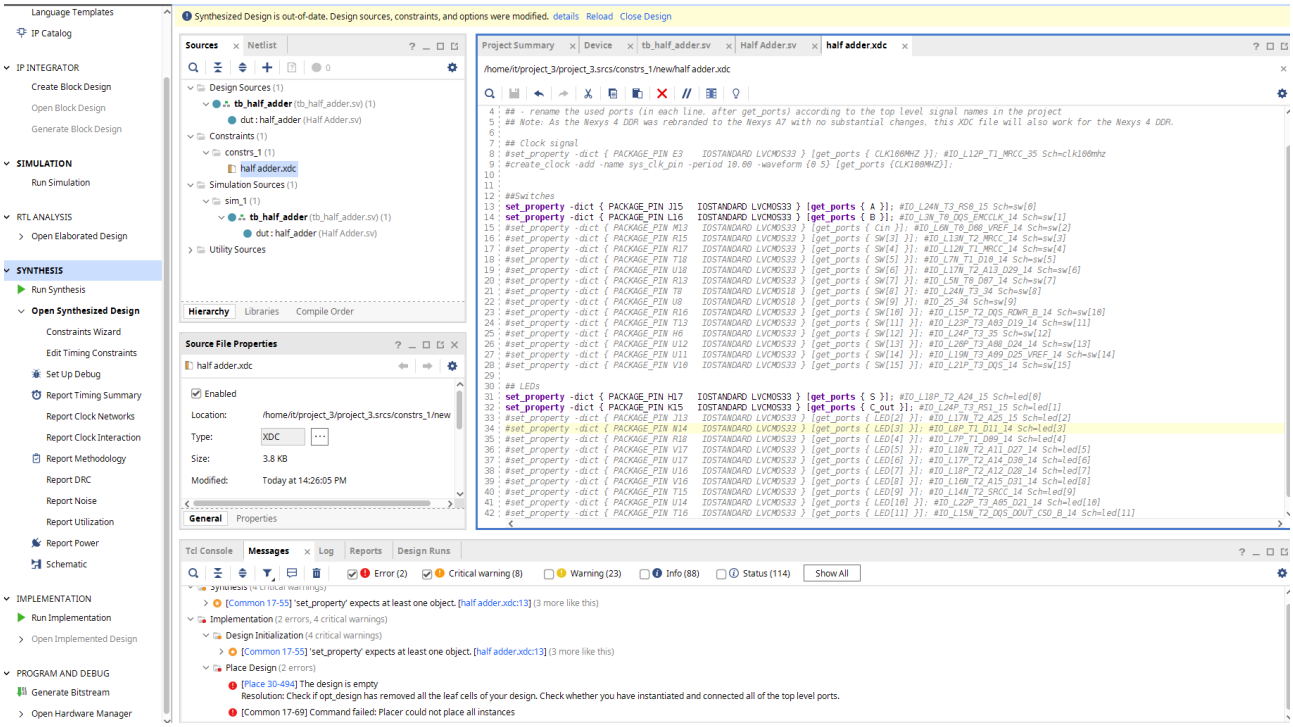
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
IMPLEMENTATION
Run Implementation
Open Implemented Design
Sources
Netlist
(empty)
Source File Properties
Select an object to see properties
Project Summary
Device
tb_half_adder.sv
Half Adder.sv
X0Y3
X1Y3
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Tcl Console
Messages
Log
Reports
Design Runs
Design is defaulting to synth run part: xc7a100tcsg324-1
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-479] Netlist was created with Vivado 2019.1
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 6950.434 ; gain = 0.000 ; free physical = 2485 ; free virtual = 33336
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
Type a Tcl command here


Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
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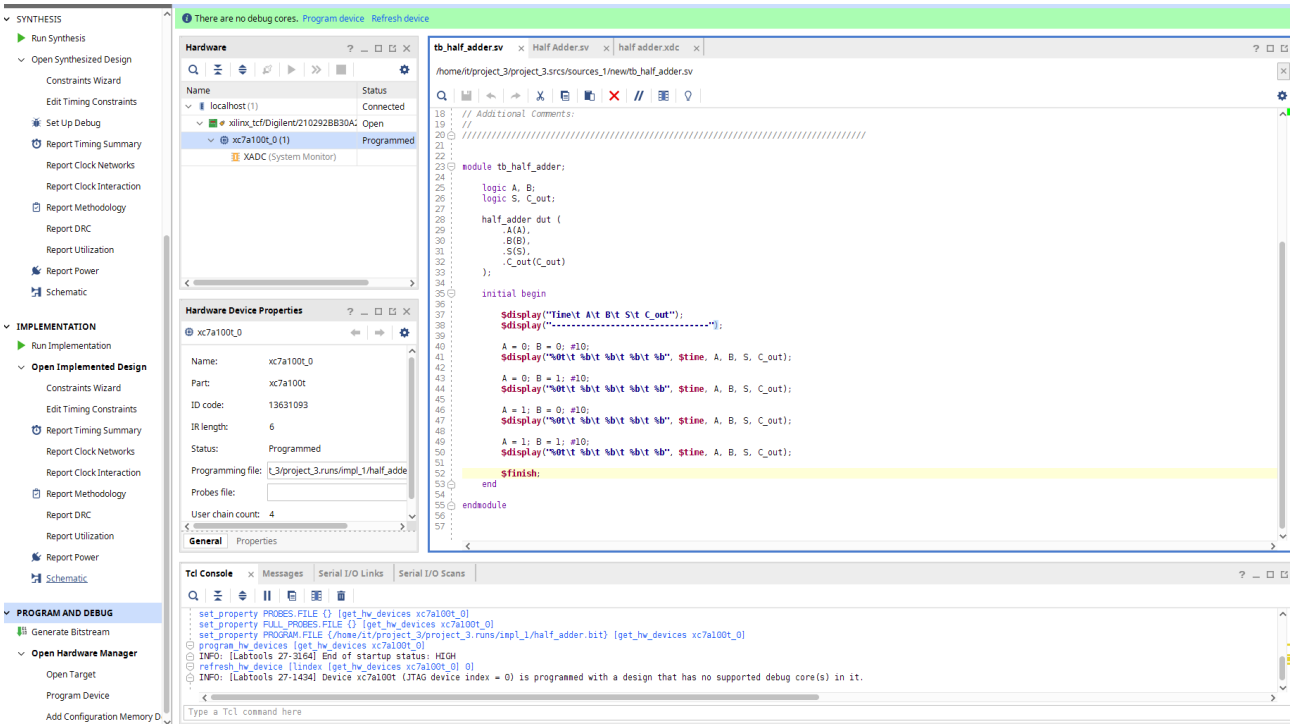
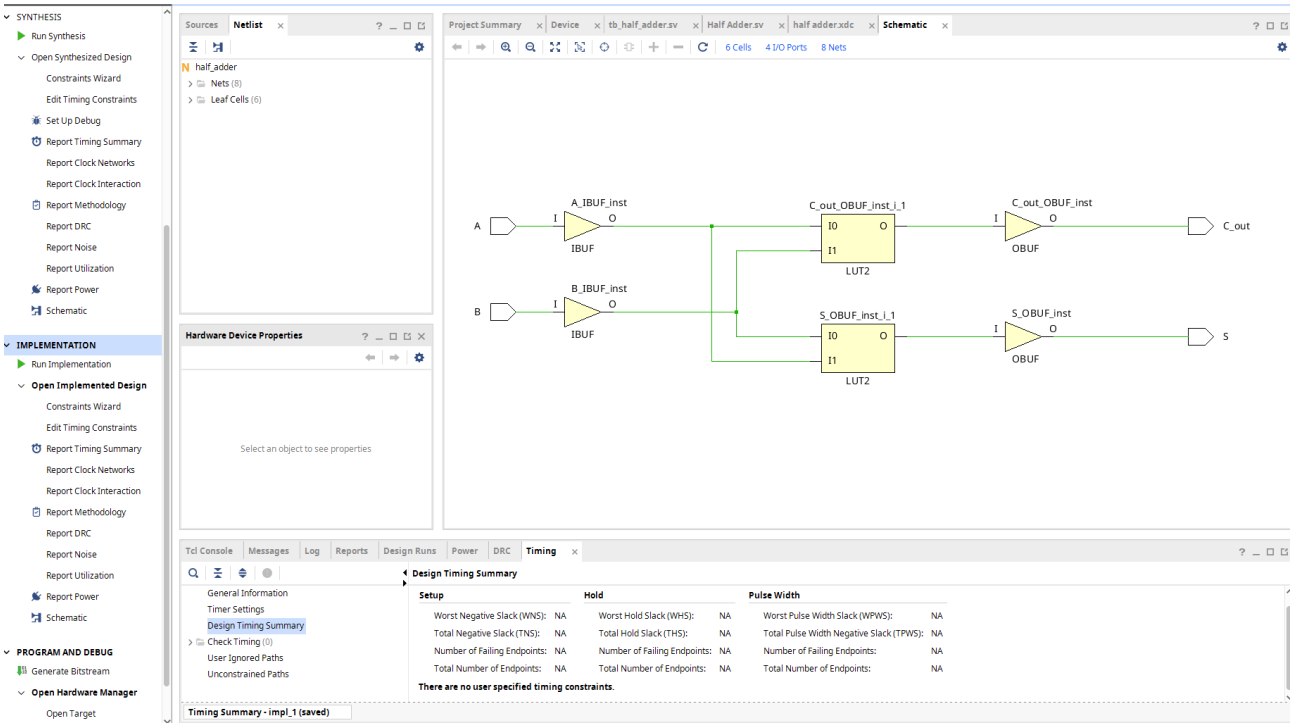
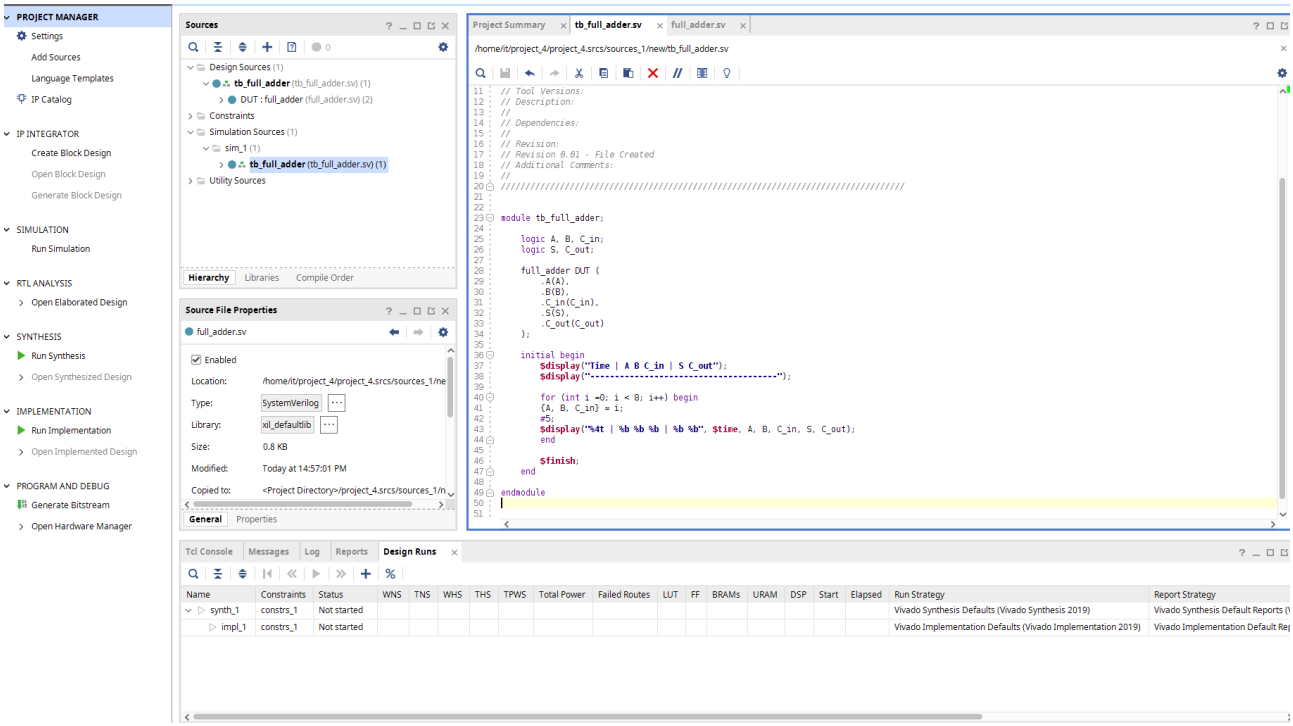
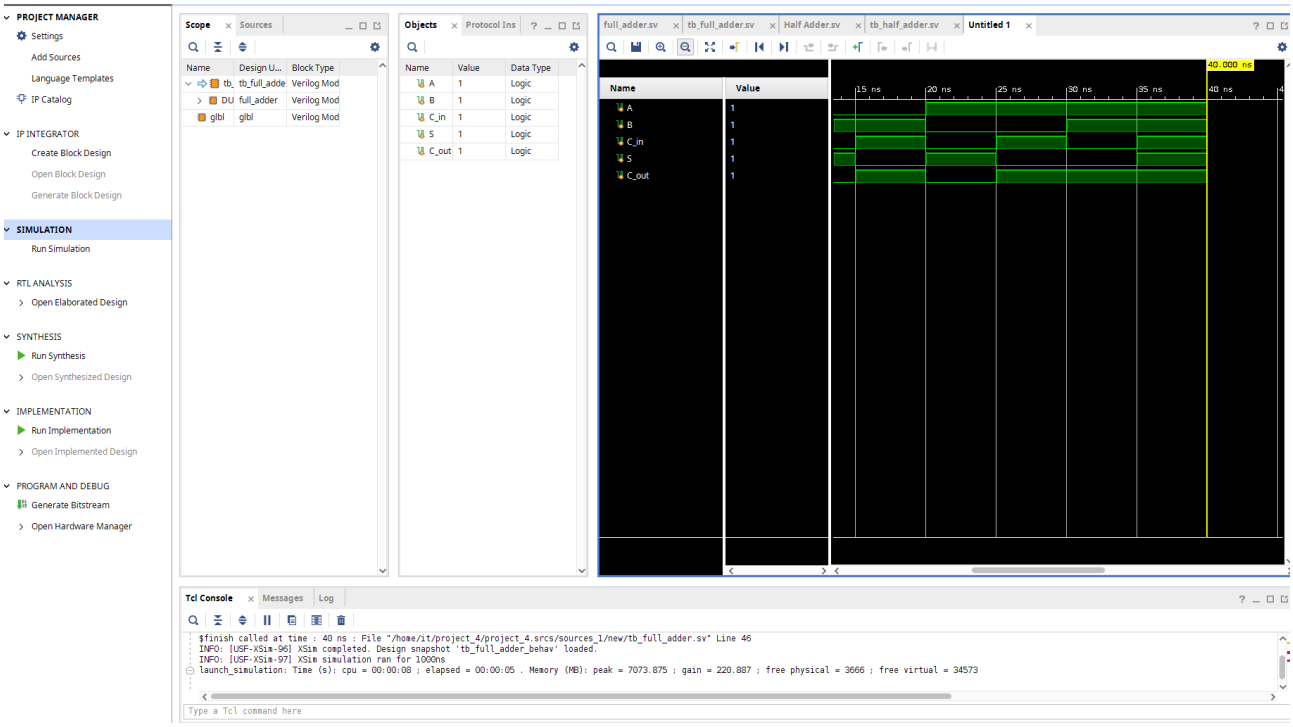
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Synthesized Design is out-of-date. Design sources, constraints, and options were modified. details Reload Close Design
Sources
Netlist
Design Sources (1)
tb_half_adder (tb_half_adder.sv) (1)
dut : half_adder (Half Adder.sv)
Constraints (1)
constrs_1 (1)
half adder.xdc
Simulation Sources (1)
sim_1 (1)
tb_half_adder (tb_half_adder.sv) (1)
dut : half_adder (Half Adder.sv)
Utility Sources
Hierarchy
Libraries
Compile Order
Source File Properties
half adder.xdc
Enabled
Location: /home/it/project_3/project_3.srcs/constrs_1/new
Type: XDC
Size: 3.8 KB
Modified: Today at 14:26:05 PM
General
Properties
Project Summary
Device
tb_half_adder.sv
Half Adder.sv
half adder.xdc
/home/it/project_3/project_3.srcs/constrs_1/new/half adder.xdc
- rename the used ports (in each line, after get_ports) according to the top level signal names in the project
Note: As the Nexys 4 DDR was rebranded to the Nexys A7 with no substantial changes, this XDC file will also work for the Nexys 4 DDR.
Clock signal
#set_property -dict { PACKAGE_PIN E3 IOSTANDARD LVCMOS33 } [get_ports { CLK100MHZ }]; #IO_L12P_T1_MRCC_35 Sch=clk100mhz
#create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports {CLK100MHZ}];
##Switches
set_property -dict { PACKAGE_PIN J15 IOSTANDARD LVCMOS33 } [get_ports { A }]; #IO_L24N_T3_RS0_15 Sch=sw[0]
set_property -dict { PACKAGE_PIN L16 IOSTANDARD LVCMOS33 } [get_ports { B }]; #IO_L3N_T0_DQS_EMCCLK_14 Sch=sw[1]
#set_property -dict { PACKAGE_PIN M13 IOSTANDARD LVCMOS33 } [get_ports { Cin }]; #IO_L6N_T0_D08_VREF_14 Sch=sw[2]
#set_property -dict { PACKAGE_PIN R15 IOSTANDARD LVCMOS33 } [get_ports { SW[3] }]; #IO_L13N_T2_MRCC_14 Sch=sw[3]
#set_property -dict { PACKAGE_PIN R17 IOSTANDARD LVCMOS33 } [get_ports { SW[4] }]; #IO_L12N_T1_MRCC_14 Sch=sw[4]
#set_property -dict { PACKAGE_PIN T18 IOSTANDARD LVCMOS33 } [get_ports { SW[5] }]; #IO_L7N_T1_D10_14 Sch=sw[5]
#set_property -dict { PACKAGE_PIN U18 IOSTANDARD LVCMOS33 } [get_ports { SW[6] }]; #IO_L17N_T2_A13_D29_14 Sch=sw[6]
#set_property -dict { PACKAGE_PIN R13 IOSTANDARD LVCMOS33 } [get_ports { SW[7] }]; #IO_L5N_T0_D07_14 Sch=sw[7]
#set_property -dict { PACKAGE_PIN T8 IOSTANDARD LVCMOS18 } [get_ports { SW[8] }]; #IO_L24N_T3_34 Sch=sw[8]
#set_property -dict { PACKAGE_PIN U8 IOSTANDARD LVCMOS18 } [get_ports { SW[9] }]; #IO_25_34 Sch=sw[9]
#set_property -dict { PACKAGE_PIN R16 IOSTANDARD LVCMOS33 } [get_ports { SW[10] }]; #IO_L15P_T2_DQS_RDWR_B_14 Sch=sw[10]
#set_property -dict { PACKAGE_PIN T13 IOSTANDARD LVCMOS33 } [get_ports { SW[11] }]; #IO_L23P_T3_A03_D19_14 Sch=sw[11]
#set_property -dict { PACKAGE_PIN H6 IOSTANDARD LVCMOS33 } [get_ports { SW[12] }]; #IO_L24P_T3_35 Sch=sw[12]
#set_property -dict { PACKAGE_PIN U12 IOSTANDARD LVCMOS33 } [get_ports { SW[13] }]; #IO_L20P_T3_A08_D24_14 Sch=sw[13]
#set_property -dict { PACKAGE_PIN U11 IOSTANDARD LVCMOS33 } [get_ports { SW[14] }]; #IO_L19N_T3_A09_D25_VREF_14 Sch=sw[14]
#set_property -dict { PACKAGE_PIN V10 IOSTANDARD LVCMOS33 } [get_ports { SW[15] }]; #IO_L21P_T3_DQS_14 Sch=sw[15]
LEDs
set_property -dict { PACKAGE_PIN H17 IOSTANDARD LVCMOS33 } [get_ports { S }]; #IO_L18P_T2_A24_15 Sch=led[0]
set_property -dict { PACKAGE_PIN K15 IOSTANDARD LVCMOS33 } [get_ports { C_out }]; #IO_L24P_T3_RS1_15 Sch=led[1]
#set_property -dict { PACKAGE_PIN J13 IOSTANDARD LVCMOS33 } [get_ports { LED[2] }]; #IO_L17N_T2_A25_15 Sch=led[2]
#set_property -dict { PACKAGE_PIN N14 IOSTANDARD LVCMOS33 } [get_ports { LED[3] }]; #IO_L8P_T1_D11_14 Sch=led[3]
#set_property -dict { PACKAGE_PIN R18 IOSTANDARD LVCMOS33 } [get_ports { LED[4] }]; #IO_L7P_T1_D09_14 Sch=led[4]
#set_property -dict { PACKAGE_PIN V17 IOSTANDARD LVCMOS33 } [get_ports { LED[5] }]; #IO_L18N_T2_A11_D27_14 Sch=led[5]
#set_property -dict { PACKAGE_PIN U17 IOSTANDARD LVCMOS33 } [get_ports { LED[6] }]; #IO_L17P_T2_A14_D30_14 Sch=led[6]
#set_property -dict { PACKAGE_PIN U16 IOSTANDARD LVCMOS33 } [get_ports { LED[7] }]; #IO_L18P_T2_A12_D28_14 Sch=led[7]
#set_property -dict { PACKAGE_PIN V16 IOSTANDARD LVCMOS33 } [get_ports { LED[8] }]; #IO_L16N_T2_A15_D31_14 Sch=led[8]
#set_property -dict { PACKAGE_PIN T15 IOSTANDARD LVCMOS33 } [get_ports { LED[9] }]; #IO_L14N_T2_SRCC_14 Sch=led[9]
#set_property -dict { PACKAGE_PIN U14 IOSTANDARD LVCMOS33 } [get_ports { LED[10] }]; #IO_L22P_T3_A05_D21_14 Sch=led[10]
#set_property -dict { PACKAGE_PIN T16 IOSTANDARD LVCMOS33 } [get_ports { LED[11] }]; #IO_L15N_T2_DQS_DOUT_CSO_B_14 Sch=led[11]
Tcl Console
Messages
Log
Reports
Design Runs
Error (2)
Critical warning (8)
Warning (23)
Info (88)
Status (114)
Show All
[Common 17-55] 'set_property' expects at least one object. [half adder.xdc:13] (3 more like this)
Implementation (2 errors, 4 critical warnings)
Design Initialization (4 critical warnings)
[Common 17-55] 'set_property' expects at least one object. [half adder.xdc:13] (3 more like this)
Place Design (2 errors)
[Place 30-494] The design is empty
Resolution: Check if opt_design has removed all the leaf cells of your design. Check whether you have instantiated and connected all of the top level ports.
[Common 17-69] Command failed: Placer could not place all instances

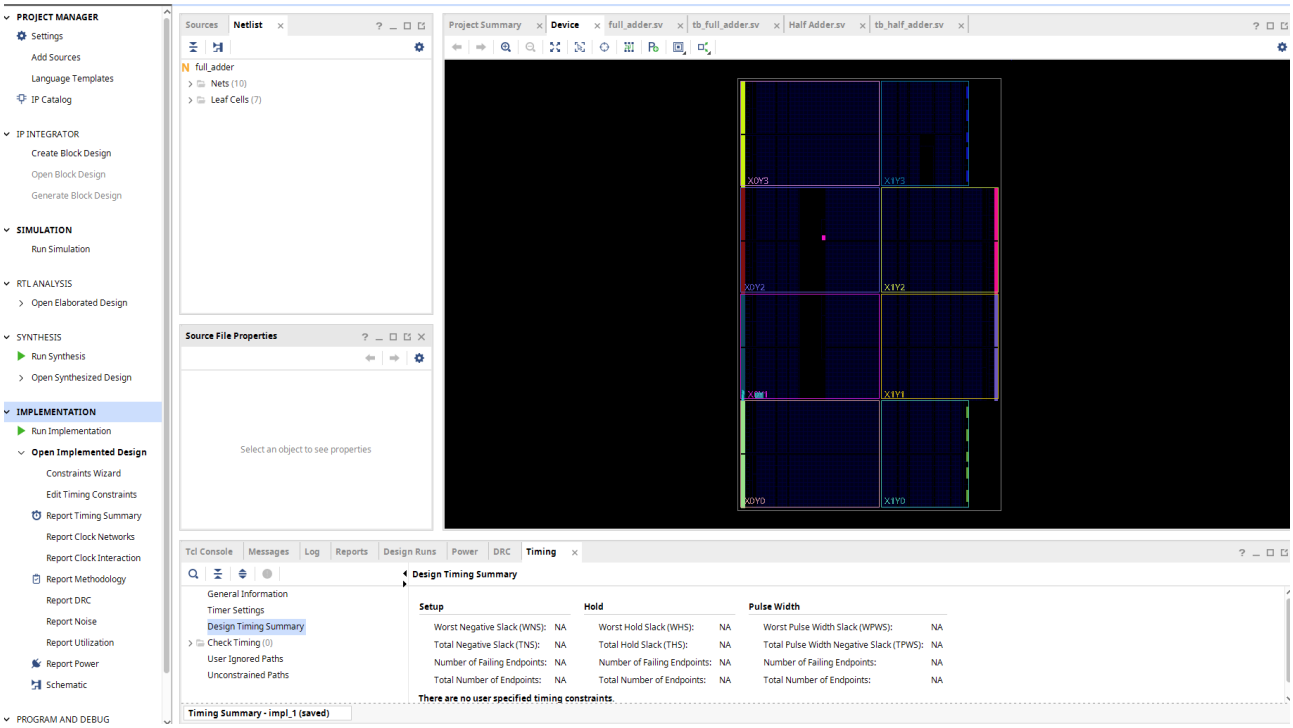

SYNTHESIS
Run Synthesis
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
Set Up Debug
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Utilization
Report Power
Schematic
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Utilization
Report Power
Schematic
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Open Target
Program Device
Add Configuration Memory D
There are no debug cores. Program device Refresh device
Hardware
Name
Status
localhost (1)
Connected
xilinx_tcf/Digilent/210292BB30A
Open
xc7a100t_0 (1)
Programmed
XADC (System Monitor)
Hardware Device Properties
xc7a100t_0
Name: xc7a100t_0
Part: xc7a100t
ID code: 13631093
IR length: 6
Status: Programmed
Programming file: t_3/project_3.runs/impl_1/half_adde
Probes file:
User chain count: 4
General
Properties
tb_half_adder.sv
Half Adder.sv
half adder.xdc
/home/it/project_3/project_3.srcs/sources_1/new/tb_half_adder.sv
// Additional Comments:
//
module tb_half_adder;
logic A, B;
logic S, C_out;
half_adder dut (
.A(A),
.B(B),
.S(S),
.C_out(C_out)
);
initial begin
$display("Time\t A\t B\t S\t C_out");
$display("-----------------------------------");
A = 0; B = 0; #10;
$display("%0t\t %b\t %b\t %b\t %b", $time, A, B, S, C_out);
A = 0; B = 1; #10;
$display("%0t\t %b\t %b\t %b\t %b", $time, A, B, S, C_out);
A = 1; B = 0; #10;
$display("%0t\t %b\t %b\t %b\t %b", $time, A, B, S, C_out);
A = 1; B = 1; #10;
$display("%0t\t %b\t %b\t %b\t %b", $time, A, B, S, C_out);
$finish;
end
endmodule
Tcl Console
Messages
Serial I/O Links
Serial I/O Scans
set_property PROBES.FILE {} [get_hw_devices xc7a100t_0]
set_property FULL_PROBES.FILE {} [get_hw_devices xc7a100t_0]
set_property PROGRAM.FILE {/home/it/project_3/project_3.runs/impl_1/half_adder.bit} [get_hw_devices xc7a100t_0]
program_hw_devices [get_hw_devices xc7a100t_0]
INFO: [Labtools 27-3164] End of startup status: HIGH
refresh_hw_device [lindex [get_hw_devices xc7a100t_0] 0]
INFO: [Labtools 27-1434] Device xc7a100t (JTAG device index = 0) is programmed with a design that has no supported debug core(s) in it.
Type a Tcl command here

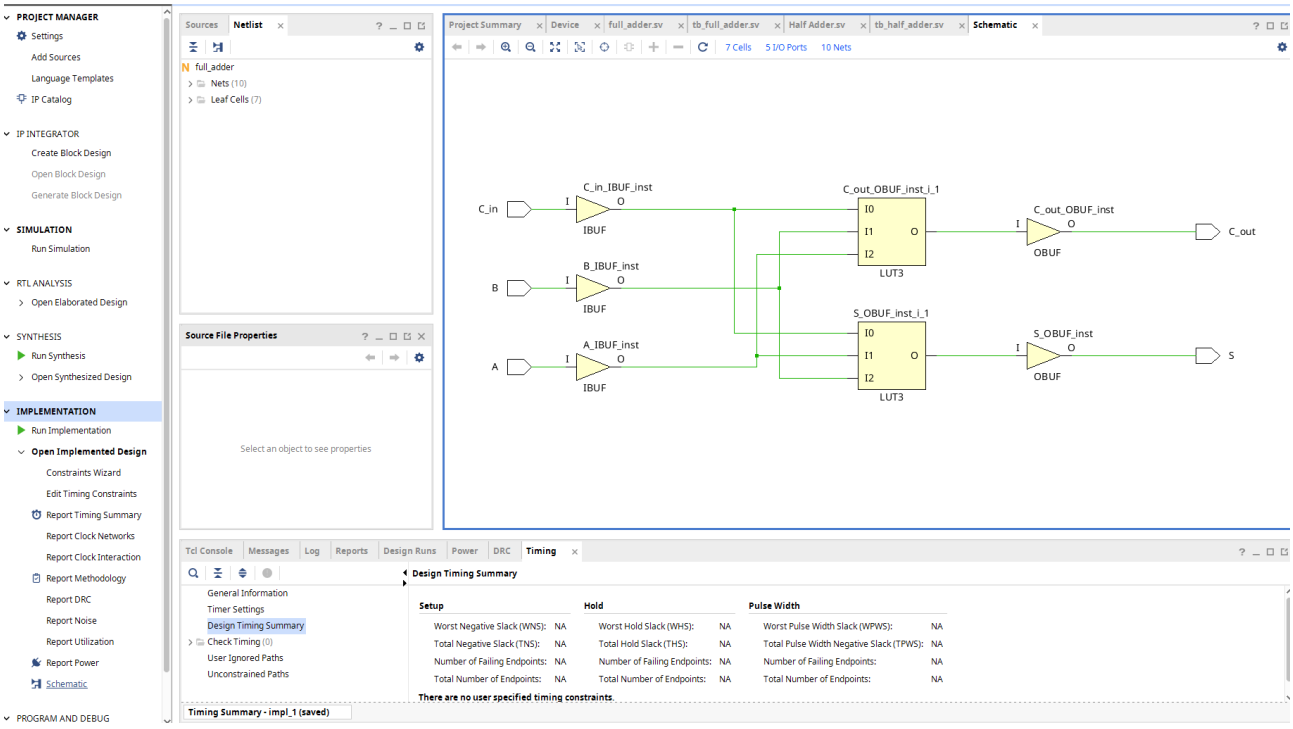

SYNTHESIS
Run Synthesis
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
Set Up Debug
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Open Target
Sources
Netlist
half_adder
Nets (8)
Leaf Cells (6)
Hardware Device Properties
Select an object to see properties
Project Summary
Device
tb_half_adder.sv
Half Adder.sv
half adder.xdc
Schematic
6 Cells
4 I/O Ports
8 Nets
A
B
A_IBUF_inst
B_IBUF_inst
IBUF
C_out_OBUF_inst_i_1
S_OBUF_inst_i_1
LUT2
C_out_OBUF_inst
S_OBUF_inst
OBUF
C_out
S
Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Timing
General Information
Timer Settings
Design Timing Summary
Check Timing (0)
User Ignored Paths
Unconstrained Paths
Design Timing Summary
Setup
Hold
Pulse Width
Worst Negative Slack (WNS): NA
Total Negative Slack (TNS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Worst Hold Slack (WHS): NA
Total Hold Slack (THS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Worst Pulse Width Slack (WPWS): NA
Total Pulse Width Negative Slack (TPWS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
There are no user specified timing constraints.
Timing Summary - impl_1 (saved)

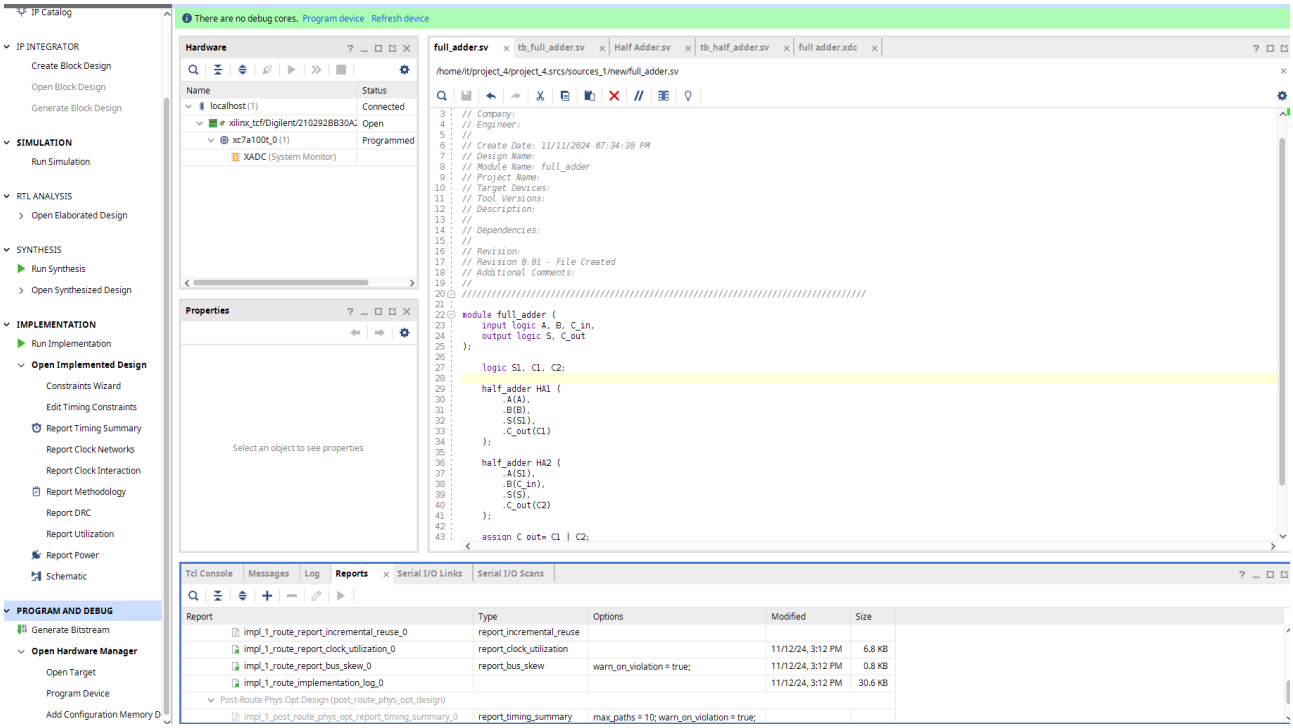
Task3


PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Sources
Design Sources (1)
tb_full_adder (tb_full_adder.sv) (1)
DUT : full_adder (full_adder.sv) (2)
Constraints
Simulation Sources (1)
sim_1 (1)
tb_full_adder (tb_full_adder.sv) (1)
Utility Sources
Hierarchy
Libraries
Compile Order
Source File Properties
full_adder.sv
Enabled
Location: /home/it/project_4/project_4.srcs/sources_1/ne
Type: SystemVerilog
Library: xil_defaultlib
Size: 0.8 KB
Modified: Today at 14:57:01 PM
Copied to: <Project Directory>/project_4.srcs/sources_1/n
General
Properties
Project Summary
tb_full_adder.sv
full_adder.sv
/home/it/project_4/project_4.srcs/sources_1/new/tb_full_adder.sv
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
module tb_full_adder;
logic A, B, C_in;
logic S, C_out;
full_adder DUT (
.A(A),
.B(B),
.C_in(C_in),
.S(S),
.C_out(C_out)
);
initial begin
$display("Time | A B C_in | S C_out");
$display("-------------------------------------");
for (int i =0; i < 8; i++) begin
{A, B, C_in} = i;
#5;
$display("%4t | %b %b %b | %b %b", $time, A, B, C_in, S, C_out);
end
$finish;
end
endmodule
Tcl Console
Messages
Log
Reports
Design Runs
Name
Constraints
Status
WNS
TNS
WHS
THS
TPWS
Total Power
Failed Routes
LUT
FF
BRAMs
URAM
DSP
Start
Elapsed
Run Strategy
Report Strategy
synth_1
constrs_1
Not started
Vivado Synthesis Defaults (Vivado Synthesis 2019)
impl_1
constrs_1
Not started
Vivado Implementation Defaults (Vivado Implementation 2019)

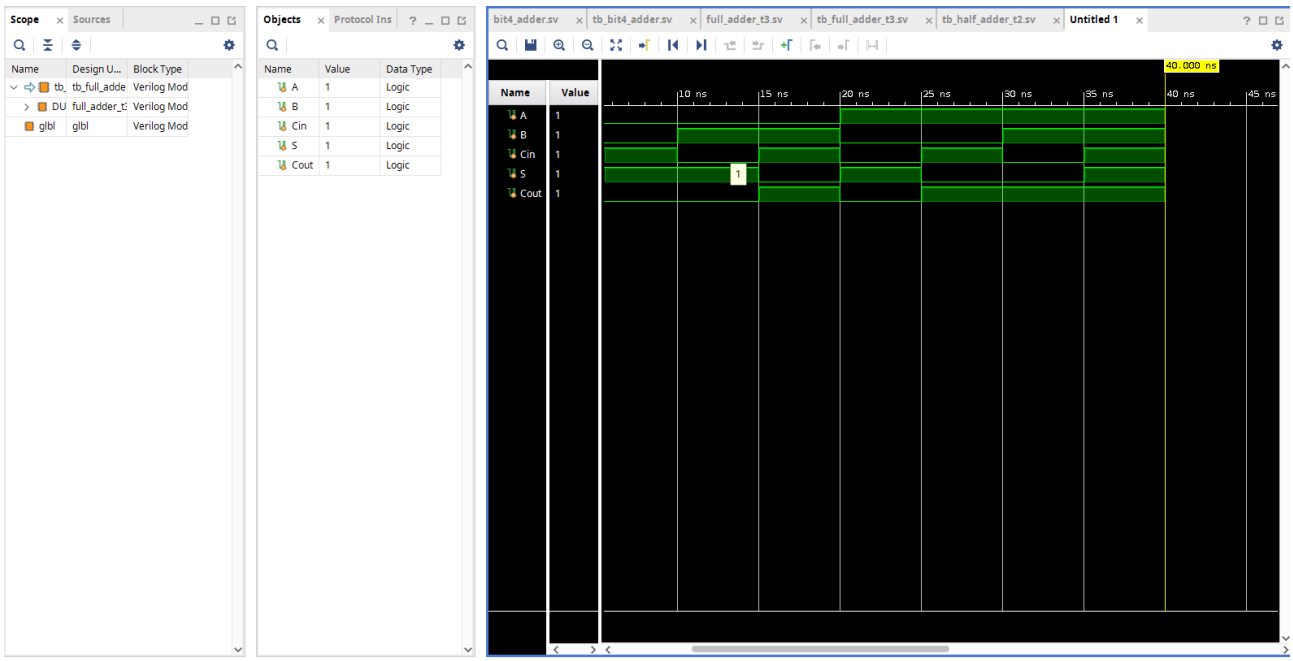

PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Scope
Sources
Objects
Protocol Ins
full_adder.sv
tb_full_adder.sv
Half Adder.sv
tb_half_adder.sv
Untitled 1
Name
Value
A
B
C_in
S
C_out
40.000 ns
Tcl Console
Messages
Log
$finish called at time : 40 ns : File "/home/it/project_4/project_4.srcs/sources_1/new/tb_full_adder.sv" Line 46
INFO: [USF-XSim-96] XSim completed. Design snapshot 'tb_full_adder_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:08 ; elapsed = 00:00:05 . Memory (MB): peak = 7073.875 ; gain = 220.887 ; free physical = 3666 ; free virtual = 34573
Type a Tcl command here

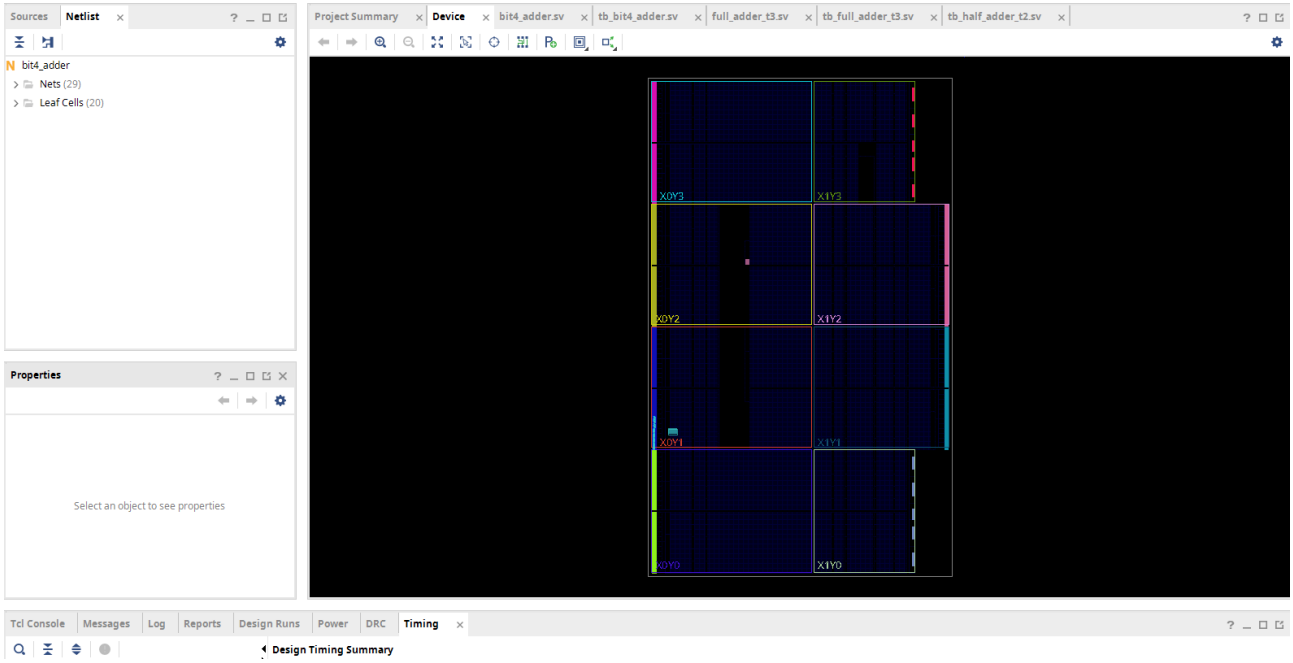

PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
PROGRAM AND DEBUG
Sources
Netlist
full_adder
Nets (10)
Leaf Cells (7)
Source File Properties
Select an object to see properties
Project Summary
Device
full_adder.sv
tb_full_adder.sv
Half Adder.sv
tb_half_adder.sv
X0Y3
X1Y3
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Timing
General Information
Timer Settings
Design Timing Summary
Check Timing (0)
User Ignored Paths
Unconstrained Paths
Design Timing Summary
Setup
Worst Negative Slack (WNS): NA
Total Negative Slack (TNS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Hold
Worst Hold Slack (WHS): NA
Total Hold Slack (THS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Pulse Width
Worst Pulse Width Slack (WPWS): NA
Total Pulse Width Negative Slack (TPWS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
There are no user specified timing constraints.
Timing Summary - impl_1 (saved)

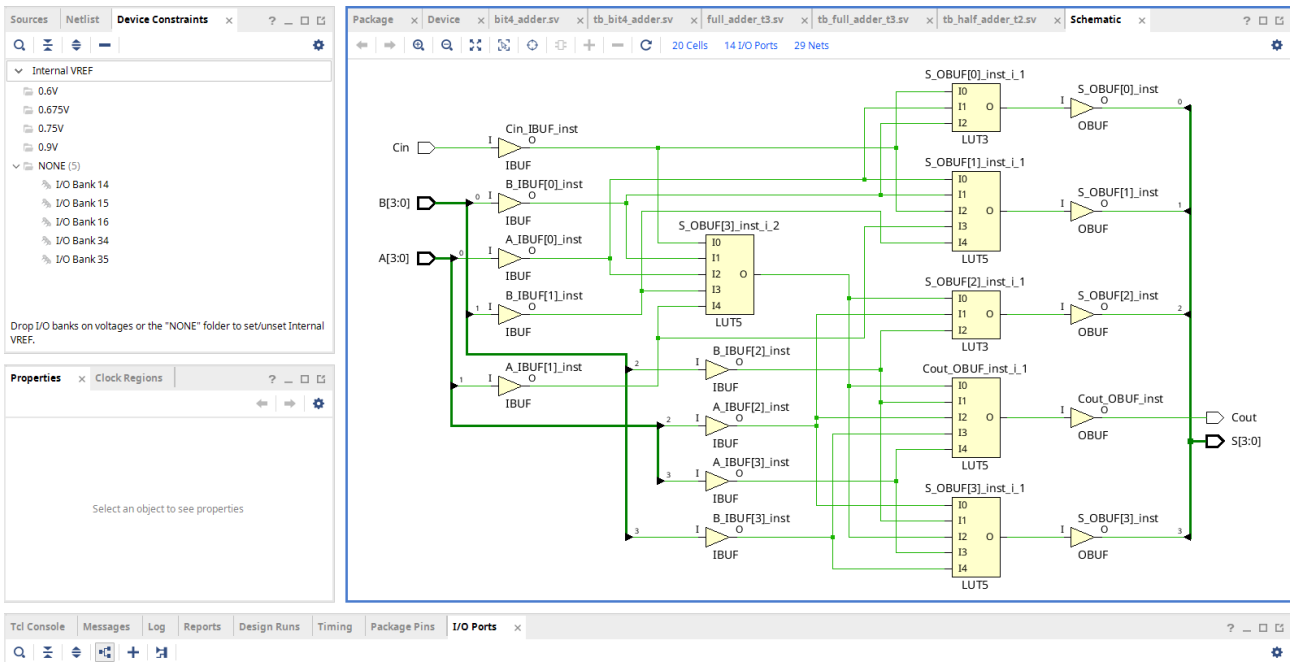

PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
PROGRAM AND DEBUG
Sources
Netlist
full_adder
Nets (10)
Leaf Cells (7)
Source File Properties
Select an object to see properties
Project Summary
Device
full_adder.sv
tb_full_adder.sv
Half Adder.sv
tb_half_adder.sv
Schematic
7 Cells
5 I/O Ports
10 Nets
C_in
B
A
C_in_IBUF_inst
B_IBUF_inst
A_IBUF_inst
IBUF
C_out_OBUF_inst_i_1
S_OBUF_inst_i_1
LUT3
C_out_OBUF_inst
S_OBUF_inst
OBUF
C_out
S
Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Timing
Design Timing Summary
General Information
Timer Settings
Design Timing Summary
Check Timing (0)
User Ignored Paths
Unconstrained Paths
Setup
Hold
Pulse Width
Worst Negative Slack (WNS): NA
Total Negative Slack (TNS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Worst Hold Slack (WHS): NA
Total Hold Slack (THS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Worst Pulse Width Slack (WPWS): NA
Total Pulse Width Negative Slack (TPWS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
There are no user specified timing constraints.
Timing Summary - impl_1 (saved)


There are no debug cores. Program device Refresh device
Hardware
Name
Status
localhost (1)
Connected
xc7a100t_0 (1)
Programmed
XADC (System Monitor)
Properties
Select an object to see properties
full_adder.sv
tb_full_adder.sv
Half Adder.sv
tb_half_adder.sv
full adder.xdc
/home/it/project_4/project_4.srcs/sources_1/new/full_adder.sv
module full_adder (
input logic A, B, C_in,
output logic S, C_out
);
logic S1, C1, C2;
half_adder HA1 (
.A(A),
.B(B),
.S(S1),
.C_out(C1)
);
half_adder HA2 (
.A(S1),
.B(C_in),
.S(S),
.C_out(C2)
);
assign C_out= C1 | C2;
Tcl Console
Messages
Log
Reports
Serial I/O Links
Serial I/O Scans
Report
Type
Options
Modified
Size
impl_1_route_report_incremental_reuse_0
report_incremental_reuse
impl_1_route_report_clock_utilization_0
report_clock_utilization
11/12/24, 3:12 PM
6.8 KB
impl_1_route_report_bus_skew_0
report_bus_skew
warn_on_violation = true;
11/12/24, 3:12 PM
0.8 KB
impl_1_route_implementation_log_0
11/12/24, 3:12 PM
30.6 KB
Post-Route Phys Opt Design (post_route_phys_opt_design)
impl_1_post_route_phys_opt_report_timing_summary_0
report_timing_summary
max_paths = 10; warn_on_violation = true;

Task4


Scope
Sources
Objects
Protocol Ins
Name
Design U...
Block Type
Value
Data Type
A
B
Cin
S
Cout
Logic
Verilog Mod
glbl
bit4_adder.sv
tb_bit4_adder.sv
full_adder_t3.sv
tb_full_adder_t3.sv
tb_half_adder_t2.sv
Untitled 1
40.000 ns
10 ns
15 ns
20 ns
25 ns
30 ns
35 ns
40 ns
45 ns


Sources
Netlist
bit4_adder
Nets (29)
Leaf Cells (20)
Properties
Select an object to see properties
Project Summary
Device
X0Y3
X1Y3
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Timing
Design Timing Summary


Sources
Netlist
Device Constraints
Internal VREF
0.6V
0.675V
0.75V
0.9V
NONE (5)
I/O Bank 14
I/O Bank 15
I/O Bank 16
I/O Bank 34
I/O Bank 35
Drop I/O banks on voltages or the "NONE" folder to set/unset Internal VREF.
Properties
Clock Regions
Select an object to see properties
Package
Device
bit4_adder.sv
tb_bit4_adder.sv
full_adder_t3.sv
tb_full_adder_t3.sv
tb_half_adder_t2.sv
Schematic
20 Cells
14 I/O Ports
29 Nets
Cin
B[3:0]
A[3:0]
Cin_IBUF_inst
B_IBUF[0]_inst
A_IBUF[0]_inst
B_IBUF[1]_inst
A_IBUF[1]_inst
B_IBUF[2]_inst
A_IBUF[2]_inst
A_IBUF[3]_inst
B_IBUF[3]_inst
IBUF
S_OBUF[3]_inst_i_2
LUT5
S_OBUF[0]_inst_i_1
S_OBUF[1]_inst_i_1
S_OBUF[2]_inst_i_1
Cout_OBUF_inst_i_1
S_OBUF[3]_inst_i_1
LUT3
LUT5
S_OBUF[0]_inst
S_OBUF[1]_inst
S_OBUF[2]_inst
S_OBUF[3]_inst
Cout_OBUF_inst
OBUF
Cout
S[3:0]
Tcl Console
Messages
Log
Reports
Design Runs
Timing
Package Pins
I/O Ports