EGC220-02 Digital Logic Fundamentals

Assignment #5

Due: October 18, 2021

Text: Digital Design With an Introduction to the Verilog HDL, VHDL, and System Verilog – Mano and Ciletti, Pearson 2018

Read Chapter 3

3.3 Four variable k-map – implicants, prime implicants, essential 1-cells, essential prime implicants, sum-of-products simplification
3.4 Product-of-sums simplification
3.5 Don't care Conditions

Chapter 4

4.2 Combinational Circuits
4.3 Analysis of Combinational Circuits
4.4 Design Procedure
4.5 Binary Adder-Subtractor – Half adder, Full adder, Binary adder, Binary subtractor
4.8 Magnitude Comparator

Problems: Work all problems and submit the solution as one pdf file

(10 pts) **Prob. 1.**

Implement the following Boolean function F, together with the don't-care conditions d, using no more than two NOR gates:

$$F(A, B, C, D) = \Sigma(2, 4, 10, 12, 14,)$$
$$d(A, B, C, D) = \Sigma(0, 1, 5, 8)$$

Assume that both the normal and complement inputs are available.

(10 pts) **Prob. 2.**

With the use of maps, find the simplest sum-of-products form of the function F = f.g, where

f = abc' + c'd + a'cd' + b'cd'
and g = (a + b + c' + d') (b' + c' + d) (a' + c + d')

(20 pts) **Prob. 3.**

Implement the following four Boolean expressions with three half adders:

$$D = A \oplus B \oplus C$$
$$E = A'BC + AB'C$$
$$F = ABC' + (A' + B')C$$
$$G = ABC$$

(15 pts) **Prob. 4.**

Design a combinational circuit with three inputs, x, y, and z, and three outputs, A, B, and C. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the input.

(15 pts) **Prob. 5.**

Design a half-subtractor circuit with inputs x and y and outputs *Diff* and B_{out}. The circuit subtracts the bits $x - y$ and places the difference in D and the borrow in B_{out}.

(a) Design a full-subtractor circuit with three inputs x, y, B_{in} and two outputs *Diff* and B_{out}. The circuit subtracts $x - y - B_{in}$, where B_{in} is the input borrow, B_{out} is the output borrow, and *Diff* is the difference.

(15 pts) **Prob. 6.**

Consider the combinational circuit shown in Fig. P4.1. (HDL—see Problem 4.49.)

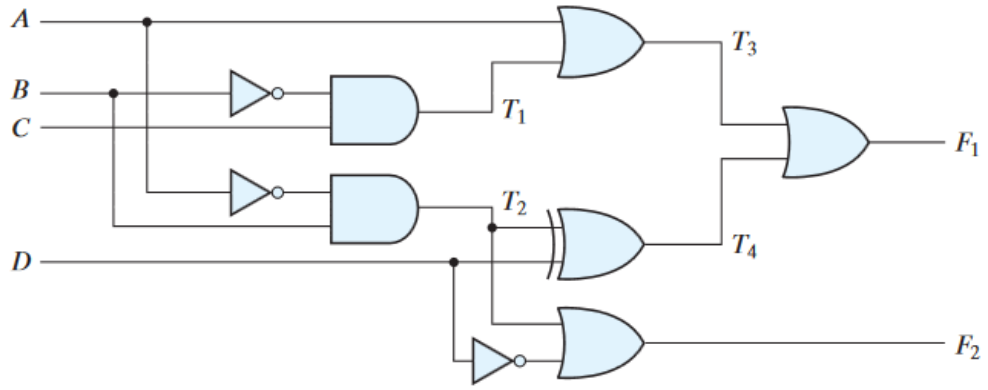

FIGURE P4.1

List the truth table with 16 binary combinations of the four input variables. Then list the binary values for T_1 through T_4 and outputs F_1 and F_2 in the table.

(15 pts) **Prob. 7.**

Obtain the simplified Boolean expressions for output F and G in terms of the input variables in the circuit of Fig. P4.2.

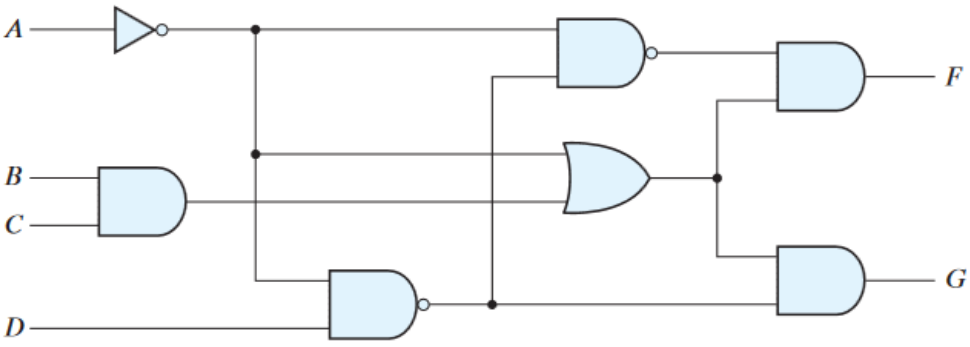

FIGURE P4.2