CSE 4207 CT 4 Assignment
Roll No: 1903077

Assignment Problem:
Category: C
Word Size = 7
ALU Operations = AND, ADD

Solution:
Video:

Have you uploaded the video?	YES
Check List 1: Have you explained the design using testbenches to prove that your circuit is working correctly and giving correct results?	YES
Check List 2: Have you shown full synthesis results showing all the required info including RTL Synthesis, RTL Floorplan, RTL Power Analysis, GDS and Heatmap (for details, see assignment template doc)?	YES
NB: Failing to upload video will cause heavy point penalty (5-6 Marks)	
NB: Failing to add any required info will cause point penalty (1-2 Marks)	

HDL Code:

Check List: Have you added all the modules written in verilog including ALU, ALU_OP1, ALU_OP2, CONTROLLER, TOP, TOP_TESTBENCH, ALU_TESTBENCH, CONTROLLER_TESTBENCH?	YES
NB: Failing to add any required info will cause point penalty (1-2 Marks)	

top.v

```
`include "controller.v"

module Top (
    input wire clk,
    input wire rst,
    output wire [6:0] res,
    output wire CF,
    output wire GZ // Greater than  zero flag
);

Controller uut0(
    .clk(clk),
```

```
    .rst(rst),
    .res(res),
    .CF(CF),
    .GZ(GZ)
);


endmodule
```

controller.v

```
`include "alu_7_bit.v"

module Controller (
    input clk,rst,
    output reg [6:0] a,
    output reg [6:0] b,
    output reg op,

    output wire [6:0] res,
    output wire GZ, //grater than zero flag
    output wire CF
);

ALU uut0(

    .a(a),
    .b(b),
    .op(op),
    .res(res),
    .GZ(GZ),
    .CF(CF)
);


localparam start =3'b000,
           one=3'b001,
           two=3'b010,
           three=3'b011,
           finish=3'b100;

reg [2:0] current_state, next_state;



always @(posedge clk)
begin
```

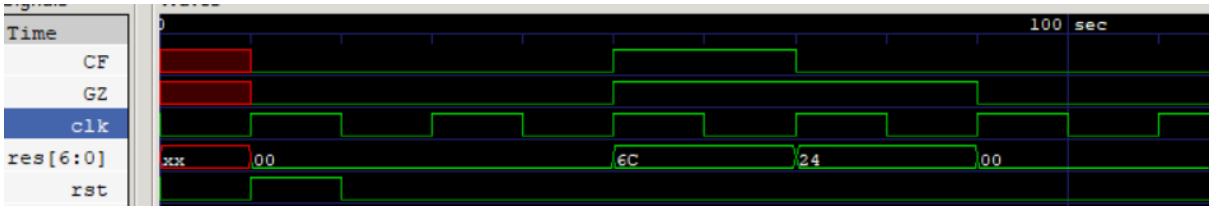
```
    if(rst)
    begin
        current_state<=start;
    end
    else
    begin
        current_state<=next_state;
    end
end

always @(*)
begin
    case (current_state)
        start:
        begin
            a=7'b0000000;
            b=7'b0000000;
            op=0;
            next_state=one;
        end
        one:
        begin
            a=7'b0000000;
            b=7'b1111111;
            op=0;
            next_state=two;
        end
        two:
        begin
            a=7'b1101101;
            b=7'b1111111;
            op=1;
            next_state=three;
        end

        three:
        begin
            a=7'b1101101;
            b=7'b0100110;
            op=0;
            next_state=finish;
        end

        finish:
        begin
            a=7'b0000000;
            b=7'b0000000;
            op=0;
```

```
            next_state=finish;
        end
        default:
        begin
            a=7'b0000000;
            b=7'b0000000;
            op=0;
            next_state=start;
        end
    endcase

end
endmodule
```

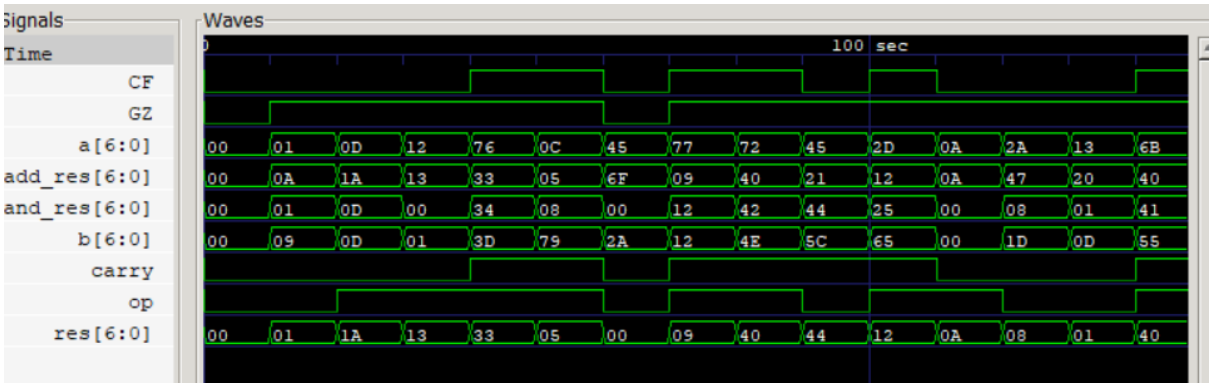
RTL Timing Diagram:

Check List: Have you added all the timing diagrams of ALU_TESTBENCH, CONTROLLER_TESTBENCH, TOP_TESTBENCH?	YES/NO
NB: Failing to add any required info will cause point penalty (1-2 Marks)	

top_tb.v



alu_tb.v



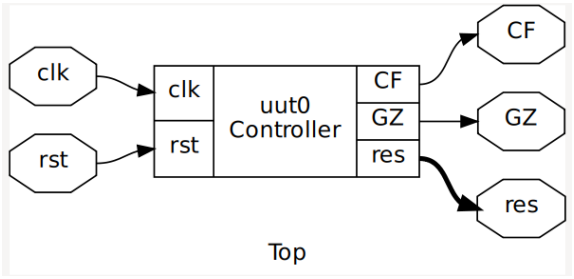
RTL Synthesis (130nm Skywater PDK with OpenLane toolchain):

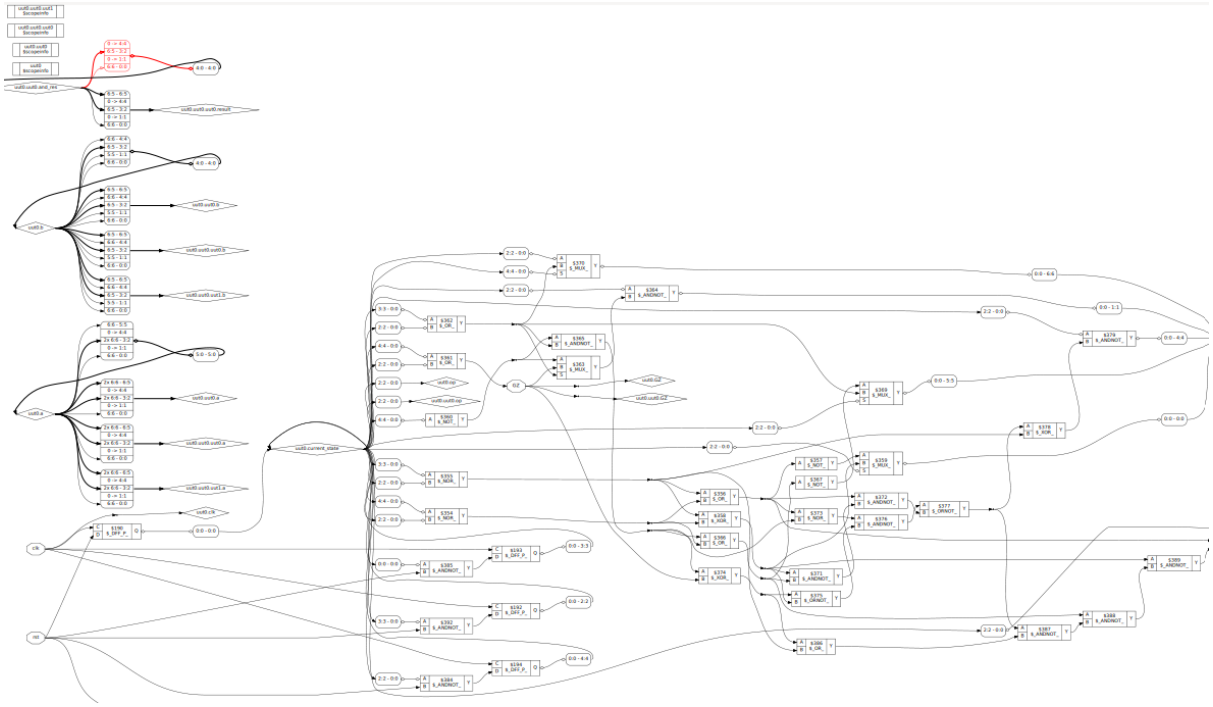
Check List: Have you added *RTL synthesis summary*, *RTL synthesized design figure* and *Standard cell usage in synthesized design*?	YES
NB: Failing to add any required info will cause point penalty (1-2 Marks)	

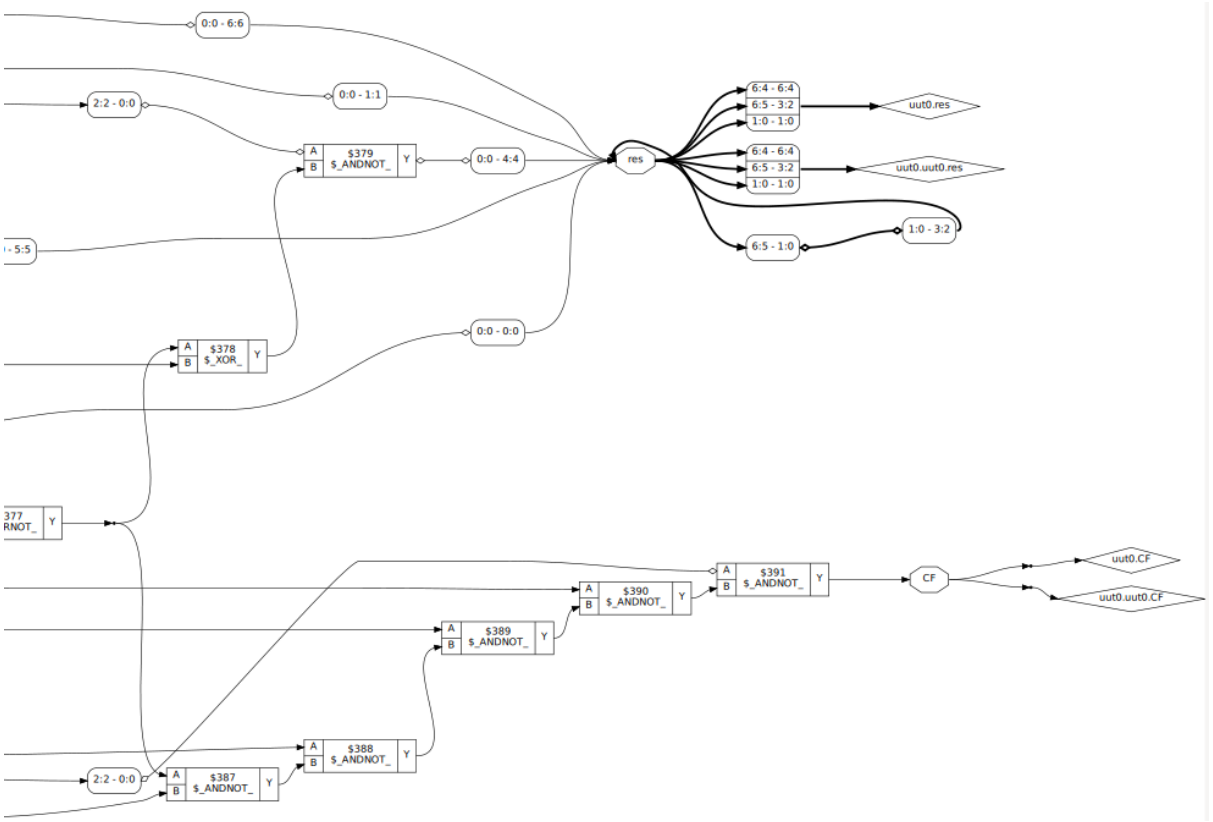
RTL synthesis summary

```
120. Printing statistics.

=== Top ===

Number of wires:                 53
Number of wire bits:            135
Number of public wires:          26
Number of public wire bits:     108
Number of ports:                  5
Number of port bits:             11
Number of memories:               0
Number of memory bits:            0
Number of processes:              0
Number of cells:                 42
$_ANDNOT_                        14
$_DFF_P_                          4
$_MUX_                            4
$_NOR_                            3
$_NOT_                            3
$_ORNOT_                          2
$_OR_                             5
$_XOR_                            3
$scopeinfo                        4
```

RTL synthesized design figure **:**







Standard cell usage in synthesized design

'runs/RUN_2025-06-01_11-58-51/52-odb-cellfrequencytables/odb-c

ells by Master

Cell	Count
sky130_ef_sc_hd__decap_12	33
sky130_fd_sc_hd__a21o_1	1
sky130_fd_sc_hd__and2b_1	3
sky130_fd_sc_hd__and3b_1	1
sky130_fd_sc_hd__buf_1	1
sky130_fd_sc_hd__buf_2	7
sky130_fd_sc_hd__clkbuf_1	3
sky130_fd_sc_hd__clkbuf_16	3
sky130_fd_sc_hd__conb_1	2
sky130_fd_sc_hd__decap_3	28
sky130_fd_sc_hd__decap_4	5
sky130_fd_sc_hd__decap_6	5
sky130_fd_sc_hd__decap_8	5
sky130_fd_sc_hd__dfxtp_1	4
sky130_fd_sc_hd__dlygate4sd3_1	3
sky130_fd_sc_hd__fill_1	15
sky130_fd_sc_hd__fill_2	4
sky130_fd_sc_hd__or2_1	2
sky130_fd_sc_hd__tapvpwrvgnd_1	12

Cell Function	Count
sky130_ef_sc_hd__decap	33
sky130_fd_sc_hd__a21o	1
sky130_fd_sc_hd__and2b	3
sky130_fd_sc_hd__and3b	1
sky130_fd_sc_hd__buf	8
sky130_fd_sc_hd__clkbuf	6
sky130_fd_sc_hd__conb	2
sky130_fd_sc_hd__decap	43
sky130_fd_sc_hd__dfxtp	4
sky130_fd_sc_hd__dlygate4sd3	3
sky130_fd_sc_hd__fill	19
sky130_fd_sc_hd__or2	2
sky130_fd_sc_hd__tapvpwrvgnd	12

Cells by SCL

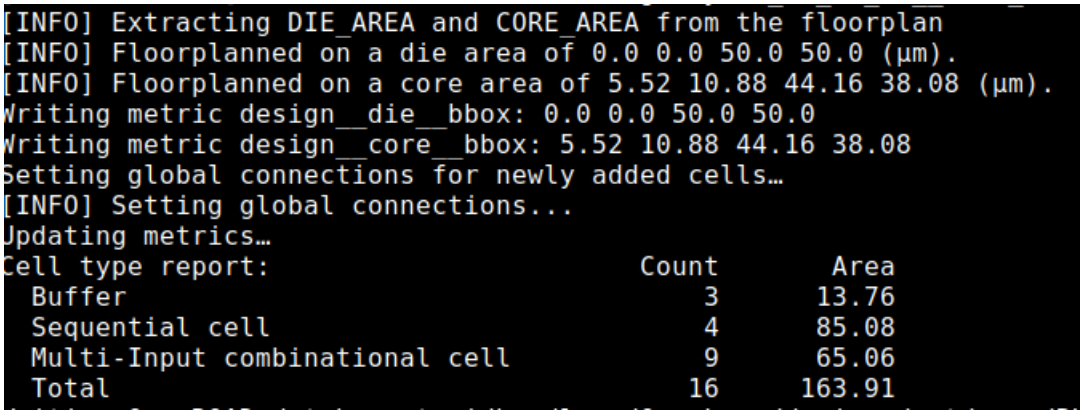
SCL	Count
sky130_ef_sc_hd	33
sky130_fd_sc_hd	104

Buffers by Cell Master

Buffer	Count
sky130_fd_sc_hd__buf_1	1
sky130_fd_sc_hd__buf_2	7
sky130_fd_sc_hd__clkbuf_1	3
sky130_fd_sc_hd__clkbuf_16	3
sky130_fd_sc_hd__dlygate4sd3_1	3

RTL Floorplan (130nm Skywater PDK with OpenLane toolchain)

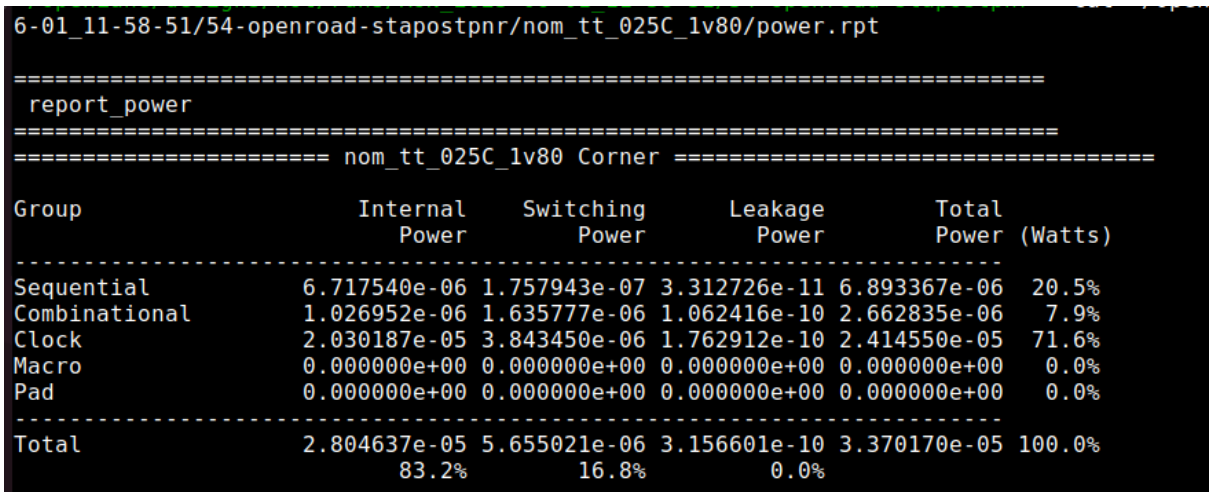
Check List: Have you added RTL Floorplan info?	YES
NB: Failing to add any required info will cause point penalty (1-2 Marks)	



```
[INFO] Extracting DIE_AREA and CORE_AREA from the floorplan
[INFO] Floorplanned on a die area of 0.0 0.0 50.0 50.0 (µm).
[INFO] Floorplanned on a core area of 5.52 10.88 44.16 38.08 (µm).
Writing metric design__die__bbox: 0.0 0.0 50.0 50.0
Writing metric design__core__bbox: 5.52 10.88 44.16 38.08
Setting global connections for newly added cells…
[INFO] Setting global connections...
Updating metrics…
Cell type report:                          Count       Area
  Buffer                                       3      13.76
  Sequential cell                              4      85.08
  Multi-Input combinational cell               9      65.06
  Total                                       16     163.91
```

RTL Power Analysis (130nm Skywater PDK with OpenLane toolchain)

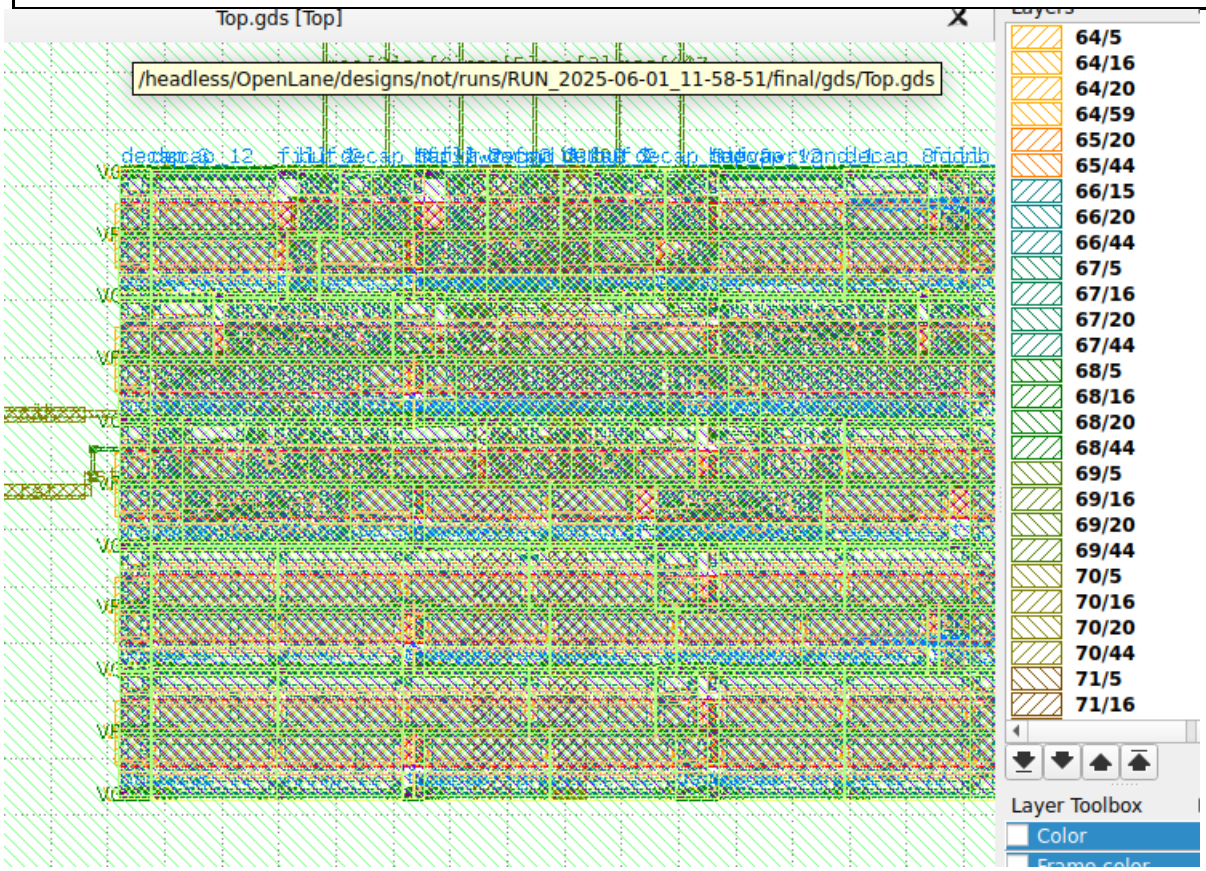
Check List: Have you added RTL Power Analysis info?	YES
NB: Failing to add any required info will cause point penalty (1-2 Marks)	



```
6-01_11-58-51/54-openroad-stapostpnr/nom_tt_025C_1v80/power.rpt

===========================================================================
 report_power
===========================================================================
======================== nom_tt_025C_1v80 Corner ===================================

Group                  Internal    Switching      Leakage        Total
                          Power        Power        Power        Power (Watts)
----------------------------------------------------------------------------
Sequential           6.717540e-06 1.757943e-07 3.312726e-11 6.893367e-06  20.5%
Combinational        1.026952e-06 1.635777e-06 1.062416e-10 2.662835e-06   7.9%
Clock                2.030187e-05 3.843450e-06 1.762912e-10 2.414550e-05  71.6%
Macro                0.000000e+00 0.000000e+00 0.000000e+00 0.000000e+00   0.0%
Pad                  0.000000e+00 0.000000e+00 0.000000e+00 0.000000e+00   0.0%
----------------------------------------------------------------------------
Total                2.804637e-05 5.655021e-06 3.156601e-10 3.370170e-05 100.0%
                            83.2%        16.8%         0.0%
```

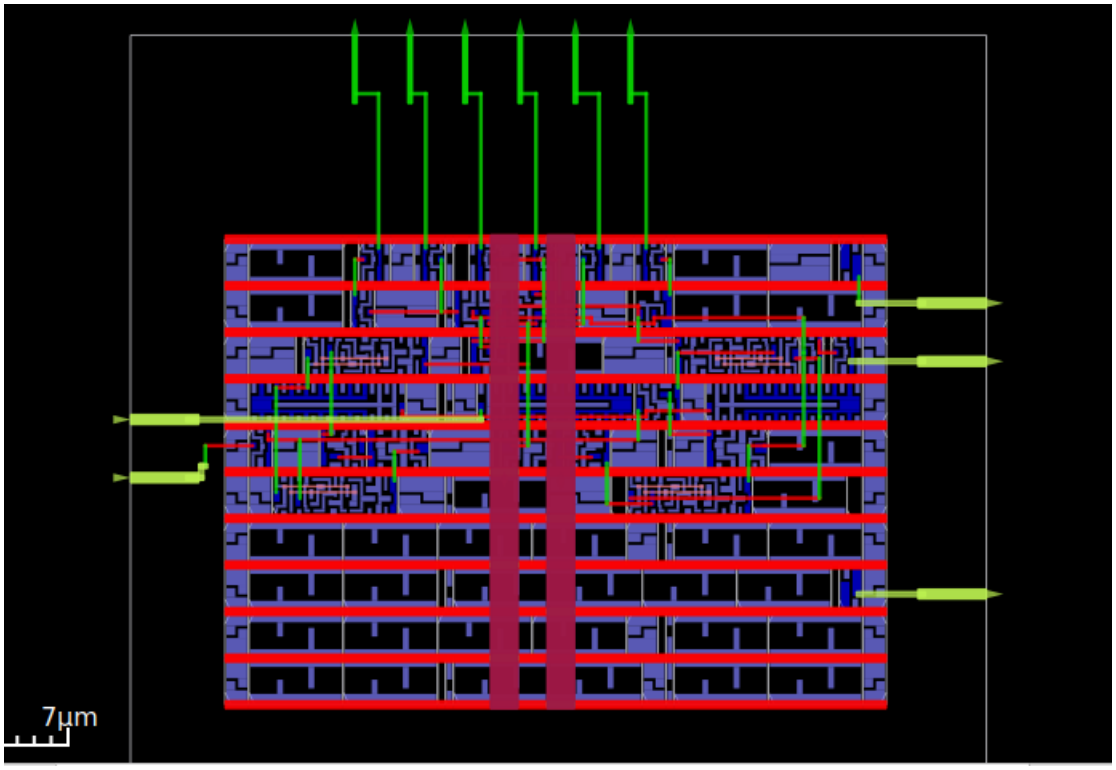
GDS Layout (130nm Skywater PDK with OpenLane toolchain)

Check List: Have you added the GDS Layout figure?	YES
NB: Failing to add any required info will cause point penalty (1-2 Marks)	



Heatmap (130nm Skywater PDK with OpenLane toolchain)

Check List: Have you added the heatmap?	YES
NB: Failing to add any required info will cause point penalty (1-2 Marks)	


7µm