Computer-Aided VLSI System Design
Homework 4 Report

Due Tuesday, Nov. 22, 14:00

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Questions and Discussion

1. Fill in the blanks

Physical category		
Design Stage	Description	Value
Gate-level Simulation	Cycle time for Gate-level Simulation (ex. 10ns)	6(ns)
	Area for Synthesis (ex. 50000μm^2)	22072
	Gate-level Simulation Time for f1	9252
	Gate-level Simulation Time for f2	9252
	Gate-level Simulation Time for f3	9252
	Gate-level Simulation Time for f4	9234
	Gate-level Simulation Time for f5	9246
	Gate-level Simulation Time for f6	9234
	Gate-level Simulation Time for f7	9234

2. Specify the methods you adopted for low-power design. (10pts)

I use three methods to achieve low power design. They are "reducing the number of registers", "reducing the number of comparators", and "the tradeoff between cycle time and power consumption".

First, reducing the number of redundant structures or registers is key. That is, we can save electricity to supply some areas. For example, I combined the tasks

PMAX and MAX to compare data. I then combined MAX, MIN based on the "fn" controlling "greater than" or "less than".

Second, using a lower number of comparators is key. That is, to save power compared to larger registers. More specifically, I'm grouping 16 8-bit registers with one wire. However, if I compare the two wires directly, it consumes a lot of power. Therefore, we should compare the 8-bit registers one by one.

In the end, the trade-off between timing and power consumption is the key point. That said, if we need lower timing constraints, the IC compiler will use powerful components for synthesis. This will produce higher power. My observation is: Although they are reverse relationships, they are not inverse relationships. We can do more experiments with different timing requirements to get better performance scores.

All in all, low-power design has a big impact on performance scores. How to trade-off between cycle time and power, and have a nice area, is my experience in this job.