Computer-Aided VLSI System Design
Homework 5 Report

Due Tuesday, Dec. 6, 14:00

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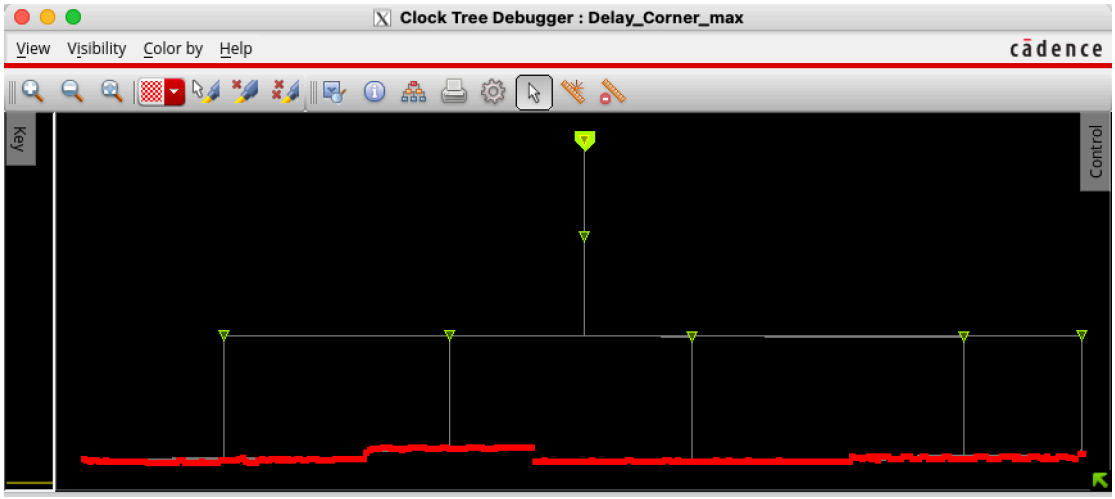
APR Results

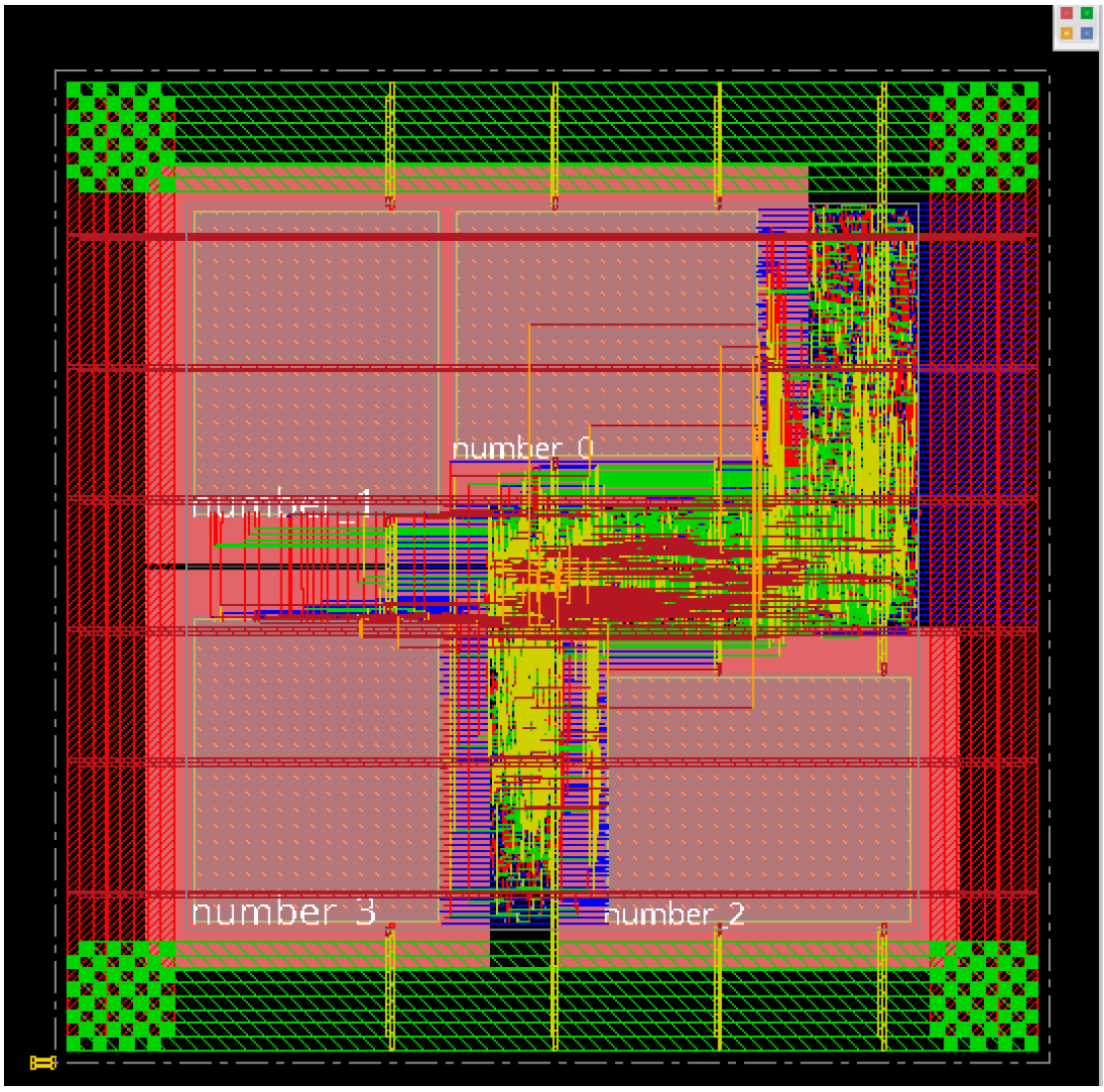
1. Fill in the blanks below.

Design Stage	Description	Value
P&R	Number of DRC violations (ex: 0) (Verify -> Verify Geometry…)	0
	Number of LVS violations (ex: 0) (Verify -> Verify Connectivity…)	0
	Die Area (um^2)	365902.11
	Core Area (um^2)	197577.36
Post-layout Simulation	Clock Period for Post-layout Simulation (ex. 10ns)	20ns
Follow your design in HW3? (If not, write down the student ID of the designer)		Yes

Questions and Discussion

1. Attach the snapshot of CCOpt Clock Tree Debugger result, and show the routing result in the layout (10%).





2. Attach the snapshot of DRC and LVS checking after routing. (5%)

```
*** Starting Verify DRC (MEM: 1311.3) ***

  VERIFY DRC ..... Starting Verification
  VERIFY DRC ..... Initializing
  VERIFY DRC ..... Deleting Existing Violations
  VERIFY DRC ..... Creating Sub-Areas
  VERIFY DRC ..... Using new threading
  VERIFY DRC ..... Sub-Area: {0.000 0.000 204.000 201.280} 1 of 9
  VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {204.000 0.000 408.000 201.280} 2 of 9
  VERIFY DRC ..... Sub-Area : 2 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {408.000 0.000 606.280 201.280} 3 of 9
  VERIFY DRC ..... Sub-Area : 3 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {0.000 201.280 204.000 402.560} 4 of 9
  VERIFY DRC ..... Sub-Area : 4 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {204.000 201.280 408.000 402.560} 5 of 9
  VERIFY DRC ..... Sub-Area : 5 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {408.000 201.280 606.280 402.560} 6 of 9
  VERIFY DRC ..... Sub-Area : 6 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {0.000 402.560 204.000 603.520} 7 of 9
  VERIFY DRC ..... Sub-Area : 7 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {204.000 402.560 408.000 603.520} 8 of 9
  VERIFY DRC ..... Sub-Area : 8 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {408.000 402.560 606.280 603.520} 9 of 9
  VERIFY DRC ..... Sub-Area : 9 complete 0 Viols.

  Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.7  ELAPSED TIME: 1.00  MEM: 0.0M) ***
```

```
******** Start: VERIFY CONNECTIVITY ********
Start Time: Sat Dec  3 14:08:30 2022

Design Name: core
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (606.2800, 603.5200)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Sat Dec  3 14:08:30 2022
Time Elapsed: 0:00:00.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.2  MEM: 0.000M)
```

3. Attach the snapshot of the timing report for **setup time and hold time** with no timing violation (post-route). (5%)

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+--------
-+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default
 |
+--------------------+---------+---------+---------+---------+---------+--------
-+
|           WNS (ns):|  6.162  | 10.648  |  6.162  |  6.662  |   N/A   |  0.000
 |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000
 |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0
 |
|          All Paths:|   709   |   369   |   324   |   16    |   N/A   |    0
 |
+--------------------+---------+---------+---------+---------+---------+--------
-+

+----------------+-------------------------------+-------------------+
|                |             Real              |       Total       |
|    DRVs        +------------------+------------+-------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)   |
+----------------+------------------+------------+-------------------+
|   max_cap      |      2 (2)       |   -0.027   |      2 (2)        |
|   max_tran     |      1 (1)       |   -0.127   |      1 (1)        |
|   max_fanout   |      0 (0)       |     0      |      0 (0)        |
|   max_length   |      0 (0)       |     0      |      0 (0)        |
+----------------+------------------+------------+-------------------+

Density: 73.433%


------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+--------
-+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | default
 |
+--------------------+---------+---------+---------+---------+---------+--------
-+
|           WNS (ns):|  0.468  |  0.468  |  9.821  | 10.876  |   N/A   |  0.000
 |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000
 |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0
 |
|          All Paths:|   709   |   369   |   324   |   16    |   N/A   |    0
 |
+--------------------+---------+---------+---------+---------+---------+--------
-+

Density: 73.433%
```

4. Show the critical path after post-route optimization. What is the path type? (5%)
   (The slack of the critical path should match the smallest slack in the timing report)

```
Path 1: MET Recovery Check with Pin z_reg_2__7_/CK
Endpoint:   z_reg_2__7_/RN (^) checked with  leading edge of 'i_clk'
Beginpoint: i_rst_n        (^) triggered by  leading edge of 'i_clk'
Path Groups: {in2reg}
Analysis View: av_func_mode_max
Other End Arrival Time          0.523
- Recovery                      0.259
+ Phase Shift                  20.000
+ CPPR Adjustment               0.000
= Required Time                20.263
- Arrival Time                 14.102
= Slack Time                    6.162
     Clock Rise Edge                     0.000
     + Input Delay                      10.000
     + Network Insertion Delay           0.500
     = Beginpoint Arrival Time          10.500
     +-------------------------------------------------------------------------+
     |     Instance     |    Arc     |   Cell    | Delay | Arrival | Required |
     |                  |            |           |       |  Time   |   Time   |
     |------------------+------------+-----------+-------+---------+----------|
     |                  | i_rst_n ^  |           |       |  10.500 |   16.662 |
     | FE_OFC17_i_rst_n | A ^ -> Y ^ | BUFX4     | 0.435 |  10.935 |   17.097 |
     | FE_OFC0_i_rst_n  | A ^ -> Y ^ | CLKBUFX6  | 0.584 |  11.520 |   17.681 |
     | FE_OFC1_i_rst_n  | A ^ -> Y ^ | BUFX4     | 0.621 |  12.141 |   18.303 |
     | FE_OFC2_i_rst_n  | A ^ -> Y ^ | BUFX4     | 0.631 |  12.772 |   18.934 |
     | FE_OFC3_i_rst_n  | A ^ -> Y ^ | BUFX4     | 0.635 |  13.407 |   19.568 |
     | FE_OFC4_i_rst_n  | A ^ -> Y ^ | CLKBUFX6  | 0.680 |  14.087 |   20.249 |
     | z_reg_2__7_      | RN ^       | DFFRX1    | 0.015 |  14.102 |   20.263 |
     +-------------------------------------------------------------------------+
```

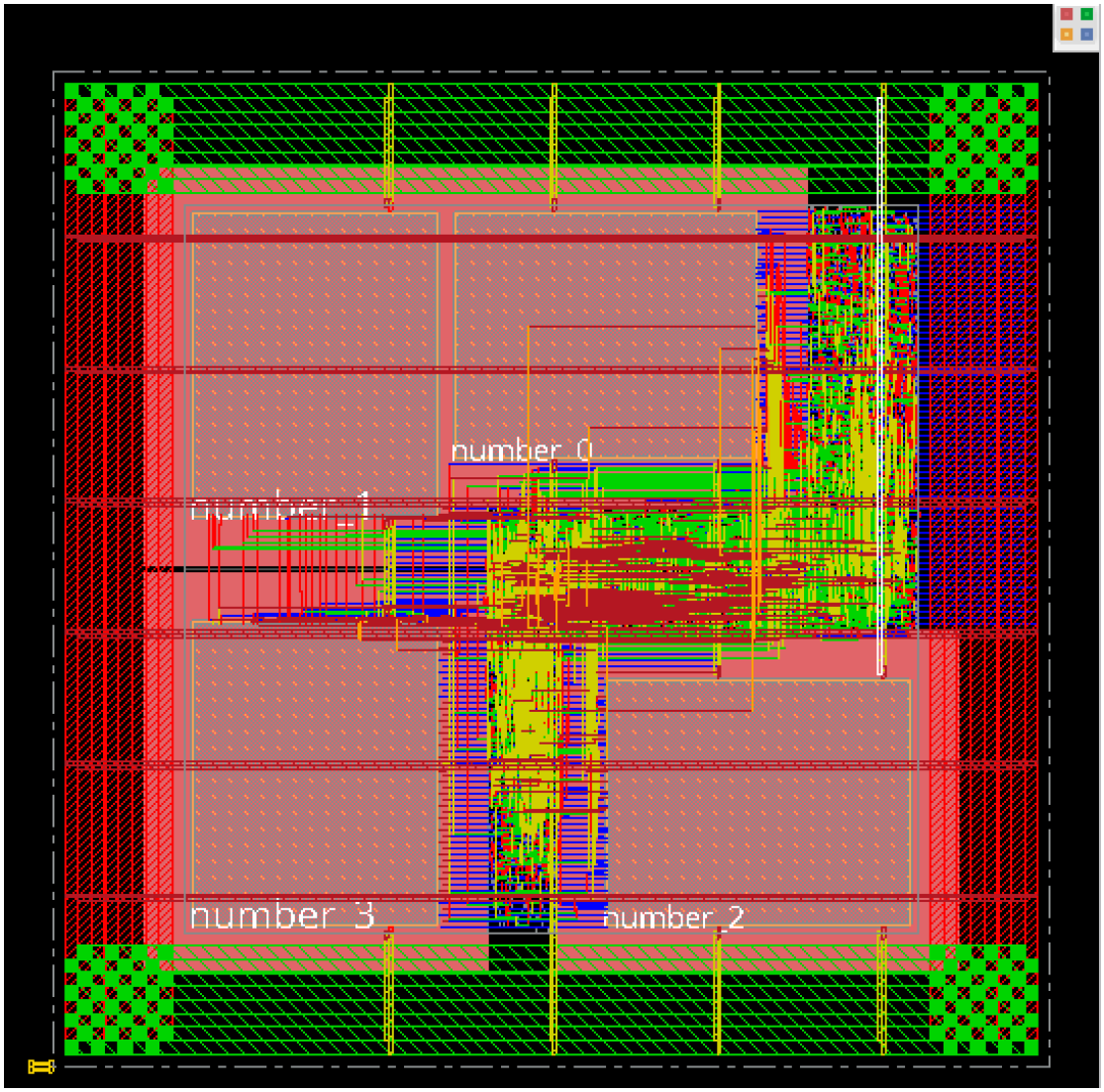
5. Attach the snapshot of GDS stream out messages. (10%)

```
Trim Metal                          0

Merging with GDS libraries
Scanning GDS file library/gds/tsmc13gfsg_fram.gds to register cell name ......
Scanning GDS file library/gds/tpz013g3_v1.1.gds to register cell name ......
Merging GDS file library/gds/tsmc13gfsg_fram.gds ......
        ****** Merge file: library/gds/tsmc13gfsg_fram.gds has version number: 5
.
        ****** Merge file: library/gds/tsmc13gfsg_fram.gds has units: 1000 per m
icron.
        ****** unit scaling factor = 1 ******
Merging GDS file library/gds/tpz013g3_v1.1.gds ......
        ****** Merge file: library/gds/tpz013g3_v1.1.gds has version number: 5.
        ****** Merge file: library/gds/tpz013g3_v1.1.gds has units: 1000 per mic
ron.
        ****** unit scaling factor = 1 ******
**WARN: (IMPOGDS-217):  Master cell: sram_512x8 not found in merged file(s) and
will therefore not be included in the resulting streamOut file. Verify the file
names specified with the -merge option are correct and that they contain a defin
ition of this cell.
**WARN: (IMPOGDS-218):  Number of master cells not found after merging: 1

######Streamout is finished!
```

6. Attach the snapshot of the final area result. (5%)

```
************************** Analyze Floorplan **************************
    Die Area(um^2)              : 365902.11
    Core Area(um^2)             : 197577.36
    Chip Density (Counting Std Cells and MACROs and IOs): 40.753%
    Core Density (Counting Std Cells and MACROs): 75.472%
    Average utilization         : 100.000%
    Number of instance(s)       : 3397
    Number of Macro(s)          : 4
    Number of IO Pin(s)         : 32
    Number of Power Domain(s) : 0
************************** Estimation Results **************************
************************************************************************
```

7. Attach the snapshot of your final layout **after adding core filler**. (Remember to switch to **Physical view** and make Pin Shapes visible) (10%)



8. What is your strategy for floorplanning (especially for placing the SRAMs)? What is the reason behind it? (10%)

Answer:

I have 4x 512x8-sram in my design. Considering the large area of each sram, I use the B*-tree algorithm to distribute the srams to the four corners. This will help a lot with routing issues such as density or connectivity.

However, in the end I only used three corners and reserved one for the power plan area. Additional sram can also be allocated via B*-tree algorithm.