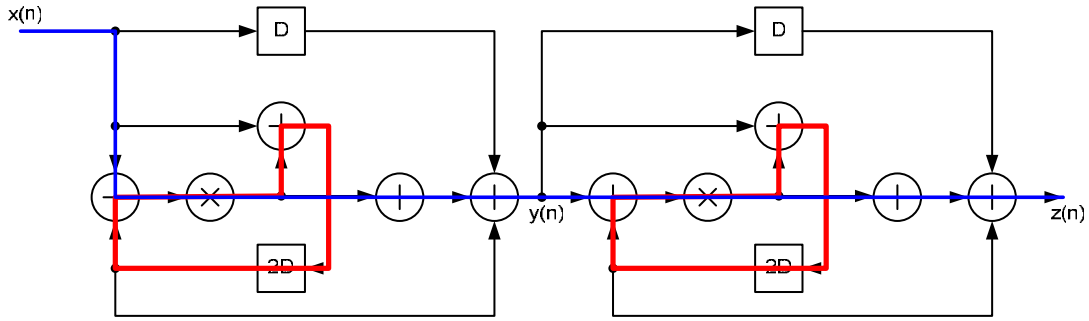
DSP in VLSI Design
Homework (IV)

Retiming
Reference Answer

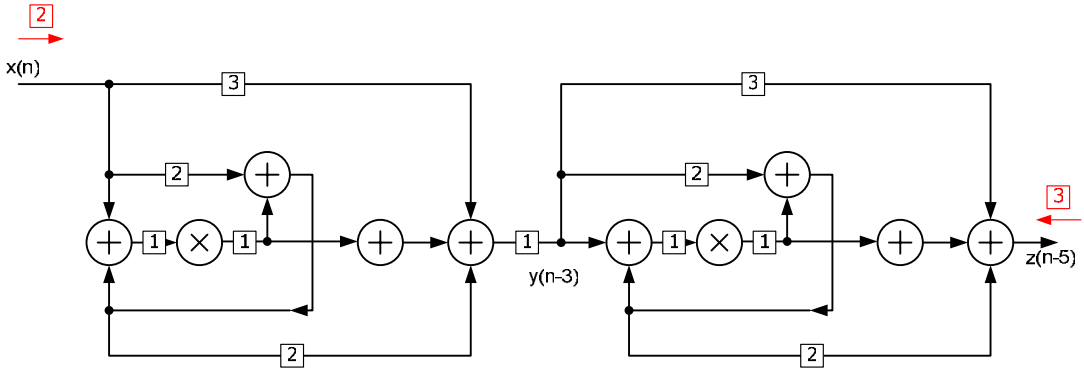
1. Consider the wave digital filter shown below. Assume that each multiply operation requires 20 ns and each add operation required 10 nsec.
   (a) Calculate the iteration period bound of this filter by inspection.
   (b) Where is the critical path?
   (c) Manually pipeline and/or retime this filter to achieve a critical path equal to the iteration period bound.



(a) Iteration bound: Red circle, 2 adders & 1 multiplier, 2 Delays, 2x10 + 1x20 = 40
Iteration bound = 40/2 = 20 ns

(b) Critical path: Blue line, 6 adders & 2 multipliers, 6x10 + 2x20 = 100
Critical path = 100 ns

(c) Pipeline from x(n) with 2 delays, from z(n) with 3 delays. After retiming, the result is shown below.



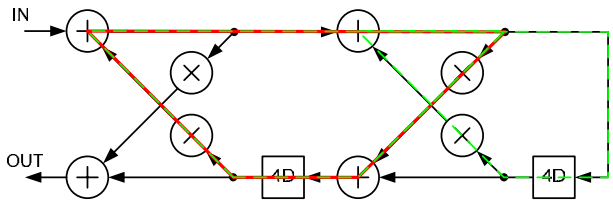
2. Consider the IIR filter DFG shown in below. Assume that addition and multiplication require 1 and 2 u.t., respectively.

(a) By inspection, calculate the iteration bound.

(b) Compute the critical path time of the circuit.

(c) Pipeline and/or retime this system to achieve a critical path of 2 u.t. Do this by inspection (manually).

(d) Pipeline and/or retime this system to achieve sample period of 1 u.t., where Fine-grain retiming is allowed. Do this by inspection (manually).



(a) 2 loop,

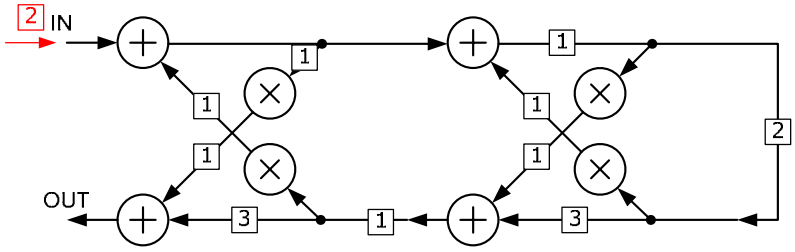
A. Red loop, 3 adders & 2 multipliers, 4 delays, 3x1 + 2x2 = 7
Loop bound = 7/4 = 1.75 u.t.

B. Green loop, 4 adders & 3 multipliers, 8 delays, 4x1 + 3x2 = 10
Loop bound = 10/8 = 1.25 u.t.

Iteration bound = max (1.75, 1.25) = 1.75 u.t.

(b) Red path, 3 adders & 2 multipliers, 3x1 + 2x2 = 7
Critical path time = 7 u.t.

(c) Pipeline from IN with 2 delays. After retiming, the result is shown below.

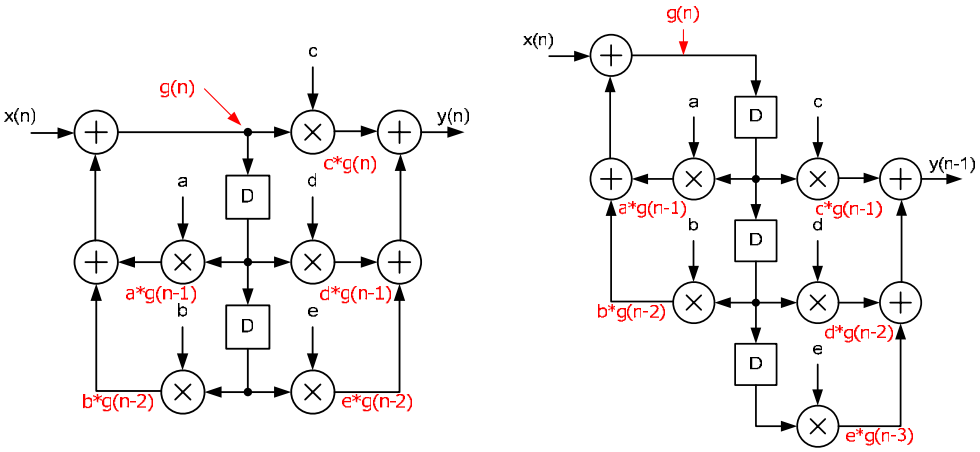


(d) Since iteration bound is greater 1 u.t. (1.75 u.t.), it's unable to use pipelining or retiming only to achieve a critical path of 1 u.t.

3. The two IIR filter DFGs shown below are equivalent.

(a) Prove the two circuits are equivalent.

(b) Transform the left circuit to the right circuit by pipelining and/or retiming.



(a) Let g(n) be the results indicated in these figures.

A. Left graph:

$g(n) = x(n) + ag(n-1) + bg(n-2)$

$y(n) = cg(n) + dg(n-1) + e(g-2)$

B. Right graph:

$g(n) = x(n) + ag(n-1) + bg(n-2)$

$y(n-1) = cg(n-1) + dg(n-2) + e(g-3) \rightarrow y(n) = cg(n) + dg(n-1) + e(g-2)$

According to A & B, two circuits are equivalent.

(b) Pipeline from x(n) with 1 delays. Take blue lines as one node and green lines as another. Combine 2 individual delays between blue node and green node. Then the final result is obtained.