# DSP in VLSI Design
## Homework (VI)

## Folding
## Reference Answer

Deadline: April 13

1. Consider the 6-tap FIR filter

$$y(n) = \sum_{i=0}^{5} h_i x(n-i)$$

implemented using data-broadcast form shown in the following figure. This filter S0={MA5, MA4}, S1={MA3, MA2}, S2={MA1, MA0}.

(a) Design the folded architecture.

(b) Construct a schedule corresponding to the folded architecture and verify that the folded architecture generated the desired filter output samples.

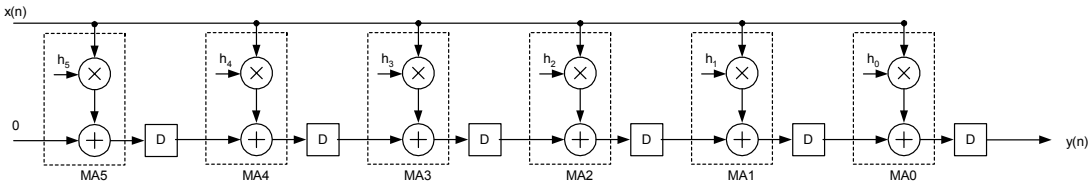



Fig. 1

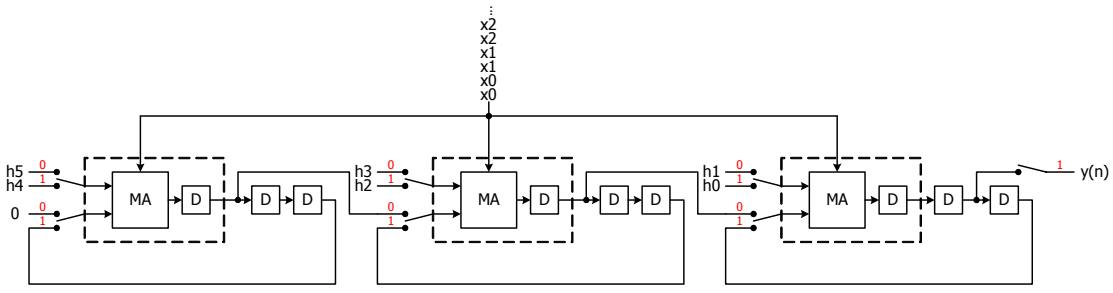
(a)

Folding Set: S0={MA5, MA4}, S1={MA3, MA2}, S2={MA1, MA0}

Folding Equations:

| $D_F(U \rightarrow V)$ | N*We-Pu+v-u |
|---|---|
| $D_F(5 \rightarrow 4)$ | 2*1-1+1-0=2 |
| $D_F(4 \rightarrow 3)$ | 2*1-1+0-1=0 |
| $D_F(3 \rightarrow 2)$ | 2*1-1+1-0=2 |
| $D_F(2 \rightarrow 1)$ | 2*1-1+0-1=0 |
| $D_F(1 \rightarrow 0)$ | 2*1-1+1-0=2 |

Folded architecture:



(OR)

Folding Set: S0={MA5, MA4}, S1={MA3, MA2}, S2={MA1, MA0}

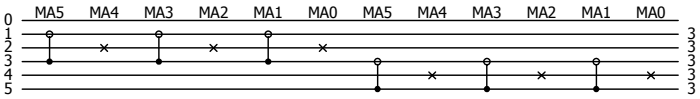
Folding Equations:

| $D_F(U \rightarrow V)$ | N*We-Pu+v-u |
|---|---|
| $D_F(5 \rightarrow 4)$ | 2*1-1+1-0=2 |
| $D_F(4 \rightarrow 3)$ | 2*1-1+0-1=0 |
| $D_F(3 \rightarrow 2)$ | 2*1-1+1-0=2 |
| $D_F(2 \rightarrow 1)$ | 2*1-1+0-1=0 |
| $D_F(1 \rightarrow 0)$ | 2*1-1+1-0=2 |

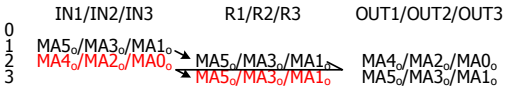
Lifetime Table:

| MA | u+Pu | u+Pu+Max($D_F(U \rightarrow V)$) |
|---|---|---|
| 5 | 1 | 3 |
| 4 | 2 | 2 |
| 3 | 1 | 3 |
| 2 | 2 | 2 |
| 1 | 1 | 3 |
| 0 | 2 | 2 |

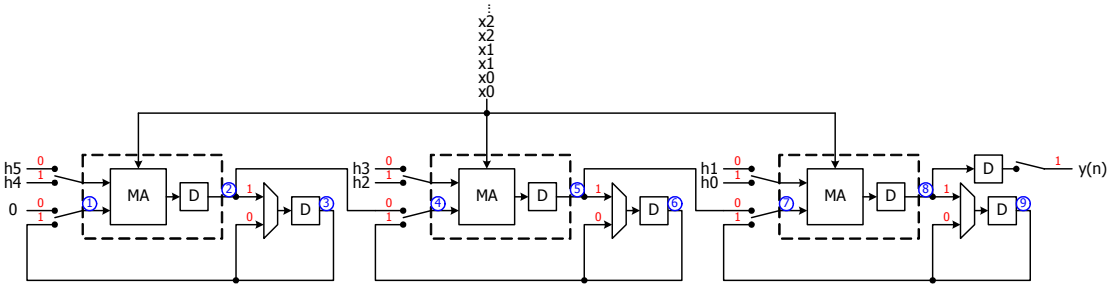
Lifetime Chart:




Forward-backward Register Allocation:




Folded architecture:




(b) Schedule

| time | x(n) | ① | ② | ③ | ④ | ⑤ | ⑥ | ⑦ | ⑧ | ⑨ | OUT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | x(0) | 0 | | | | | | | | | |
| 1 | x(0) | | $S_{50}$ | | | | | | | | |
| 2 | x(1) | 0 | $S_{40}$ | $S_{50}$ | | | | | | | |
| 3 | x(1) | $h_5x(0)=S_{50}$ | $S_{51}$ | $S_{50}$ | | | | | | | |
| 4 | x(2) | 0 | $h_4x(1)+h_5x(0)=S_{50\text{-}41}$ | $S_{51}$ | $S_{50\text{-}41}$ | | | | | | |
| 5 | x(2) | $h_5x(1)=S_{51}$ | $S_{52}$ | $S_{51}$ | | $S_{50\text{-}41\text{-}32}$ | | | | | |
| 6 | x(3) | 0 | $S_{51\text{-}42}$ | $S_{52}$ | $S_{51\text{-}42}$ | | $S_{50\text{-}41\text{-}32}$ | | | | |
| 7 | x(3) | $h_5x(2)=S_{52}$ | $S_{53}$ | $S_{52}$ | $S_{50\text{-}41\text{-}32}$ | $S_{51\text{-}42\text{-}33}$ | $S_{50\text{-}41\text{-}32}$ | | | | |
| 8 | x(4) | 0 | $S_{52\text{-}43}$ | | | $S_{50\text{-}41\text{-}32\text{-}23}$ | | $S_{50\text{-}41\text{-}32\text{-}23}$ | | | |
| 9 | x(4) | | | | | | | | $S_{50\text{-}41\text{-}32\text{-}23\text{-}14}$ | | |
| 10 | x(5) | | | | | | | $S_{51\text{-}42\text{-}33\text{-}24}$ | | $S_{50\text{-}41\text{-}32\text{-}23\text{-}14}$ | |
| 11 | x(5) | | | | | | | $S_{50\text{-}41\text{-}32\text{-}23\text{-}14}$ | $S_{51\text{-}42\text{-}33\text{-}24\text{-}15}$ | $S_{50\text{-}41\text{-}32\text{-}23\text{-}14}$ | |
| 12 | x(6) | | | | | | | | $S_{50\text{-}41\text{-}32\text{-}23\text{-}14\text{-}05}$ | $S_{51\text{-}42\text{-}33\text{-}24\text{-}15}$ | |
| 13 | x(6) | | | | | | | | | | $S_{50\text{-}41\text{-}32\text{-}23\text{-}14\text{-}05}$ |
| 14 | x(7) | | | | | | | | | | |
| 15 | x(7) | | | | | | | | | | $S_{51\text{-}42\text{-}33\text{-}24\text{-}15\text{-}06}$ |

The output of the folded architecture is the same as the output of original FIR filter but slow by 2.

2. Consider the 4-bit carry propagation adder (CPA) shown in the following figure. Now, we want to derive its bit-serial architecture by using folding technique.

(a) Derive the folding set.

(b) Design the folded architecture.

(c) Construct the schedule to show the architecture can do the same operation as CPA.

(d) Similarly, use the same method to derive 2-digit-serial architecture with the folding set, folded architecture, and schedule.

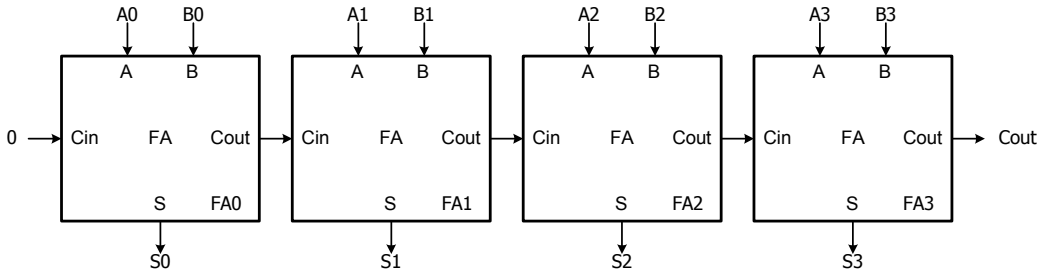
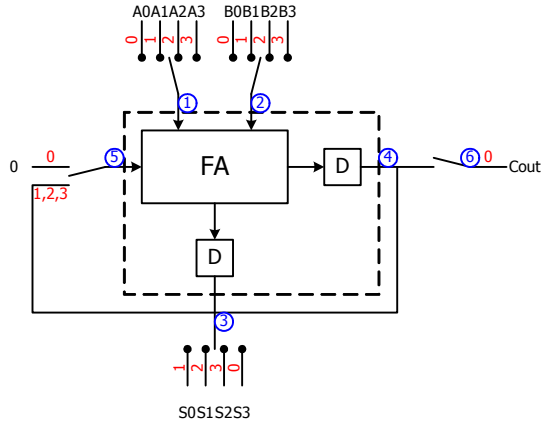



Fig. 2

(a) Folding Set: {FA0, FA1, FA2, FA3}

| $D_F(U \rightarrow V)$ | N*We-Pu+v-u |
|---|---|
| $D_F(0 \rightarrow 1)$ | 4*0-1+1-0=0 |
| $D_F(1 \rightarrow 2)$ | 4*0-1+2-1=0 |
| $D_F(2 \rightarrow 3)$ | 4*0-1+3-2=0 |

(b) Folded Architecture:



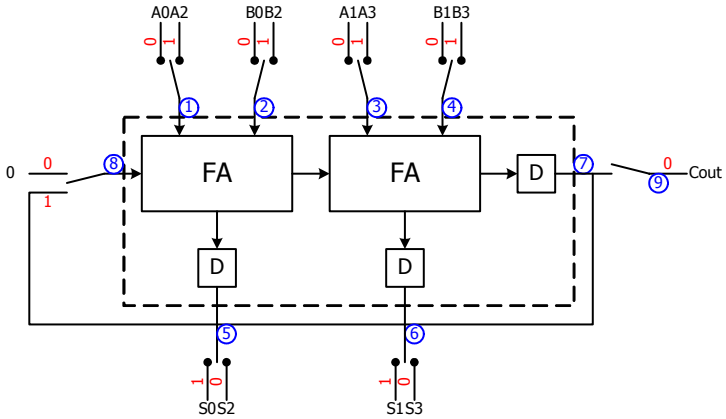

(c) Schedule:

| time | ① | ② | ③ | ④ | ⑤ | ⑥ |
|---|---|---|---|---|---|---|
| 0 | A0 | B0 | | | 0 | |
| 1 | A1 | B1 | S0 | C0 | C0 | |
| 2 | A2 | B2 | S1 | C1 | C1 | |
| 3 | A3 | B3 | S2 | C2 | C2 | |
| 4 | | | S3 | C3 | 0 | C3 |

(d) Folding Set: {FA0-FA1, FA2-FA3}

| $D_F(U \rightarrow V)$ | N*We-Pu+v-u |
|---|---|
| $D_F(01 \rightarrow 23)$ | 2*0-1+1-0=0 |

Folded Architecture:




Schedule:

| time | ① | ② | ③ | ④ | ⑤ | ⑥ | ⑦ | ⑧ | ⑨ |
|---|---|---|---|---|---|---|---|---|---|
| 0 | A0 | B0 | A1 | B1 | 0 | | | 0 | |
| 1 | A2 | B2 | A3 | B3 | S0 | S1 | C1 | C1 | |
| 2 | A2 | B2 | S1 | C1 | S2 | S3 | C3 | 0 | C3 |

(OR) Folding Set: {FA0, FA2}, {FA1, FA3}

| $D_F(U \rightarrow V)$ | N*We-Pu+v-u |
|---|---|
| $D_F(0 \rightarrow 1)$ | 2*0-0+0-0=0 |
| $D_F(1 \rightarrow 2)$ | 2*0-1+1-0=0 |
| $D_F(2 \rightarrow 3)$ | 2*0-0+1-1=0 |