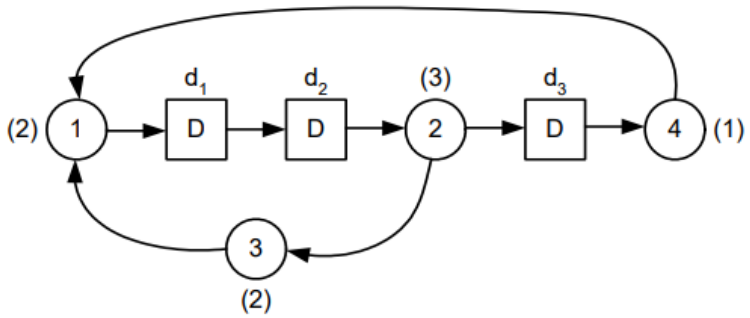
DSP in VLSI Design
Homework (V)

Unfolding
Reference Answer

1. In homework (II), you have computed the iteration bound of the following DFG. Please design a new DFG with unfolding to achieve this iteration bound.



In homework 2, we know the iteration bound = 7/2

The critical path of this DFG is 7 u.t., unfolding factor J = 2 is required

$U_i \rightarrow V_{(i+w)\%2}$ with $\left\lfloor \frac{i+w}{2} \right\rfloor$ delays

$1_0 \rightarrow 2_{(0+2)\%2}, \left\lfloor \frac{0+2}{2} \right\rfloor D$

$1_1 \rightarrow 2_{(1+2)\%2}, \left\lfloor \frac{1+2}{2} \right\rfloor D$

$2_0 \rightarrow 3_{(0+0)\%2}, \left\lfloor \frac{0+0}{2} \right\rfloor D$

$2_1 \rightarrow 3_{(1+0)\%2}, \left\lfloor \frac{1+0}{2} \right\rfloor D$

$3_0 \rightarrow 1_{(0+0)\%2}, \left\lfloor \frac{0+0}{2} \right\rfloor D$

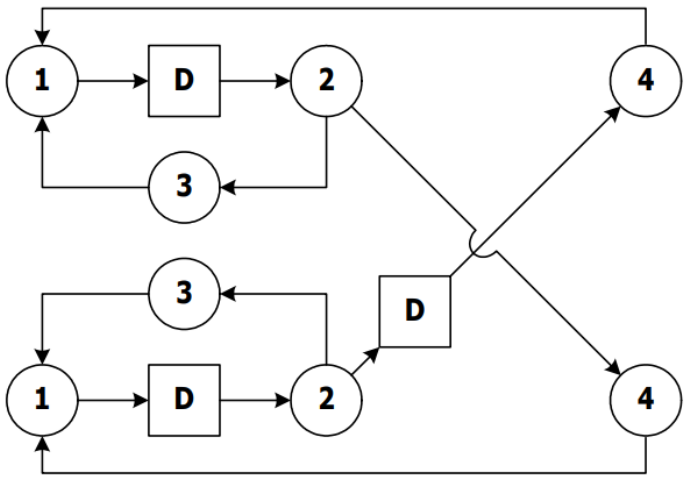
$3_1 \rightarrow 1_{(1+0)\%2}, \left\lfloor \frac{1+0}{2} \right\rfloor D$

$2_0 \rightarrow 4_{(0+1)\%2}, \left\lfloor \frac{0+1}{2} \right\rfloor D$

$2_1 \rightarrow 4_{(1+1)\%2}, \left\lfloor \frac{1+1}{2} \right\rfloor D$

$4_0 \rightarrow 1_{(0+0)\%2}, \left\lfloor \frac{0+0}{2} \right\rfloor D$

$4_1 \rightarrow 1_{(1+0)\%2}, \left\lfloor \frac{1+0}{2} \right\rfloor D$



2. In homework (III), you have designed a 3-parallel architecture for a direct-form FIR filter, $y(n) = ax(n) + bx(n-2) + cx(n-3)$. Please derive the 3-parallel architecture again by using the unfolding technique.

Unfolding factor J = 3

$U_i \rightarrow V_{(i+w)\%3}$ with $\left\lfloor \frac{i+w}{3} \right\rfloor$ delays