DSP in VLSI Design
Homework (III)

Pipelining and Parallel Processing
Reference Answer

1. Consider a direct-form implementation of the FIR filter

$$y(n) = ax(n) + bx(n-2) + cx(n-3)$$

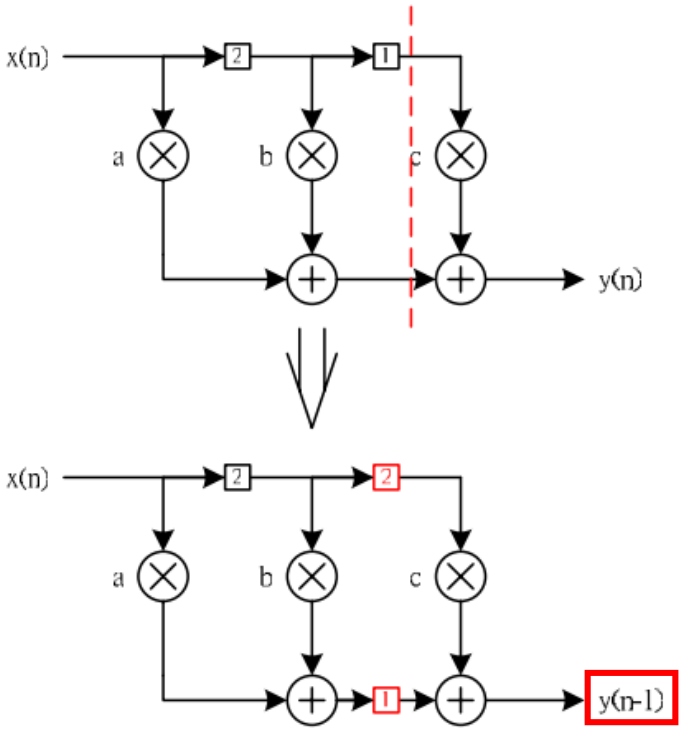
Assume that the time required for 1 multiply-add operation is T.

(a) Pipeline this filter such that the clock period is approximately T.

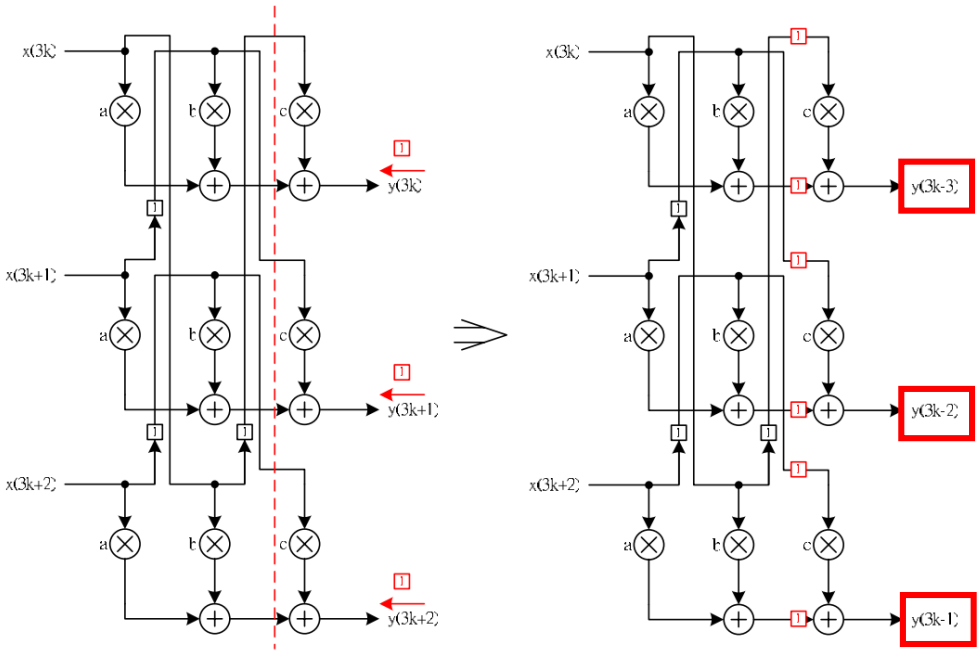
(b) Draw a block filter architecture for a block size of three. Pipeline this block filter such that the clock period is about T. What is the system sample rate?

(c) Pipeline the block filter in part (b) such that the block period is about T/2. Show the appropriate cutsets and label the outputs clearly. What is the system sample rate now? (Hint: you can use fine-grain pipelining.)

(a) Pipeline from y(n) with 1 delay. After retiming, the result is shown below.



(b)

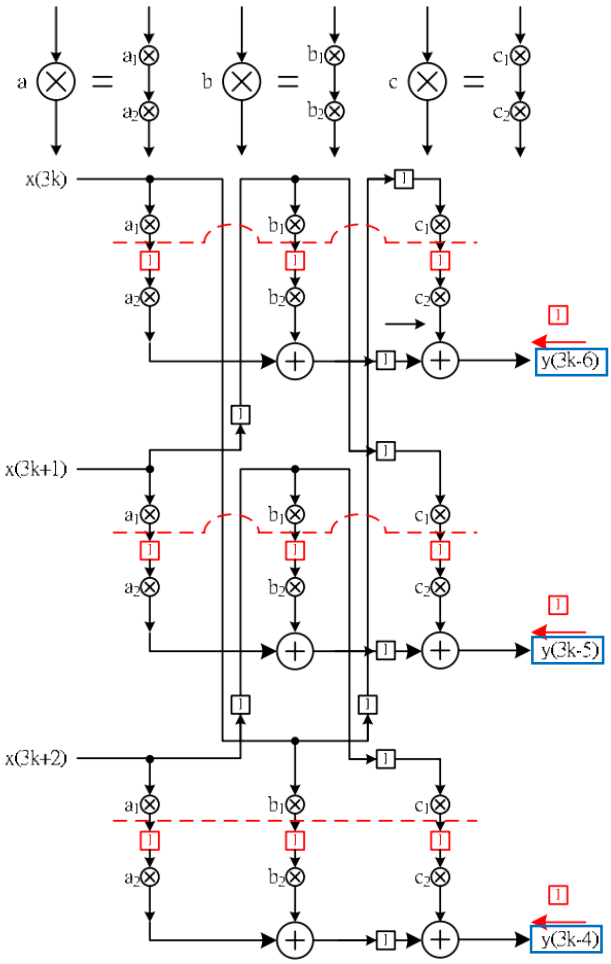


System sample rate = $(1/T_{sample})$

T_{sample} = T/3

System sample rate = 3/T

(c)



System sample rate = $(1/T_{sample})$

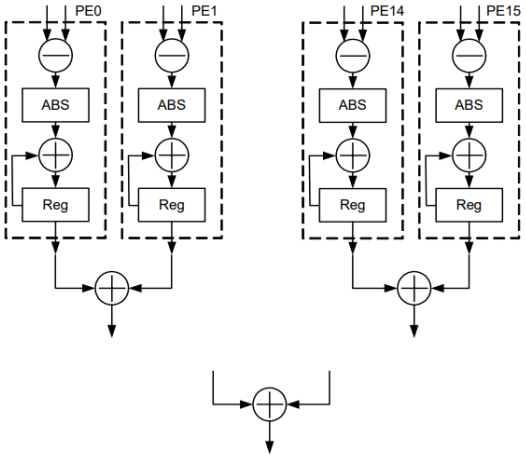
T_{sample} = (T/2)/3 = (T/6)

System sample rate = 6/T

2. Consider the core of a systolic array motion estimation architecture shown in the following figure. Assume the computation time of subtractor, absolutor, and adder are 5ns, 7ns, and 6ns, respectively.

(a) Where is the critical path? What is the maximum working frequency of this circuit?

(b) If we want to double the working frequency, please design the associated architecture.



(a) Two possible critical path:

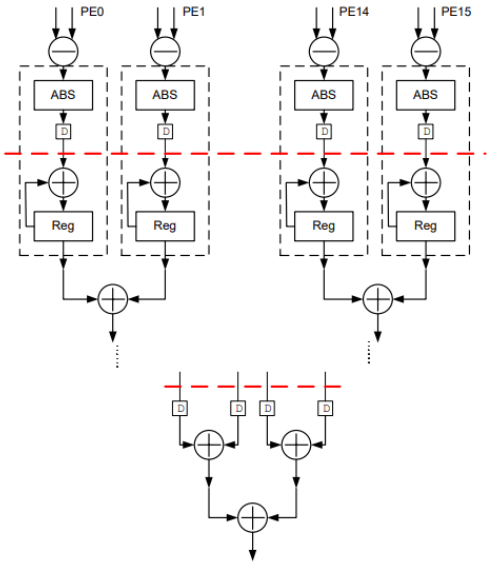
Sub → ABS → Add: 5+7+6=18 ns

Add → Add → Add → Add (Adder tree): 6 + 6 + 6 + 6 = 24 ns

Critical path: adder tree, 24ns

Maximum working frequency: 1/24ns = 42 MHz

(b) In this case, doubling the working frequency 1/24ns to 1/12ns, we should **pipeline the adder tree**, each step contain 2 adders. After that, **new critical path** is "Sub → ABS → Add", then we pipeline this path to fix T = 12ns, that means, "Sub → ABS → Reg → Add"



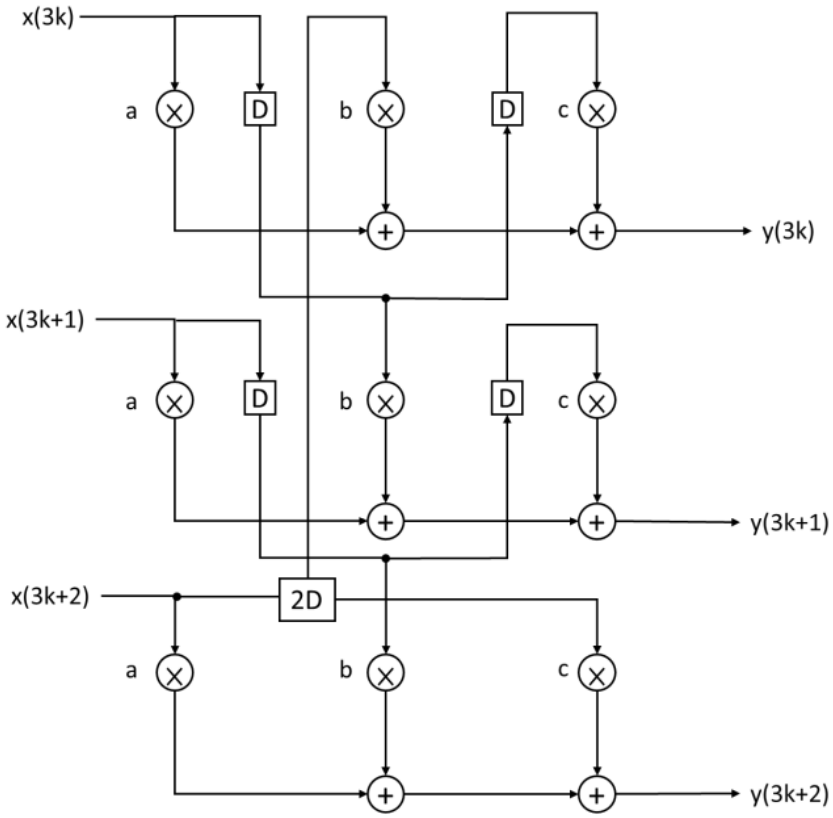
You can also consider other assumptions like four serial adders don't need 4x6 cycles or combining substractor and ABS operation to have faster version of the architecture.

3. Consider the 6-th-order FIR filter

$$y(n) = ax(n) + bx(n-4) + cx(n-6)$$

Draw the block diagram of this filter for block size of 3.

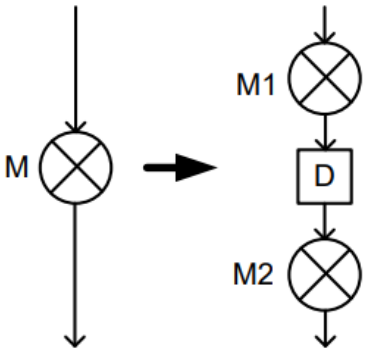
$$\begin{aligned} y(3k) &= ax(3k) + bx(3k-4) + cx(3k-6) \\ y(3k+1) &= ax(3k+1) + bx(3k-3) + cx(3k-5) \\ y(3k+2) &= ax(3k+2) + bx(3k-2) + cx(3k-4) \end{aligned}$$



4. For the example shown in Page 30 in the handout, with the same sampling period (9 u.t.).

(a) How is the new supply voltage?
(b) How is the power saving percentage?

We then employ fine-grained pipelining technique to further reduce the power consumption, that is, each multiplier is replaced with a pipelined multiplier as follows:



where T_M=8 u.t., T_{M1}=T_{M2}=4 u.t. ; C_M=8C_A, C_{M1}=C_{M2}=4C_A

(c) How is the new supply voltage?
(d) How is the power saving percentage?

(a)

$$T_{seq} = \frac{9C_A V_{cc}}{k(V_{cc} - V_t)^2}$$

$$T_{par} = 2T_{seq} = \frac{10C_A \beta V_{cc}}{k(\beta V_{cc} - V_t)^2}$$

$$\rightarrow 5\beta(V_{cc} - V_t)^2 = 9(\beta V_{cc} - V_t)^2$$

$$\rightarrow \beta = 0.6589 \text{ or } 0.0282 \quad (0.0282 \text{ is invalid})$$

New supply voltage is $\beta V_{cc} = 2.17437$ V

(b)

Power saving percentage is $1 - \beta^2 = 56.59\%$

(c)

$$T_{seq} = \frac{9C_A V_{cc}}{k(V_{cc} - V_t)^2}$$

$$T_{par,pip} = 2T_{seq} = \frac{6C_A \beta V_{cc}}{k(\beta V_{cc} - V_t)^2}$$

$$\rightarrow 3\beta(V_{cc} - V_t)^2 = 9(\beta V_{cc} - V_t)^2$$

$$\rightarrow \beta = 0.4828 \text{ or } 0.0385 \quad (0.0385 \text{ is invalid})$$

New supply voltage is $\beta V_{cc} = 1.59324$ V

(d)

Power saving percentage is $1 - \beta^2 = 76.69\%$

5. This example can give you more insights of the advantages of multi-core processors. Assume we have two processors fabricated in the same process with the threshold voltage in 1V. Processor A is a single-core processor with the supply voltage of 5V. For executing one specific task, the dynamic power consumption is 1W, where the static power consumption is 200mW, and the execution time is 10S. Processor B is a new design with four cores. We assume that the task can be perfectly executed in parallel, and there is no extra data accessing overhead for executing the same specific task on the quad-core processor. It is also assumed that the leakage current over unit circuit area is a constant.

(a) If Processor B employs the same supplied voltage. What are the advantages of the new design in terms of processing speed and energy consumption?

Because Processor A and Processor B employ the same supplied voltage, the working frequency can be the same.

Processor A:
- Computation time : 10S
- Dynamic power : 1W
- Static power : 0.2W
- Energy consumption : (1W+0.2W)×10S = 12J

Processor B:
- Computation time : 10S÷4 = 2.5S
- Dynamic power : 1W×4 = 4W
- Static power : 0.2W×4 = 0.8W
- Energy consumption : (4W+0.8W)×2.5S = 12J

→ Computation time becomes 1/4, and energy consumption is the same.

(b) If it is allowed to lower the supply voltage to 4V for Processor B. What are the advantages of the new design in terms of processing speed and energy consumption?

Because the supplied voltage of Processor B reduce to 4V, the trainsition time (propagation delay) may become longer, then we have to reduce the working frequency of Processor B.

$T_{seq} = \frac{C_A V_{cc}}{k(V_{cc}-V_t)^2}$, $T_{seq} \alpha \frac{V_{cc}}{(V_{cc}-V_t)^2}$, so the computation becomes $\frac{4}{(4-1)^2} \div \frac{5}{(5-1)^2} = \frac{64}{45}$
Working frequency becomes to $\frac{45}{64}$
New Processor B:
- Computation time : 10S÷4× $\frac{64}{45} = \frac{32}{9}$ S
- Dynamic power : CV^2f → 1W×$(\frac{4}{5})^2$×$\frac{45}{64}$ × 4 = 1.8W
- Static power : $I_{leakage}V$ → 0.2W× $\frac{4}{5}$ ×4 = 0.64W
- Energy consumption : (1.8W+0.64W)×$\frac{32}{9}$S ≈ 8.68J

→ Computation time becomes 1/2.8, and energy consumption is smaller than Processor A.