Logic Synthesis & Verification, Fall 2023

National Taiwan University

Problem Set 4

(Due by 2023/12/08 23:59.)

1 Weak Division

(10%) Given an expression F and a divisor G, suppose $F = G \cdot H + R$ by weak division, that is, $H = F/G$. Prove that H and R are unique.

2 [Kernelling and Factoring]

(20%) Let

$$F = ad + ae + af + bcd + bce + bcf + de + df.$$

(a) (5%) Compute $\texttt{KERNEL}(0, F)$ with literals ordered alphabetically. Draw the kernelling tree (as in the slides) and list the kernels and their corresponding co-kernels.
(b) (5%) Compute all 2-cube divisors and 2-literal cube divisors (including those after complementation). For each 2-cube divisor, indicate whether or not it is a kernel.
(c) (5%) Apply `GFACTOR` on F by using the largest level-0 kernels as the divisors and using weak division. (In case that there are several choices of divisors, using one of them is sufficient.)
(d) (5%) Apply `GFACTOR` on F by using the 2-cube divisors with literals appearing most frequently in F and using weak division. (Exclude divisors that result in trivial division with the quotient equal to constant 1. Also, in case that there are several choices of divisors, using one of them is sufficient.)

3 [Extraction and Rectangle Covering]

(10%) Let

$$F = abc + aef + bcd + be + ce + def$$
$$G = abcd + abe + ace + adef + bdf + cdf.$$

Perform extraction using rectangle covering to simplify F and G such that the number of literals in the entire Boolean network is minimized (consider only level-0 kernels).

4 [Functional Dependency]

(10%) Given a function vector $\boldsymbol{f} = (f_1, f_2, f_3)$ over input variables $\boldsymbol{x} = (a, b, c, d, e)$ with

$$f_1 = a'b'd' + bce + b'de' + d'e$$
$$f_2 = be + bc'd$$
$$f_3 = a'd' + a'b'e' + b'd'e' + ade.$$

Determine, by BDD-based computation, whether f_1 can be re-expressed with a function $h(y_2, y_3)$ for variables y_2 and y_3 being the output variables of functions f_2 and f_3. If yes, what is the h function?

5 [SDC and ODC]

(15%) Consider the Boolean network of Figure 1.

(a) (5%) Write down a Boolean formula for the SDC of the entire network.
(b) (5%) Write down a Boolean formula for the satisfiability don't cares SDC_4 of Node 4. Since SDC_4 is imposed by the fanins of Node 4, the formula should depend on variables $x_1, \ldots, x_4, y_1, \ldots, y_3$. How can you make SDC_4 only depend on y_1, y_2, y_3 such that we can minimize Node 4 directly?
(c) (5%) Compute the observability don't cares ODC_4 of Node 4.

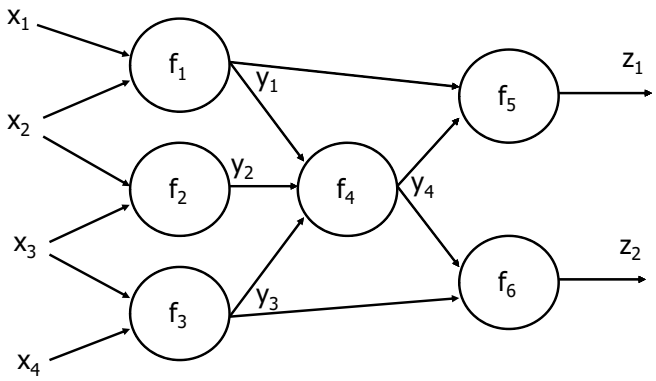

Fig. 1. A Boolean network, where $f_1 = x_1 \vee \neg x_2$, $f_2 = \neg x_2 x_3$, $f_3 = \neg x_3 \neg x_4$, $f_4 = \neg y_1 \neg y_2 \vee y_2 \neg y_3 \vee y_1 \neg y_3$, $f_5 = y_1 \vee y_4$, and $f_6 = y_3 y_4$.

6 [Don't Cares in Local Variables]

(10%) Consider the Boolean network of Figure 1. Suppose the XDC for z_1 is $\neg x_1 \neg x_2 \neg x_3 x_4$ and that for z_2 is $x_1 x_2 \neg x_3 x_4$.

(a) (5%) Compute the don't cares D_4 of Node 4 in terms of its local input variables y_1, y_2, and y_3. (Note that in general the computation of ODC may be affected by XDC especially when there exist different XDCs for different primary outputs.)
(b) (5%) Based on the computed don't cares, what is the best implementable function for Node 4 (in terms of the literal count and cube count in SOP)?

7 [Complete Flexibility]

(25%) Consider the Boolean network of Figure 1. Let $Y = \{y_1, y_2, y_3\}$.

(a) (5%) Suppose the XDC for z_1 is $\neg x_1 \neg x_2 \neg x_3 x_4$ and that for z_2 is $x_1 x_2 \neg x_3 x_4$. Write down the specification relation $S(X, Z)$.
(b) (5%) What is the influence relation $I(X, y_4, Z)$ of Node 4?
(c) (5%) What is the environment relation $E(X, Y)$ of Node 4?
(d) (5%) What is the complete flexibility $CF_4(Y, y_4)$ of Node 4?
(e) (5%) Is the previously computed don't care set D_4 of Node 4 subsumed (contained) by CF_4?

8 [Complete Flexibility for Multi-Nodes]

(Bonus Question) (20%) Compute the complete flexibility $CF(x_1, x_2, x_3, y_1, y_2)$ for combined nodes y_1 and y_2 in the following circuit. Simplify the circuit as much as possible based on the flexibility.

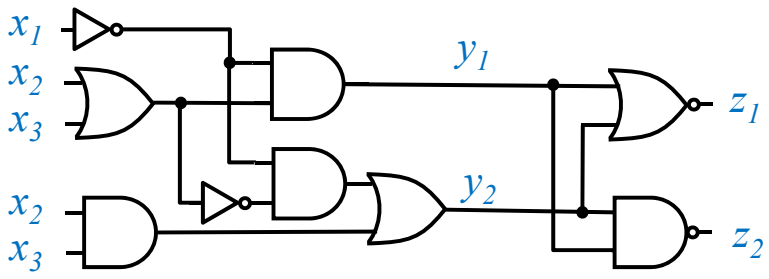

Fig. 2. Circuit under simplification.