Logic Synthesis & Verification, Fall 2023

National Taiwan University

Problem Set 5

Due on 2023/12/18 by 8:00.

1 [Technology Mapping]

(36%)

(a) (6%) Specify the two criteria that make a collection of pattern graphs form a legal cover of technology mapping for a given subject graph.
(b) (10%) Given the subject graph of Figure 1, perform SAT based technology mapping to find a legal mapping solution using the library of Figure 2. Show the CNF formula and give a legal mapping solution.
(c) (10%) Given the subject graph of Figure 1, explore different tree partitioning options of the subject graph and perform the DAGON (dynamic programming) algorithm on each tree to find an area-minimum mapping solution using the library of Figure 2 assuming the cost specified in Figure 2 corresponds to gate area. Show all intermediate costs and the final optimum covering.
(d) (10%) Repeat (c), but find a delay-minimum mapping solution assuming the cost specified in Figure 2 corresponds to gate delay. Show all intermediate costs and the final optimum covering.

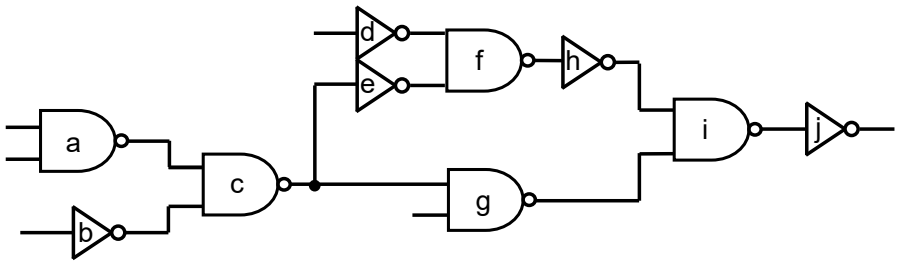

Fig. 1. Subject graph under technology mapping.

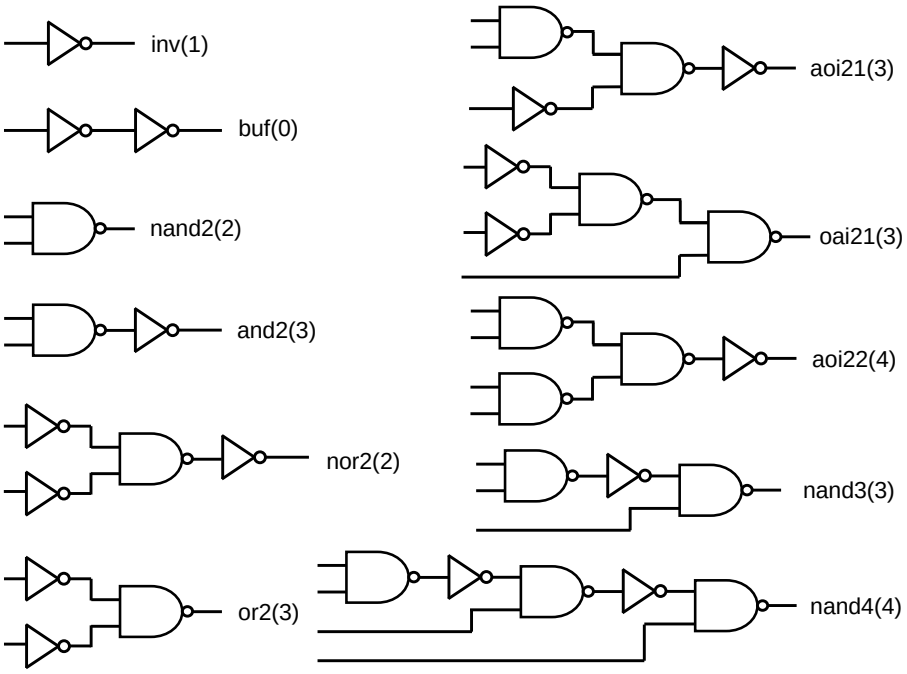

Fig. 2. Pattern graphs.

2 [Timing Critical Region Property]

(10%) Consider static timing analysis of a circuit. Prove that the critical region in which the slack values are less than or equal to some constant c must consist of paths connecting primary inputs and primary outputs.

3 [Static Timing Analysis]

(24%)

(a) (20%) Given the circuit of Figure 3, compute the *arrival time*, *required time*, and *slack* of every net.
(b) (4%) Identify the critical region (consisting of gates and wires) with negative slacks in Figure 3. Justify the property stated in Problem 2.

4 [Functional Timing Analysis]

(30%) Consider the circuit of Figure 3.

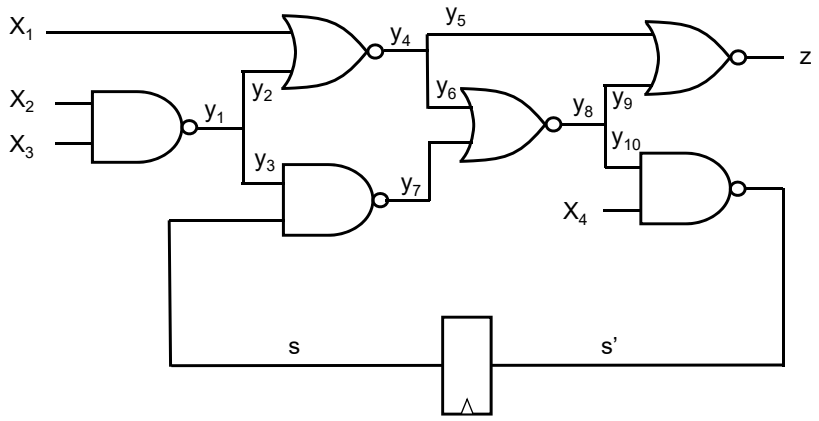

Fig. 3. A circuit under timing analysis, where the clock period is set to 10 ns, the propagation delay and the setup time of the flip-flop are both 1 ns, arrival times for all of the primary inputs are 0, the gate delay of a NAND gate is 2 ns, and the gate delay of a NOR gate is 3 ns.

(a) (5%) Perform X-valued simulation on the circuit to determine the signal steady time for every net under the assignment $x_1 = x_2 = x_3 = x_4 = s = 1$.
(b) (12%) Perform the SAT-based functional timing analysis on the circuit to determine the longest true delay.
(c) (8%) Given the satisfying assignment in (b) establishing the longest true delay, identify the corresponding longest true delay path. (Hint: You may need the *exact sensitization criterion*, that is, the delay at a gate is determined by 1) the earliest arrival input with a controlling value, or 2) the latest arrival input when all inputs are of non-controlling values.)
(d) (5%) Continuing (b), determine the minimum clock cycle of the circuit.