Logic Synthesis & Verification, Fall 2023

National Taiwan University

Reference Solution to Problem Set 5

Due on 2023/12/18 8:00.

1 [Technology Mapping]

(a) Given a subject graph, a cover is a collection of pattern graphs such that

(1) every node of the subject graph is contained in one or more pattern graphs, and

(2) each input required by a pattern graph is a PI or an output of some other pattern graph.

(b) Let the inputs be x_1, x_2, x_3, x_4, x_5 respectively, as shown in figure 1.

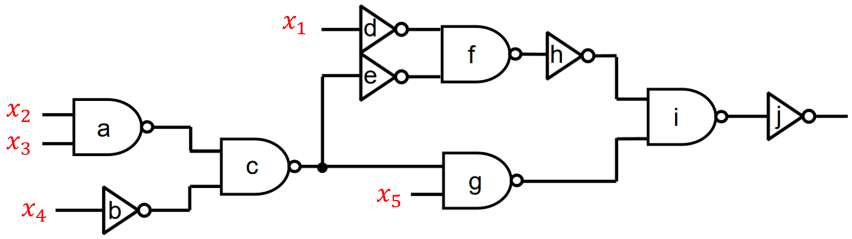

Fig. 1: The subject graph with named input.

The possible matches for all nodes are as shown in table 1.
First, we generate the clauses for constraint (1).

$$\begin{aligned} C_1 =&(m_1 + m_7)(m_2 + m_7)(m_3 + m_6 + m_7 + m_{10} + m_{11})(m_4 + m_9 + m_{14}) \\ &(m_5 + m_6 + m_7 + m_9 + m_{10} + m_{14} + m_{17}) \\ &(m_8 + m_9 + m_{10} + m_{13} + m_{14} + m_{16} + m_{17})(m_{11} + m_{20}) \\ &(m_{12} + m_{13} + m_{14} + m_{16} + m_{17} + m_{20}) \\ &(m_{15} + m_{16} + m_{17} + m_{19} + m_{20})(m_{18} + m_{19} + m_{20}) \end{aligned}$$

Table 1: The possible matches for all nodes.

Match	Gate	Cost	Inputs	Root	Covers
m_1	nand2	2	x_2, x_3	a	a
m_2	inv	1	x_4	b	b
m_3	nand2	2	a, b	c	c
m_4	inv	1	x_1	d	d
m_5	inv	1	c	e	e
m_6	and2	3	a, b	e	c, e
m_7	aoi21	3	x_2, x_3, x_4	e	a, b, c, e
m_8	nand2	2	d, e	f	f
m_9	or2	3	x_1, c	f	d, e, f
m_{10}	nand3	3	a, b, d	f	c, e, f
m_{11}	nand2	2	x_5, c	g	g
m_{12}	inv	1	f	h	h
m_{13}	and2	3	d, e	h	f, h
m_{14}	nor2	2	x_1, c	h	d, e, f, h
m_{15}	nand2	2	g, h	i	i
m_{16}	nand3	3	d, e, g	i	f, h, i
m_{17}	nand4	4	a, b, d, g	i	c, e, f, h, i
m_{18}	inv	1	i	j	j
m_{19}	and2	3	g, h	j	i, j
m_{20}	aoi21	3	x_5, c, f	j	g, h, i, j

Then, we generate the clauses for constraint (2).

$$
\begin{aligned}
C_2 =&(m_3' + m_1)(m_3' + m_2)(m_5' + m_3)(m_6' + m_1)(m_6' + m_2)\\
&(m_8' + m_4)(m_8' + m_5 + m_6 + m_7)(m_9' + m_3)(m_{10}' + m_1)(m_{10}' + m_2)(m_{10}' + m_4)\\
&(m_{11}' + m_3)(m_{12}' + m_8 + m_9 + m_{10})(m_{13}' + m_4)(m_{13}' + m_5 + m_6 + m_7)(m_{14}' + m_3)\\
&(m_{15}' + m_{11})(m_{15}' + m_{12} + m_{13} + m_{14})(m_{16}' + m_4)(m_{16}' + m_5 + m_6 + m_7)(m_{16}' + m_{11})\\
&(m_{17}' + m_1)(m_{17}' + m_2)(m_{17}' + m_4)(m_{17}' + m_{11})(m_{18}' + m_{15} + m_{16} + m_{17})\\
&(m_{19}' + m_{11})(m_{19}' + m_{12} + m_{13} + m_{14})(m_{20}' + m_3)(m_{20}' + m_8 + m_9 + m_{10})
\end{aligned}
$$

The whole CNF formula is $C_1 \wedge C_2$. A satisfying solution is $m_1, m_2, m_3, m_9, m_{20}$ assigned to 1, and other variables assigned to 0.

(c) The results of two different tree partitioning options are shown in figure 2 and figure 3, respectively. The pattern graphs in red text are selected. The red and blue boxes indicate the nodes covered by the selected pattern graphs.

(d) The result is shown in Fig. 4, respectively. The pattern graphs in red text are selected. The red and blue boxes indicate the nodes covered by the selected pattern graphs.

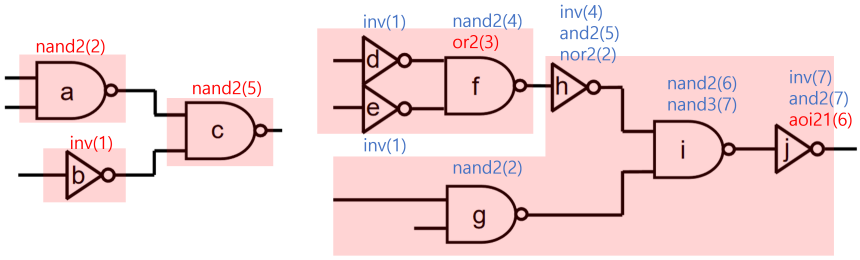

Fig. 2: Performing DAGON with trivial partition (two trees.) The resulting optimum covering has an area of $6 + 5 = 11$.

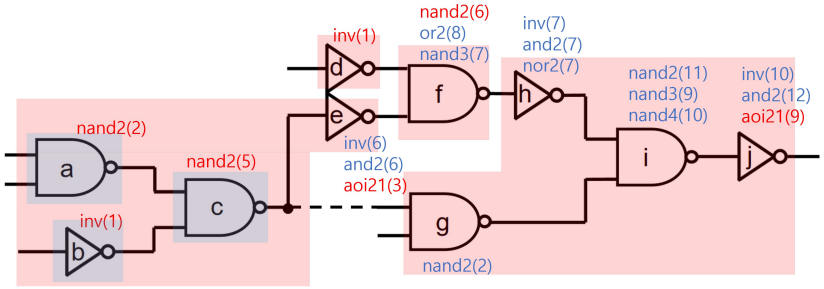

Fig. 3: Performing DAGON with single-cone partition. The resulting optimum covering has an area $9 + 5 = 14$.

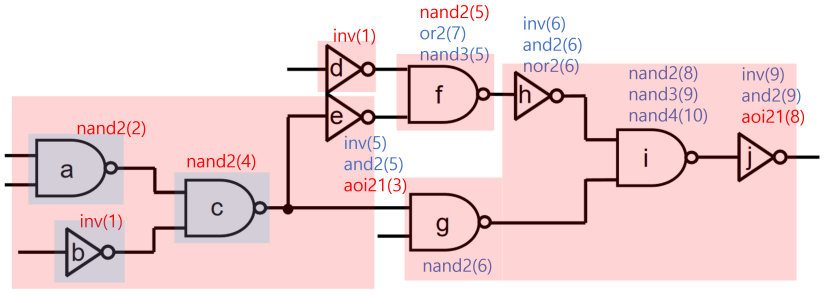

Fig. 4: Performing DAGON. The resulting optimum covering has a delay of 8.

2 [Timing Critical Region Property]

Let e be an edge (wire segment) from node X to node Y with slack value $S(e) \leq c$. Note that a node can be a gate, primary output (PI), primary input (PO), or a connection between a fanout stem and fanout branches. Let the fanin edges of X be $x_1, \cdots, x_n$, and the fanout edges of Y be $y_1, \cdots, y_m$. Let $D(X)$ denotes the delay of node X. Let $A(e), R(e), S(e)$ denote the arrival time, required time, and slack value respectively.

Lemma 1. *If X is not a PI, there exists a fanin edge x_i such that $S(x_i) \leq S(e)$.*

Proof: $R(x_i) \leq R(e) - D(X)$ for all x_i. Also, since $A(e) = \max\{A(x_1), \cdots, A(x_n)\} + D(X)$, there exists x_i s.t. $A(x_i) = A(e) - D(X)$. Therefore,

$$S(x_i) = R(x_i) - A(x_i) \leq (R(e) - D(e)) - (A(e) - D(e)) = S(e).$$

Lemma 2. *If Y is not a PO, there exists a fanout edge y_i such that $S(y_i) \leq S(e)$.*

Proof: $A(y_i) \geq R(e) + D(Y)$ for all y_i. Also, since $R(e) = \min\{R(y_1), \cdots, R(y_m)\} - D(X)$, there exists y_i s.t. $R(y_i) = R(e) + D(Y)$. Therefore,

$$S(y_i) = R(y_i) - A(y_i) \leq (R(e) + D(e)) - (A(e) + D(e)) = S(e).$$

As a result, for any edge e with slack $S(e) \leq c$ in the critical region, a path P from PI to PO containing e s.t.

$$S(x) \leq S(e) \leq c \quad \forall x \in P$$

must exist according to lemma 1 and lemma 2. Thus, all the edges in the region belong to some paths in this region from PIs to POs. Therefore, the region must consist of paths from PI to PO.

3 [Static Timing Analysis]

(a) The result is shown in Table 2.
(b) The critical region with negative slack is shown as the red region in Fig. 5, which indeed contains PIs (x_2 and x_3) and POs (z and s').

4 [Functional Timing Analysis]

(a) The result is shown in Fig. 6.
(b) Based on the results of Problem 3(b) and Problem 4(a), the longest true delay should fall in the range $[10, 11]$. We first try the possibility that the longest true delay $L = 10$. Note that the propagation delay and setup time are considered.

$$z(0, t = 10) = \ y_4(1, t = 7) \cup y_8(1, t = 7)$$

Table 2: Static Timing Analysis

Wire	Arrival Time (ns)	Required Time (ns)	Slack (ns)
x_1	0	1	1
x_2	0	-1	-1
x_3	0	-1	-1
x_4	0	7	7
s	1	2	1
y_1	2	1	-1
y_2	2	1	-1
y_3	2	2	0
y_4	5	4	-1
y_5	5	7	2
y_6	5	4	-1
y_7	4	4	0
y_8	8	7	-1
y_9	8	7	-1
y_{10}	8	7	-1
z	11	10	-1
s'	10	9	-1

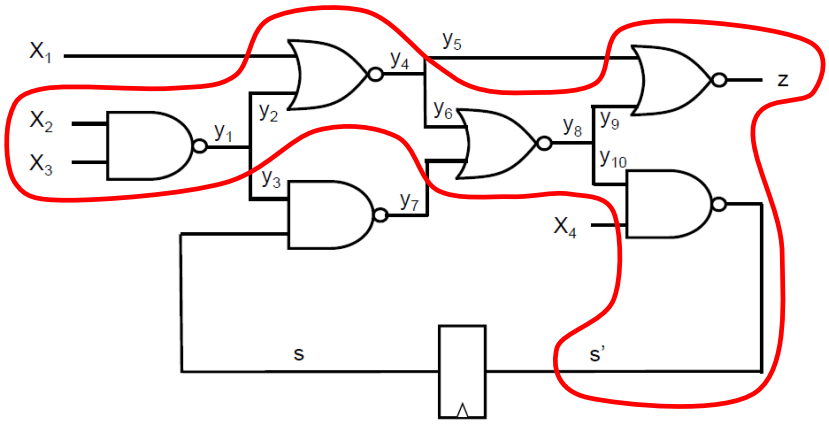

Fig. 5: Critical region.

$$
\begin{aligned}
&= [x_1(0, t=4) \cap y_1(0, t=4)] \cup [(y_4(0, t=4) \cap y_7(0, t=4)] \\
&= [x_1(0, t=4) \cap x_2(1, t=2) \cap x_3(1, t=2)] \\
&\cup [[x_1(1, t=1) \cup y_1(1, t=1)] \cap [s(1, t=2) \cap y_1(1, t=2]] \\
&= [x_1(0, t=4) \cap x_2(1, t=2) \cap x_3(1, t=2)] \\
&\cup [x_1(1, t=1) \cap y_1(1, t=2) \cap s(1, t=2)] \cup [y_1(1, t=1) \cap s(1, t=2)] \\
&= [x_1(0, t=4) \cap x_2(1, t=2) \cap x_3(1, t=2)] \\
&\cup [x_1(1, t=1) \cap [x_2(0, t=0) \cup x_3(0, t=0)] \cap s(1, t=2)] \\
&\cup [[x_2(0, t=-1) \cup x_3(0, t=-1)] \cap s(1, t=2)] \\
&= [\neg x_1 x_2 x_3] \vee [x_1(\neg x_2 \vee \neg x_3)s] \vee [0 \wedge s] \\
&= \neg x_1 x_2 x_3 \vee x_1 \neg x_2 s \vee x_1 \neg x_3 s
\end{aligned}
$$

$$
\begin{aligned}
z(1, t=10) = \; & y_4(0, t=7) \cap y_8(0, t=7) \\
= \; & [x_1(1, t=4) \cup y_1(1, t=4)] \cap [(y_4(1, t=4) \cup y_7(1, t=4)] \\
= \; & [x_1(1, t=4) \cup x_2(0, t=2) \cup x_3(0, t=2)] \\
& \cap [[x_1(0, t=1) \cap y_1(0, t=1)] \cup s(0, t=2) \cup y_1(0, t=2)] \\
= \; & [x_1(1, t=4) \cap x_1(0, t=1) \cap y_1(0, t=1)] \\
& \cup [x_1(1, t=4) \cap s(0, t=2)] \\
& \cup [x_1(1, t=4) \cap y_1(0, t=2)] \\
& \cup [x_2(0, t=2) \cap x_1(0, t=1) \cap y_1(0, t=1)] \\
& \cup [x_2(0, t=2) \cap s(0, t=2)] \\
& \cup [x_2(0, t=2) \cap y_1(0, t=2)] \\
& \cup [x_3(0, t=2) \cap x_1(0, t=1) \cap y_1(0, t=1)] \\
& \cup [x_3(0, t=2) \cap s(0, t=2)] \\
& \cup [x_3(0, t=2) \cap y_1(0, t=2)] \\
= \; & 0 \vee x_1 \neg s \vee x_1 x_2 x_3 \vee 0 \vee \neg x_2 \neg s \vee 0 \vee 0 \vee \neg x_3 \neg s \vee 0 \\
= \; & x_1 \neg s \vee x_1 x_2 x_3 \vee \neg x_2 \neg s \vee \neg x_3 \neg s
\end{aligned}
$$

We find that $z(0, t=10) \vee z(1, t=10) \neq 1$. For example, $\neg x_1 \neg x_2 \neg x_3 \neg x_4\, s$ is a satisfying assignment of $\neg[z(0, t=10) \vee z(1, t=10)]$. Therefore, there exist some input patterns making z not stable at value 0 or 1 at time 10, so the longest true delay must be longer than 10. Therefore, the longest true delay is 11.

(c) By conducting X-valued simulation under the assignment $x_1 = x_2 = x_3 = x_4 = 0$, $s = 1$, as shown in Fig. 7, we can find that the critical path is x_2(or x_3) $\rightarrow y_1 \rightarrow y_2 \rightarrow y_4 \rightarrow y_6 \rightarrow y_8 \rightarrow y_9 \rightarrow z$.

(d) The minimum clock cycle is 11 ns.

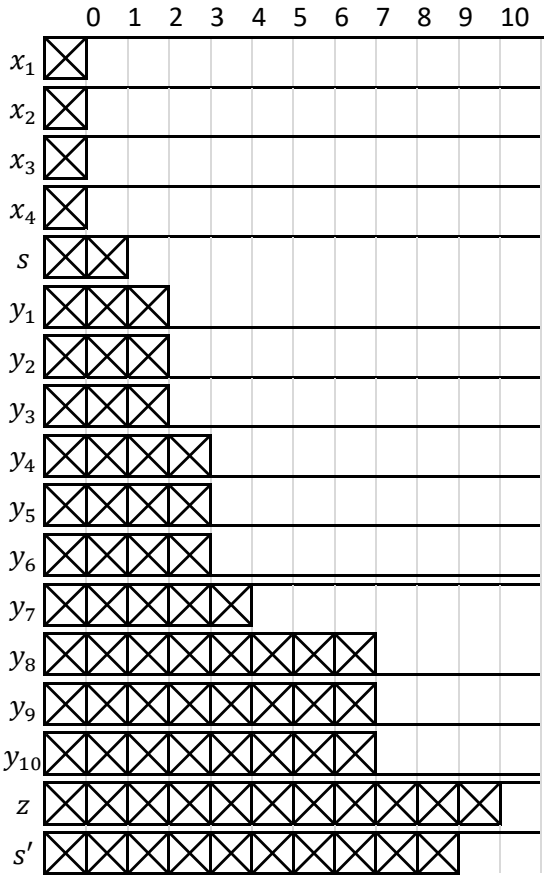

Fig. 6: X-valued simulation for Problem 4(a).

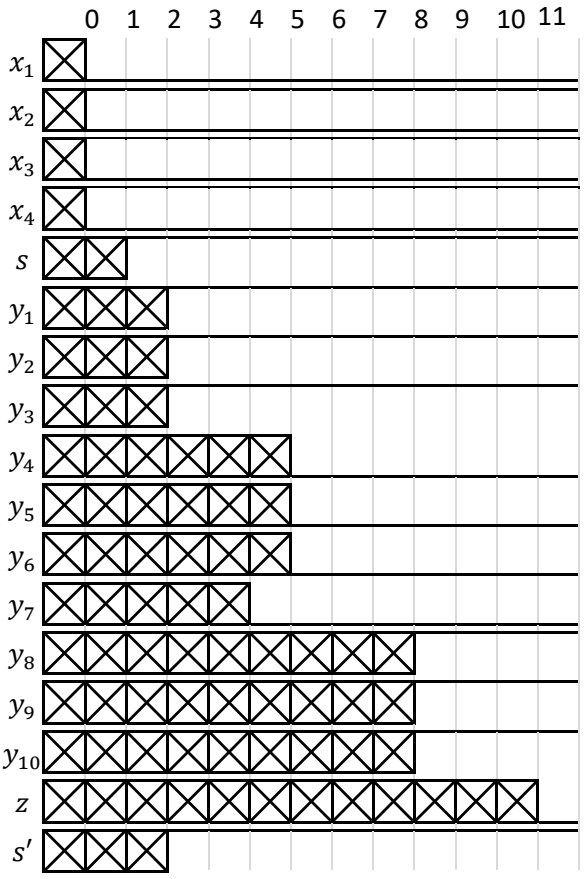

Fig. 7: X-valued simulation for Problem 4(c).