Introduction to Processor Architecture

32 BITS 2-STAGE PIPELINE PROCESSOR

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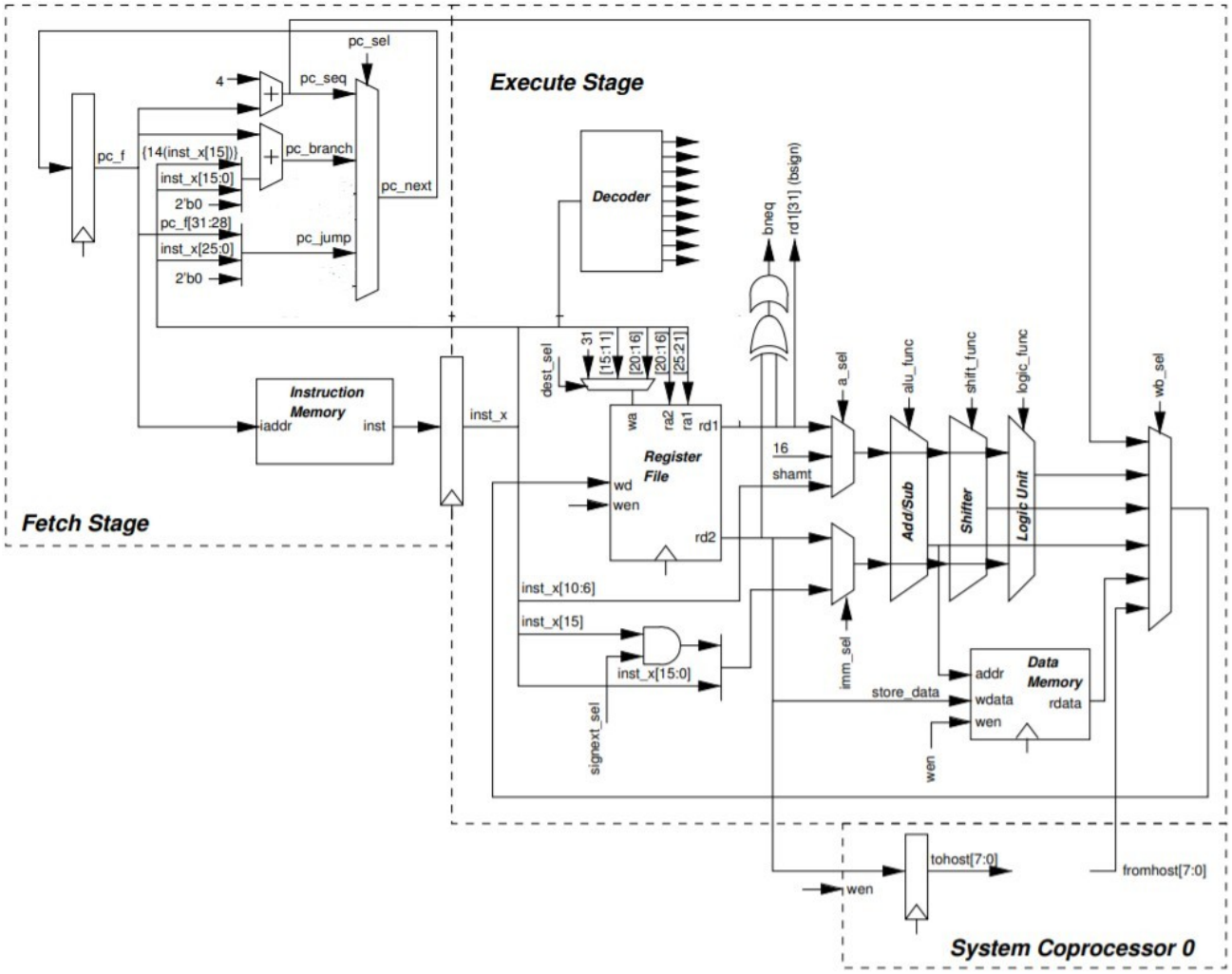
Contents

1. Architecture of the Processor



2. Main Memory Design

The Memory is a Harvard style architecture. There is a separate Data and Instruction Memory. Big Endian ordering is used in this processor.

3. Design of Experiment

3.1 Instructions Supported

• ADD
• SUB
• SLT
• SLTU
• AND
• OR
• NOR
• XOR
• SLL
• SLLV
• SRA
• SRAV
• SRL
• SRLV
• ADDI
• ANDI
• SLTI
• SLTIU
• ORI
• XORI
• BGTZ
• BLEZ
• BNE
• BEQ
• SW
• LW
• JUMP

3.2 Instructions not supported

• ADDU
• ADDIU
• DIV
• DIVU
• MULT
• MULTU
• SUBU
• JAL
• JALR
• JR
• LB
• LBU
• LH
• LHU
• SH
• SB
• Data movement Instructions
• TRAP Instructions

3.3 Clock Frequency

The processor works at 0.1GHz with clock at 10ns.

4.BIBLIOGRAPHY

For Design

• The picture is taken from 2-stage processor slide on Moodle

For Simulation

• Designing and Simulation credits: Vivado