RAJIV **G**ANDHI **U**NIVERSITY OF **K**NOWLEDGE **T**ECHNOLOGIES

Department of
Electronocis & **C**ommunication **E**ngineering

ANALOG ELECTRONIC CIRCUITS LAB

INDEX

I. LIST OF EXPERIMENTS:--

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2. D.C. characterization and finding ac model parameters of a MOSFET.
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4. Design of amplifiers with MOSFET.
5. Design and characterization of simple current mirror circuits using BJT and MOSFET.
6. Design and characterization of cascode current mirror circuits using BJT and MOSFET.
7. Design of Common collector amplifier
8. Design of differential amplifier using BJT with resistive load.
9. Design of differential amplifier using MOSFET with active load.

II.LIST OF EQUIPMENT:-

SLNO	NAME	RANGE	QUANTITY	DATE OF ARRIVAL
1	Digital CRO		26	01/07/11
2	RPS		24	29/06/11
3	Function Generator	3MHz-With Modulation	26	22/06/11
4	Multimeter	MASTECH	34	28/07/11
5	Bread board	----------	31	28/07/11
6	CRO demonstrator	20 MHz-Dual channel	1	22/06/11
7	Tables		12	04/08/11
8	Faculty chair		1	12/09/11
9	Student stools		25	12/09/11

Procedure Followed in Lab:

Arrangement in the lab:

Equipment is arranged on the table in such a way that two batches of students can use a single table.Students are divided into batches of three.So on each table 6 students would be working.(Separate equipment for separate batches)

What is expected from the student?

Dress code has to be strictly followed in the lab.The lab is totally of 3 hrs duration during which the student is expected finish the experiment.Each and every student should submit their report of the previous experiment.Every student has to have an idea over the experiment that is to be done in that session.With that he/she has to prepare a list of the equipment necessary which is to be submitted to the particular lab assistant.

Role of the Lab assistant:

Lab assistant would take attendance right at the beginning of the session .He/she has to check if everyone has submitted their report.Later after the students submit their list of equipment he/she should acknowledge the list provided by the students and provide them with the Equipment.While students do the experiment if they have any problem or doubt,Lab assistants would clarify it.Lab assistants would help them during the entire session in doing the experiment.

III. LAB MANUAL

Experiment no:1

DC CHARACTERIZATION AND FINDING AC MODEL PARAMETERS OF A BJT

AIM: a) To obtain common emitter characteristics of npn transistor
b) To find ac model parameters of BJT

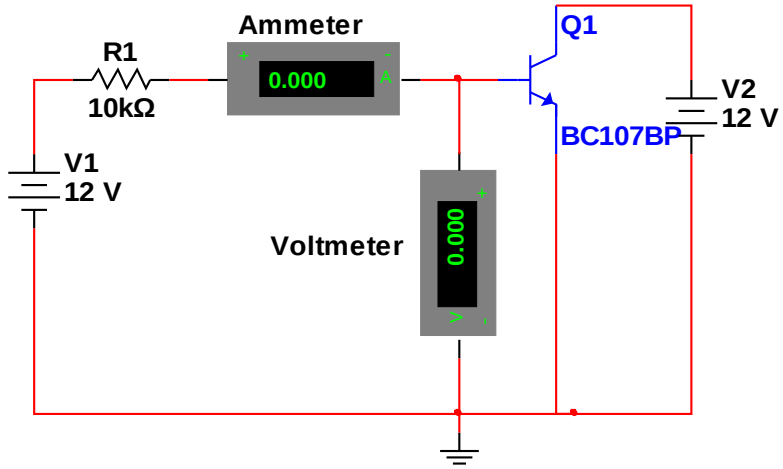


Figure 1.1

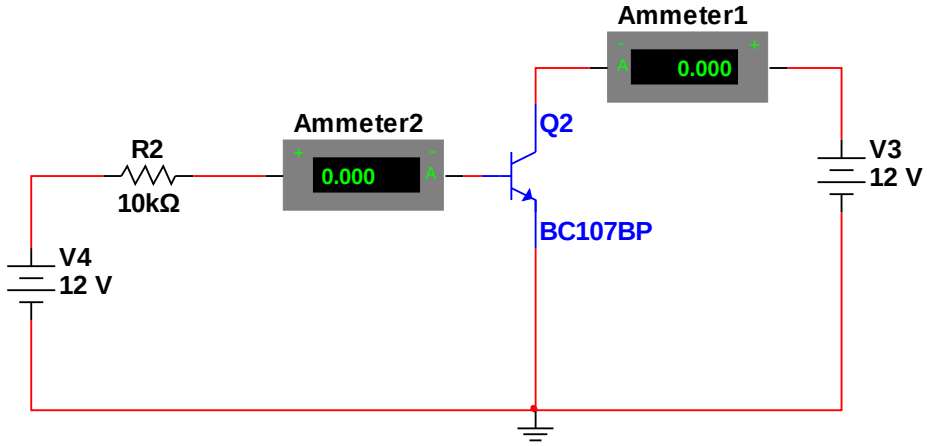


Figure 1.2

Theory:

Transistor is an active three terminal device. The three terminals are collector,base and emitter. We can connect these three terimianls in three different configurations. When emitter is common to both input and output ports, this type of configuration is known as common emitter. Input is applied to base and output is grwan form collector side.

Input characteristics are obtained by keepin V_{CE} constant and varying V_{BE} and measuring I_B value input characteristics are drawn between by keeping V_{CE} constant where for a small change in V_{BE} Vs I_B changes to sudden increment that voltage known as cutin voltage

Output characteristics will be obtained by keeping I_B constant and plot V_{CE} Vs I_C after certian V_{CE} , I_C will increase very slowly and saturates

Procedure:-

a) connect the circuit asper the diagram .

b) By keeping VCE=0 vary the VBE voltage and observe the corresponding IB Values.

c) Tabulate mesured values.

d) Repeat the above steps for different values of VCE

e) Plot the graph betwen VBE and IB

For output Characteristics:

a) connect the circuit asper the diagram .

b)By keeping IB vary the VCE voltage and observe the corresponding IC Values.

c) Tabulate mesured values.

d) Repeat the above steps for different values of VCE

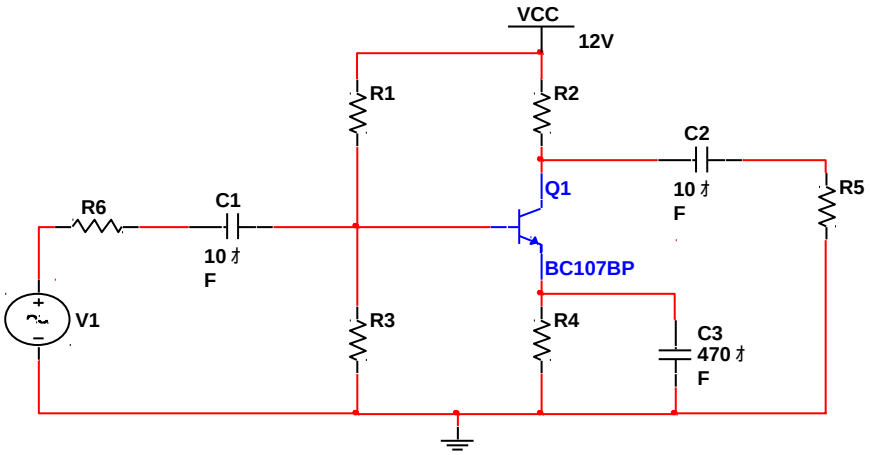
e) Plot the graph betwen VCE and IC at a constant value of IB.

Result:

Experiment no:2

DESIGN OF COMMON EMITTER AMPLIFIER

Aim:-
To design CE amplifier to find the frequency response of CE amplifier.



Theory:-
It has moderately low input resistance
its output resistance is moderately large
its current gain is high
it has very high voltage gain in the order of 1500 or so.
It produces very high power gain in the order of 10,000
it produces phase reversal of input signal.

Designing procedure:-

Let V_{CC}=12v
$V_{CE} \leq V_{CC}/2$
$V_E \leq Vcc/10$

Let I_E =2mA
$R_E=V_E/I_E$
$R_C=(V_{CC}-V_{CE}-V_E)/I_C$
$V_B=V_{BE}+V_E$

PROCEDURE:-

1)Take the components according to the teroritical design values.
2) connect the circuit as per the ckt diagram.
3) Apply DC input to circuit and mesure the DC conditions and notedown the values.
4) Apply AX signla using function gentator and connect the output across the

collector resistor RC

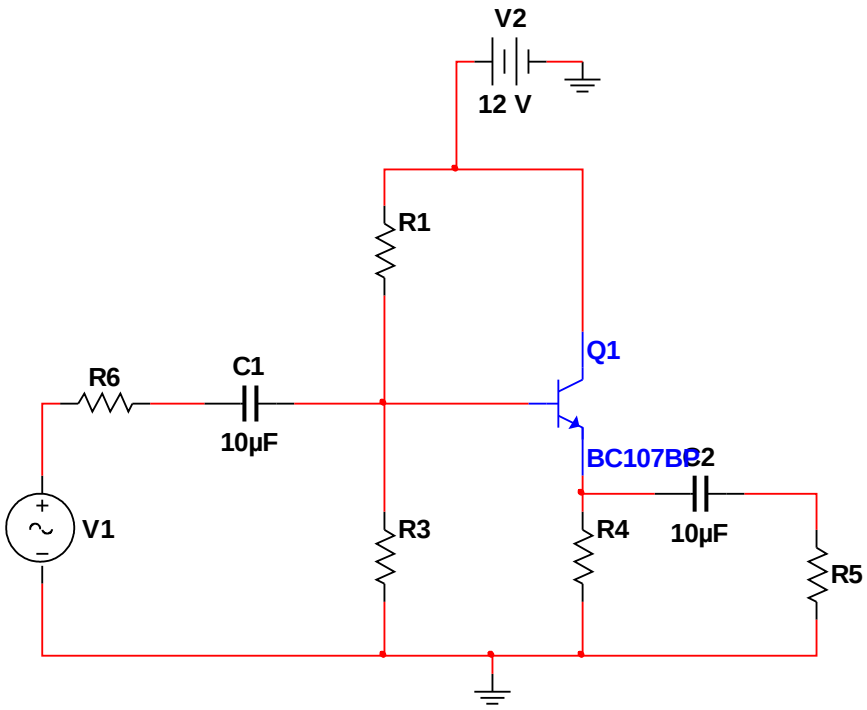
5) measure the output signal value and calculate the gain.
6) Keep the input voltage to any constant value within the range vary the frequency to a cetiain range.
7) Notedown the output values and tabultate them.
8) Plot frequency Vs gain.

Result:

Experiment no:3

DESIGN OF COMMON COLLECTOR AMPLIFIER

Aim:-
To design CC amplifier to find the frequency response.



Theory:-
It has high input resistance.
its output resistance is low.
its current gain is high
it has very high voltage gain lessthan 1.
It produces very high power gain in the order of 10 to 20 dB

Designing procedure:-

$$V_{CC} = 12\,V$$

$$Let\ (I_C, V_{CE}) = (2\text{mA}, 5\text{V})$$

$$R_E = \frac{V_{CC} - V_{CE}}{I_C}$$

$$\frac{V_{CC} \times R_2}{R_1 + R_2} = V_{Th}$$

$$R_i = R_{Th} \square \beta (r_e + R_E)$$

PROCEDURE:-

1)Take the components according to the teroritical design values.

2) connect the circuit as per the ckt diagram.
3) Apply DC input to circuit and mesure the DC conditions and notedown the values.
4) Apply AC signal using function generator and connect the output across the collector resistor RC
5) Measure the output signal value and calculate the gain.
6) Keep the input voltage to any constant value within the range vary the frequency to a certain range.
7) Notedown the output values and tabultate them.
8) Plot frequency Vs gain.

Result:-

Experiment no:4

DESIGN OF DIFFERENTIAL AMPLIFIER USING BJT WITH RESISTIVE LOAD.

Aim:-

To design differential amplifier using BJT with resistive load and to find out single ended output, differential output, frequency response, and Ad,Ac and CMRR.

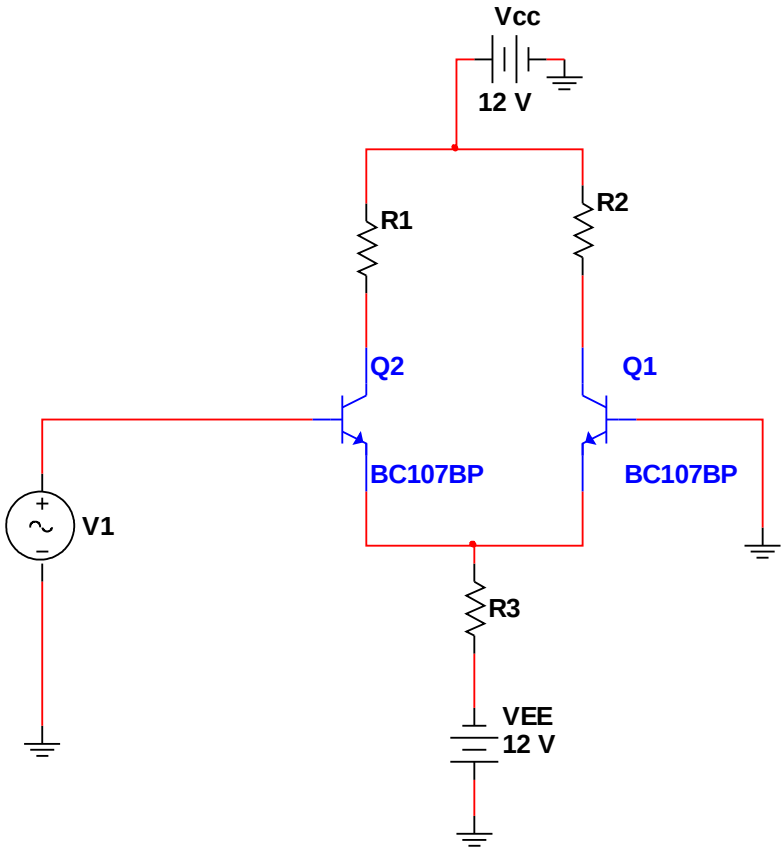


Figure 4.1

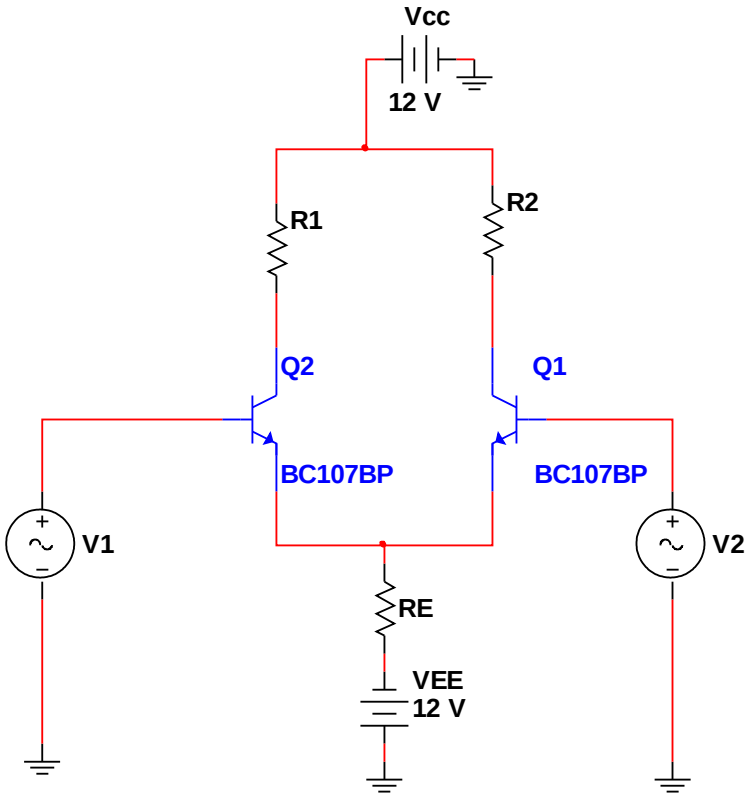


Figure 4.2

Theory:-

the differnetial ampliferi is the basis for the operationsl amplifier which has very high input resistance and gain.

The usefulness of differential pair stem from two way properties cascades of differential pairs can be directly connected to one another without interstage coupling capacitors.

To increase the range of differential mode input over which the emitter coupled pair behaves approximately as a linear amplifier, emitter degentaion resistors are frequently included in series with the emitter of transistors.

Designing procedure:-

$$V_{CC} = V_{EE} = 12\text{V}$$

$$Let\ (V_{CB}, I_C) = (5\text{V}, 0.5\text{mA})$$

$$I_O = I_{E1} + I_{E2}$$

$$R_E = \frac{V_{EE} - V_\gamma}{I_O}$$

$$A_d = \frac{-g_m R_C}{2}$$

$$A_c = \frac{-R_C}{r_e + 2R_E}$$

Procedure:-

1) Check the given equipment whether they are working properly of not and connect the circuit as shown in fig.
2) Set the DC voltages from DRPS and measure the DC conditions of the circuit.
3) Feed the differential signal to circuit from funciton generator and observe the single ended outputs at two outputs ports on the CRO.
4) Observe the differential ouptut using math function and notedown the values.
5) Calculate Ad, observe frequency response and measure signal hangling capacity.
6) Now feed the common mode signal by connection two base terminals to positive teminal of input and observe the same as that of differential input.
7) Calculate the common mode rejection ratio.

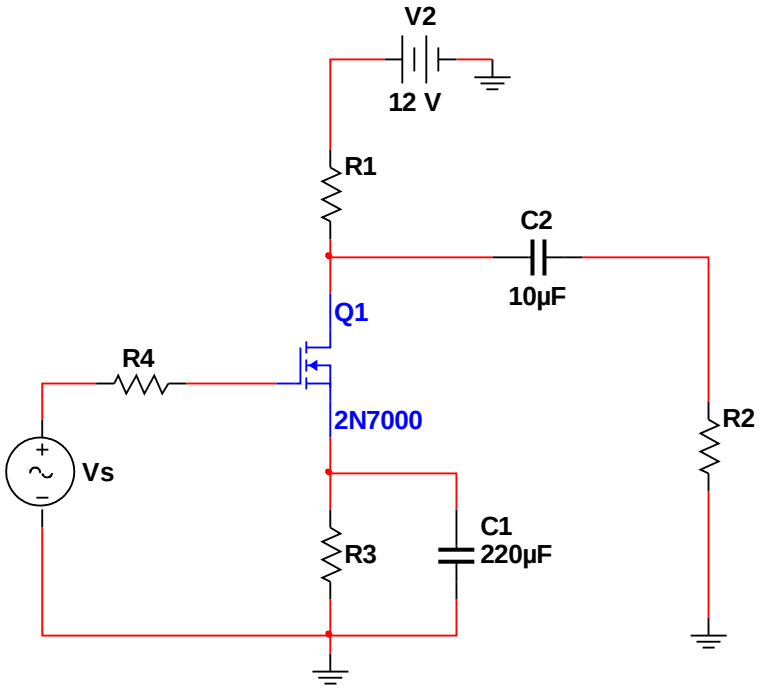
Result:-

Experiment no:5

DESIGN OF COMMON SOURCE AMPLIFIER

Aim:-

To design CS amplifier to find the frequency response.



Designing procedure:-

$$V_{DD} = V_{SS} = 12\text{V}$$

$$V_{GS} = \sqrt{\frac{I_{DSQ}}{K}} + V_T$$

$$I_D R_S \gg V_{GS}$$

$$R_D = \frac{V_{DD} - V_{DG}}{I_D}$$

$$R_S = \frac{V_{SS} - V_{GS}}{I_D}$$

PROCEDURE:-

1)Take the components according to the teroritical design values.

2) Connect the circuit as per the ckt diagram.
3) Apply DC input to circuit and mesure the DC conditions and notedown the values.
4) Apply AC signal using function gentator and connect the output across the collector resistor RC

5) measure the output signal value and calculate the gain.
6) Keep the input voltage to any constant value within the range vary the frequency to a certain range.

7) Notedown the output values and tabulate them.
8) Plot frequency Vs gain.

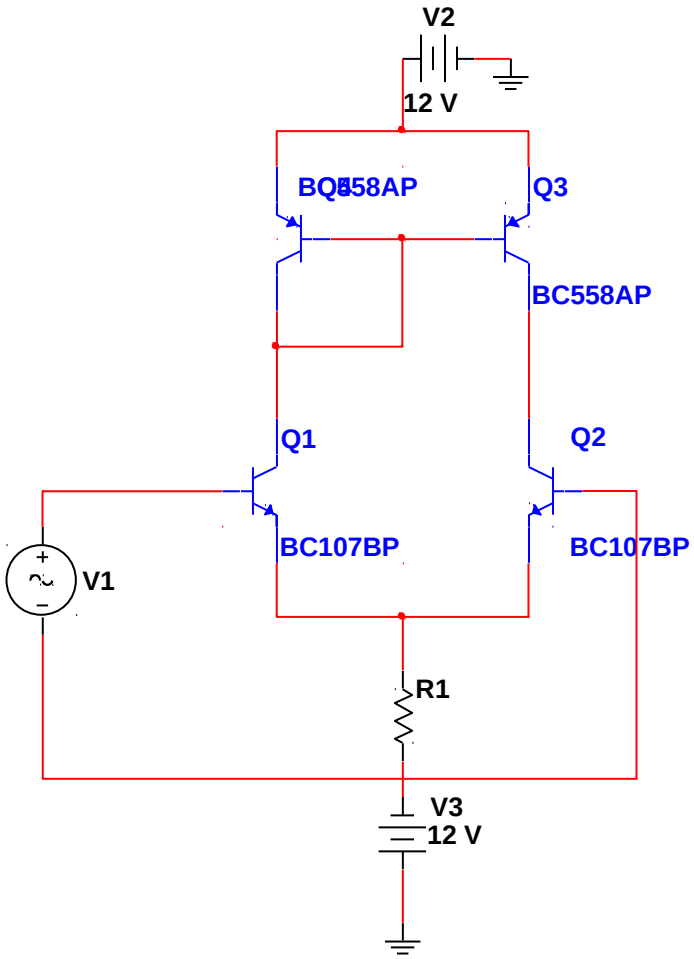
Result:-

Experiment no:6

DESIGN OF DIFFERENTIAL AMPLIFIER USING BJT WITH ACTIVE LOAD.

Aim:-

To design differential amplifier using BJT with active load and to find out single ended output, differential output, frequency response, and Ad,Ac and CMRR.



Theory:-

In the active load we use two npn transistors which identical and 2 pnp identical transsitors. In differential amplifier Rc is replaced by current mirror circuit which is acting as load. The current mirror circuit itself it contains active elements that's why we call it as activeload. By using theis acitveload we can get more fdifferential mode gain and CMRR can be improved.

Designing procedure:-

$V_{CC} = V_{EE} = 12V$

$I_{E1} = I_{E2} = 1mA$

$I_O = I_{E1} + I_{E2}$

$$R_E = \frac{V_{EE} - V_{BE}}{I_O}$$

PROCEDURE:-

1) Connect the circuit as per the ckt diagram.
2) Apply DC input to circuit and mesure the DC conditions and notedown the values.
3) Apply AC signal using function gentator and connect the output across the collector resistor RC.
4) measure the output signal value and calculate the gain.
5) Keep the input voltage to any constant value within the range vary the frequency to a cetiain range.
6) Notedown the output values and tabultate them.
7) Plot frequency Vs gain.

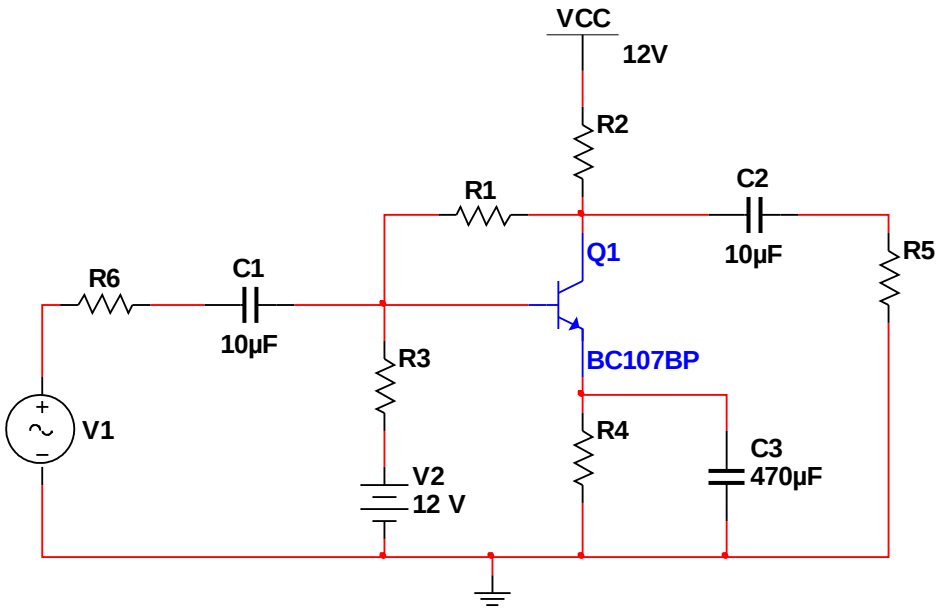
Result:-

Experiment no:7

DESIGN OF FEEDBACK AMPLIFIER USING BJT.

Aim:-

To design feedback amplifier with BJT and to find out the gain and frequency response with and without feedback network.



Theory:-

In a feedback amplifier a portion of the amplifier coutput Vo is connected to the feedback network which provides a reduced portion of the output as a feedback signal to the input mixer network.Depending an the relative poloarity of the signal bein feedback into a circuit. One may have negative or positive feedback resutls in decreased voltage gain.

PROCEDURE:-

1)Take the components according to the teroritical design values.

2) connect the circuit as per the ckt diagram.
3) Apply DC input to circuit and mesure the DC conditions and notedown the values.
4) Apply AC signal using function gentator and connect the output across the collector resistor RC
5) Measure the output signal value and calculate the gain.

6) Keep the input voltage to any constant value within the range vary the frequency to a cetiain range.
7) Notedown the output values and tabultate them.

8) Plot frequency Vs gain.
9) Repeat the steps from 3 to 6 for the network with feedback.
10) Compare the results of amplifier with and without feedback network.

Result:-

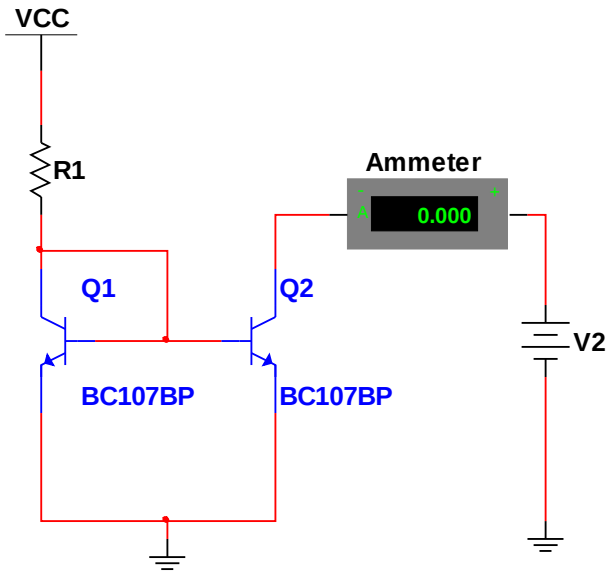
Experiment no:8

DESIGN AND CHARACTERIZATION OF SIMPLE CURRENT MIRROR CIRCUIT USING BJT.

Aim:-

1) To design simple current mirror circuit usign BJT.

2) To plot characteris of simple current mirror circuit and to find the output resistance.



Theory:-

Circuit consisting of two matching transistors with the collector of one connected to the bases of both, thus providing the same collector current in each transistor. Under ideal conditions, the current mirror gain is independent of input frequency and the voltage between the output and common terminals.

Designing procedure:-

$LetI = 1\text{mA}, V_{CC} = 6\text{V}$

$$\frac{V_{CC} - V_{BE}}{I} = R$$

PROCEDURE:-

1) connect the circuit as per the ckt diagram

2) measure the input current and compare it with Io.
3) Now vary the potentiometer value over the available range.. and measure the corresponding Io and output voltage Vo values.
4) Tabulate the values and plot the graph.
5) Now find out the output resistance values from the slope of the graph, it is similar to potentiometer value.

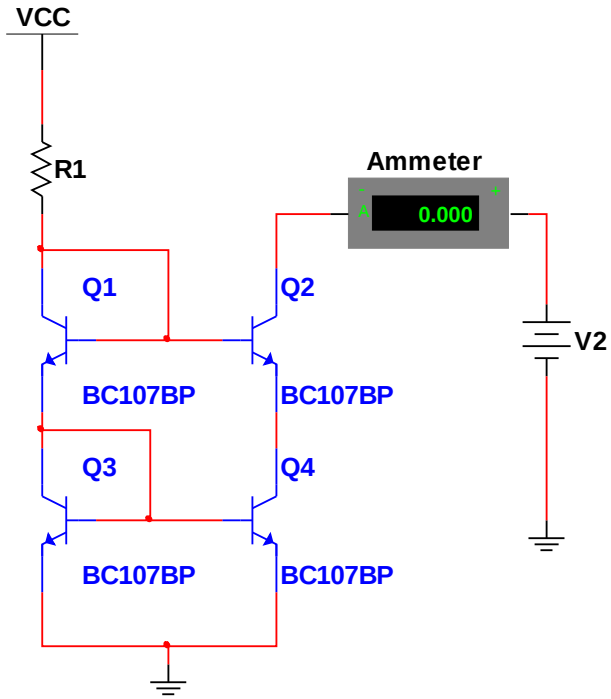
Result:-

Experiment no:9

DESIGN AND CHARACTERIZATION OF CASCODE CURRENT MIRROR CIRCUIT USING BJT.

Aim:-

To design cascode current mirror circuit usign BJT and to plot the characterization of the cascode current mirror.



Theory:-

Cascode is the combination of CE and CB amplifier. Emitter Terminal in the CE Configuration is connected to the emitter of CB.

The Cascode transistor raises the level of ouptut resistance. And the cascoding increases the magnitude of the open circuit voltage. A drawback of the cascode current mirror is that it consumes a relatively large portion of the steadily shrinking supply voltage the minimum voltage required across the output cascode mirror is 1V, this limits the signal swing at the output of mirror.

Designing procedure:-

$Let\ I = 1\text{mA}, V_{CC} = 6\text{V}$

$$\frac{V_{CC} - 2V_{BE}}{I} = R$$

PROCEDURE:-

1) connect the circuit as per the ckt diagram
2) measure the input current and compare it with Io.

3)Now vary the potentiometer value over the available range.. and measure the corresponding Io and output voltage Vo values.
4) Tabulate the values and plot the graph.
5) Now find out the output resistance values from the slope of the graph, it is similar to potentiometer value.

Result:-

IV.PROCEDURE:-

a) 70 students are divided into 23 batches with 3 students in each batch.
b) Labs session are conducted on basis on learning by doing.
c) every week one experiment is conducted.
d) students need to submit lab observation while leaving lab in each lab session.
e) lab reports has to submit every week.

V. STAFF:

LAB INCHARGE:

Lab Assistant: mohd.haneef